M68EML08GPGT

EMULATION MODULE

User's Manual

freescale™ semiconductor

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Quick Start Guide

Before you attempt an installation, disconnect any system cable connections and remove power. For instructions, consult the MMDS or MMEVS operations manuals.

Caution - *Ordinary amounts of static electricity from clothing or the work environment can damage or degrade electronic devices and equipment. For example, the electronic components installed on printed circuit boards are extremely sensitive to electrostatic discharge (ESD). Wear a ground wrist strap whenever handling any printed circuit board. This strap provides a conductive path for safely discharging static electricity to ground.*

Follow these quick-start steps to configure the M68EML08GPGT emulator module (GPGTEM) and install it in a Motorola Modular Development System (MMDS) or Motorola Modular Evaluation System (MMEVS). For other parts of system installation, see the MMDS or MMEVS hardware manuals.

1. Set the Configuration Headers to their Factory Defaults

To set the GPGTEM configuration headers to their factory defaults (For MC68HC908GT16 and MC68HC908KX8 emulation):

1. Make sure that a jumper is installed between pins 2 and 3 (LVDD) of configuration header J1.
2. Make sure that a jumper is installed between pins 2 and 3 (GND) of configuration header J2.
3. Make sure that a jumper is installed between pins 2 and 3 (LVDD) of configuration header J3.
4. Make sure that a jumper is installed between pins 2 and 3 (GND) of configuration header J6.
5. Make sure that NO jumper is installed on header J7.
6. Make sure that a jumper is installed on header J9.
7. Make sure that a jumper is installed between pins 1 and 2 (OSC1) of configuration header J10.

8. Make sure that a jumper is installed between pins 1 and 2 (PTE2) of configuration header J11.

9. Make sure that a jumper is installed between pins 3 and 4 (MMDS) of configuration header U11.

2. Install the GPGTEM

Once you have assured that the configuration headers are set to their factory defaults, you can install the GPGTEM in the MMDS or MMEVS.

Option 1 - To Install the GPGTEM in an MMDS Station Module

To install the GPGTEM in an MMDS station module:

1. Remove the entire top half of the station-module enclosure.

2. Fit together GPGTEM connectors J4 and J5 (on the bottom of the board) and control-board connectors P11 and P12.

3. Snap the corners of the GPGTEM onto the plastic standoffs.

Option 2 - To Install the GPGTEM in an MMEVS Station Module

To install the GPGTEM in an MMEVS station module:

1. Fit together GPGTEM connectors J4 and J5 (on the bottom of the board) and platform-board connectors P6 and P7.

2. Snap the corners of the EM onto the plastic standoffs.

3. Copy the Personality Files

To complete the installation, you must copy the personality files from the provided diskette to the directory that contains the debugging software. The personality files for the GPGTEM are:

- 00455Vxx.MEM — P&E Personality file for MC68HC908GT16 MCU

- 00C55Vxx.MEM — MCUez Personality file for MC68HC908GT16 MCU

At this point, the installation is complete. Remake any system cable connections and restore power. For instructions, consult the MMDS or MMEVS operations manuals.

Section 1. General Description

1.1 Introduction

The M68EML08GPGT emulator module (GPGTEM) lets you emulate and debug target systems based on the MC68HC908GT16 microcontroller unit (MCU). The GPGTEM is a low-voltage emulator operating in the range 2.7 to 5 Vdc which allows the emulation and debugging of target systems based on the followings microcontroller units (MCUs)

- MC68HC908GT16
- MC68HC908KX2/8

Replace the installed MC68HC908GT16 MCU with MC68HC908GP32 MCU on GPGTEM will enable GPGTEM to emulate the followings microcontroller units:

- MC68HC908GP20/32
- MC68HC908GR4/8
- MC68HC908JL3/MC68HC908JK3

This user's manual explains connection, configuration, and operation information specific to the M68EML08GPGT emulator module (EM).

Section 1 contains the following topics:

- Motorola Development Systems
  - The Motorola Modular Development System (MMDS)
  - The Motorola Modular Evaluation System (MMEVS)
- System Layout
- System Specifications

1.2 Freescale Development Systems

This section describes the two Freescale development systems that use the GPGTEM, and shows the GPGTEM’s layout.

The GPGTEM can be part of two Motorola development systems:

- MMDS0508 Freescale Modular Development System (MMDS)
- MMEVS0508 Freescale Modular Evaluation System (MMEVS)

1.2.1 Freescale Modular Development System

The MMDS is an emulator system that provides a bus state analyzer and real-time memory windows. The unit's integrated design environment includes an editor, an assembler, user interface, and source-level debug.

A complete MMDS consists of:

- Station module — The metal MMDS enclosure containing the control board and the internal power supply
- Emulator module — A separately purchased printed circuit board that enables system functionality for a specific set of MCUs
- Two logic clip cable assemblies — Twisted-pair cables that connect the station module to the target system, a test fixture, a clock, an oscillator, or any other circuitry useful for evaluation or analysis. One end of each cable assembly has a molded connector, which fits into station-module pod A or pod B. Leads at the other end of each cable terminate in female probe tips. Ball clips come with the cable assemblies.
- A 9-lead RS-232 serial cable — Cable that connects the station module to the host computer RS-232 port
- A 9- to 25-pin adapter — A molded assembly that connects the 9-pin cable to a 25-pin serial port
- System software — MCUez™ software on CD-ROM and P&E Microcomputer System, Inc. software on CD-ROM

- MMDS documentation — *MMDS Operations Manual*, Motorola document order number MMDS0508OM/D; the MCUez software manual, included with the MCUez software package; a system software manual, included with the P&E Microcomputer System, Inc.’s MMDS0508 software package; and this EM user's manual (this manual)

MMDS baud rates are selected by the user at 2400, 4800, 9600, 19,200, 38,400, or 57,600.

As mentioned, the GPGTEM gives the MMDS the ability to emulate target systems based on the MCUs specify in Section 1.1. By substituting a different EM, MMDS can be enabled to emulate target systems based on a different MCU. (A local Motorola representative can explain all the EMs available.)

1.2.2 Freescale Modular Evaluation System

An MMEVS is an economical, two-board tool for designing, debugging, and evaluating target systems based on MC68HC05 or MC68HC08 MCUs.

A complete MMEVS consists of:

- Platform board (PFB) — The bottom board, which supports the emulator module, has connectors for power and for a terminal or host computer
- Emulator module (EM) — A separately purchased printed circuit board that enables system functionality for a specific set of MCUs and fits onto the PFB
- RS-232 serial cable — A separately purchased cable that connects the PFB to the host computer RS-232 port
- System software — MCUez™ software on CD-ROM and P&E Microcomputer System, Inc. software on CD-ROM
- MMEVS documentation — *MMEVS Operations Manual*, Motorola document order number MMEVSOM/D; the MCUez software manual, included with the MCUez software package; a system software manual, included with the P&E Microcomputer System, Inc.’s MMEVS0508 software package; and this emulator user's manual

An MMEVS features automatic selection of the communication baud rate from these choices: 2400, 4800, 9600, 19,200, 38,400, or 57,600.

When used with an GPGTEM, the MMEVS emulates target systems based on the MCUs specify in Section 1.1. By substituting a different EM, the MMEVS can be enabled to emulate target systems based on a different MCU. (A local Motorola representative can explain all the EMs available.)

1.3 GPGTEM Layout

Figure 1-1. shows the layout of the GPGTEM.

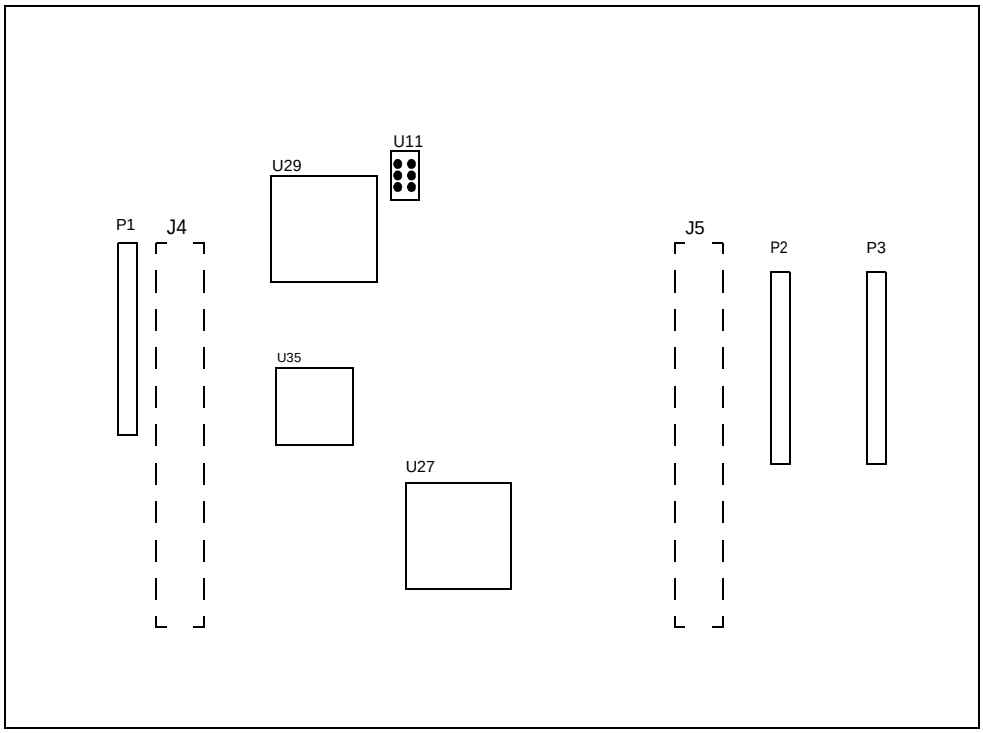


Figure 1-1. M68EML08GPGT Emulator Module

The main elements of the GPGTEM are:

- DIN connectors J4 and J5 — Connect the EM to the MMDS control board or the MMEVS platform board
- Connector P1 — Permits connection to a logic analyzer
- Jumper header U11 — GPGTEM internal clock source selector
- Connectors P2 and P3 — Customer-specific interfaces to the target system

The GPGTEM requires a user-supplied 80-lead target cable and target head adapter to connect the target system to connectors P2 and P3.

1.4 Specifications

Table 1-1. lists GPGTEM specifications.

Table 1-1. GPGTEM Specifications

Characteristics	Specifications
MCU extension I/O ports	HCMOS compatible
Operating temperature	0° to 40°C
Storage temperature	–40° to +85°C
Relative humidity	0 to 90% (non-condensing)
Power requirements	+5 V dc and +12 V dc (charge pump), provided from the MMDS control board or MMEVS platform board
Dimensions	8.27 x 7 inches; 210 x 178 mm
Weight	200g; 4.44 ounce

Section 2. Configuration and Operation

2.1 Introduction

This section explains configuration and operation of the GPGTEM when it is installed in a Motorola Modular Development System (MMDS) or Motorola Modular Evaluation System (MMEVS). Individual topics discussed in this section are:

- Setting Jumpers on Configuration Headers
  - ADC Module Voltage Selector (J1-J3, J6)
  - GP/GR/JL/JK series MCU emulation enable (J7)
  - JL3 ADC module Voltage Enable (J9)
  - Clock source Selector (J10)
  - PTE2/CGMXFC function Selector (J11)
  - Internal Clock Selector (U11)

For other parts of system installation or configuration, see the MMDS or MMEVS hardware manuals.

Note - *An GPGTEM already installed in an MMDS station module can be reconfigured. To do so, switch off station-module power, then follow the guidance in this section. Similarly, an GPGTEM that is already installed on the MMEVS platform board can be reconfigured, provided that platform-board power is disconnected.*

Caution - *Be sure to switch off or disconnect power when reconfiguring an installed EM. Reconfiguring EM jumper headers with the power on can damage system circuits.*

Caution - *Ordinary amounts of static electricity from clothing or the work environment can damage or degrade electronic devices and equipment. For example, the electronic components installed on printed circuit boards are extremely sensitive to electrostatic discharge (ESD). Wear a ground wrist strap whenever handling any printed circuit board. This strap provides a conductive path for safely discharging static electricity to ground.*

2.2 Installation of Microcontroller on GPGTEM

The default factory configuration, with an MC68HC908GT16 MCU installed in socket U29, enabling GPGTEM to emulate MC68HC908GT16 and MC68HC908KX2/8.

Users could reconfigure the GPGTEM to emulate MC68HC908GP20/32, MC68HC908GR4/8 and MC68HC908JL3/JK3 by substituting the MC68HC908GT16 with MC68HC908GP32 on socket U29 of GPGTEM.

Note - *Please ensure the MMDS station had switched off when installing the MCU on GPGTEM. Similarly, disconnected power from the MMEVS platform board during the re-configuration of GPGTEM.*

2.3 Setting Jumpers on Configuration Headers

The GPGTEM has nine configuration headers. Table 2-1. contains a summary of settings for these headers. The following sections give additional information about each jumper headers.

Table 2-1. Configuration Headers

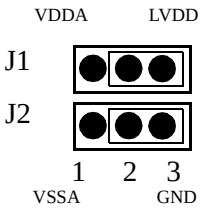
Configuration Header	Type	Description
J1 & J2		***For GT16/KX8 emulation*** Jumpers between pins 1 and 2 on J1 & J2 select the VDDA and VSSA from target system as the analog voltage source for the MC68HC908GT16 ADC module. Jumpers between pins 2 and 3 on J1 & J2 (factory default) select the isolated on-board voltage sources LVDD and GND as the analog voltage source for the MC68HC908GT16 ADC module. ***For GT32/GR8/Jl3/JK3 emulation*** Jumpers must be installed between pins 2 and 3 on J1 & J2 to select the isolated on-board voltage sources LVDD and GND as the voltage source for the **MC68HC908GP32** PLL module.

Table 2-1. Configuration Headers

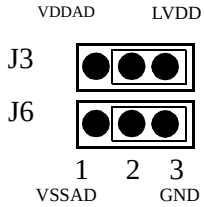
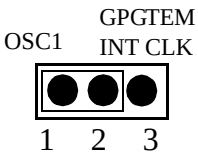
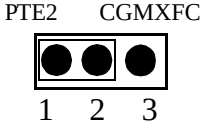
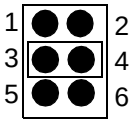
J3 & J6		***For GT/KX emulation*** Jumpers between pins 1 and 2 on J3 & J6 select the VDDAD and VSSAD from the target system as the analog voltage references for the MC68HC908GT16 ADC module. Jumpers between pins 2 and 3 on J3 & J6 (factory default) select the isolated on-board voltage sources LVDD and GND as the analog voltage references for the MC68HC908GT16 ADC module. ***For GP/GR/JL/JK emulation*** Jumpers between pins 1 and 2 on J3 & J6 select the VDDAD and VSSAD from the target system as the analog voltage sources for the **MC68HC908GP32** ADC module. Jumpers between pins 2 and 3 on J3 & J6 (factory default) selects the isolated on-board voltage sources LVDD and GND as the analog voltage sources for the **MC68HC908GP32** ADC module.
J7		No jumper between pins 1 and 2 (factory default) configure the GPGTEM to emulate MC68HC908GT16 and MC68HC908KX8 A jumper between pins 1 and 2 configure the GPGTEM to emulate MC68HC908GP20/32, MC68HC908GR4/8, MC68HC908JL3 and MC68HC908JK3.
J9		***For JL/JK emulation only*** No jumper between pins 1 and 2 disconnect VDDAD from LVDD on the ADC replacement on GPGTEM. A jumper between pins 1 and 2 (factory default) connect LVDD to VDDAD on ADC replacement unit for JL3 ADC module emulation on GPGTEM.
J10		A jumper between pins 1 and 2 (factory default) select an external clock source for the OSC1 (PTE4 on GT16) input signal from target head connectors. A jumper between pins 2 and 3 select an internal clock source generated by GPGTEM (See U11 for internal clock selection) for the OSC1 input signal.
J11		A jumper between pins 1 and 2 (factory default) enable PTE2 function for GT16. A jumper between pins 2 and 3 enable CGMXFC function for GP32 and GR4/8.

Table 2-1. Configuration Headers

U11		A jumper between pins 1 and 2 selects the onboard 32.768-kHz crystal oscillator as the clock source. A jumper between pins 3 and 4 (factory default) selects the clock signal from the MMDS control board or MMEVS platform board. A jumper between pins 5 and 6 selects the onboard 32MHz oscillator as the clock source.

2.3.1 ADC Module Voltage Selector (J1-J3, J6)

2.3.1.1 *For GT/KX emulation*

Configuration Headers J1 and J2 are used to select the on-board voltage source (LVDD and GND) or an external analog voltage supply (VDDA and VSSA) as the voltage sources for the MC68HC908GT16 ADC module. The following figure shows the default factory jumper headers configuration, which has fabricated jumpers installed between pins 2 and 3 on J1 and J2.

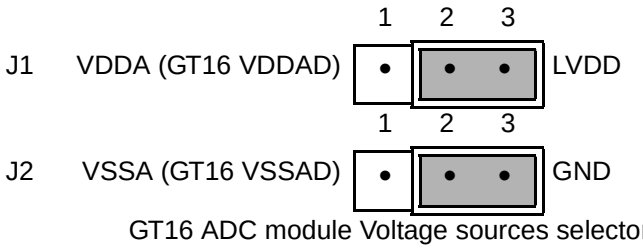


Figure 2-1. Configuration Headers J1& J2 (For GT/KX emulation)

Configuration Headers J3 and J6 are used to select the on-board voltage source (LVDD and GND) or an external analog voltage reference (VDDAD and VSSAD) as the voltage reference for the MC68HC908GT16 ADC module. The following figure shows the default factory jumper headers configuration, which has fabricated jumpers installed between pins 2 and 3 on J3 and J6

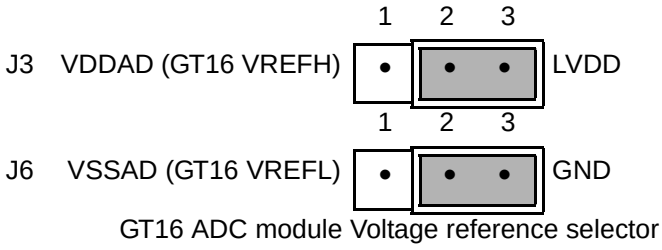


Figure 2-2. Configuration Header J3 & J6 (For GT/KX emulation)

2.3.1.2 *For GP/GR/JL/JK emulation*

Jumpers must be installed between pins 2 and 3 on J1 and J2 when configure GPGTEM to emulate GP/GR/JL/JK MCUs series. These connections will connect the on-board voltage source (LVDD and GND) for the MC68HC908GP32 PLL module. The following figure shows the default factory jumper headers configuration, which has fabricated jumpers installed between pins 2 and 3 on J1 and J2

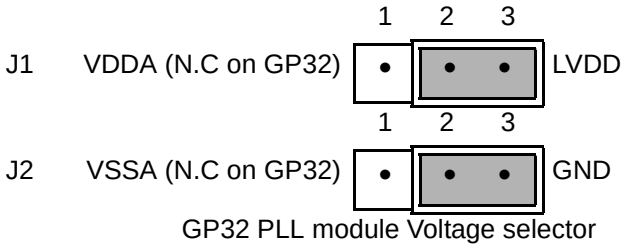


Figure 2-3. Configuration Headers J1& J2 (For GP/GR/JL/JK emulation)

Configuration Headers J3 and J6 are used to select the on-board voltage source (LVDD and GND) or an external analog voltage sources (VDDAD and VSSAD) as the voltage sources and voltage reference for the MC68HC908GP32 ADC module. The following figure shows the default factory jumper headers configuration, which has fabricated jumpers installed between pins 2 and 3 on J3 and J6

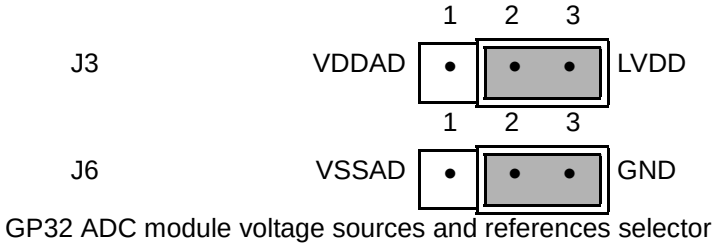


Figure 2-4. Configuration Header J3 & J6 (For GP/GR/JL/JK emulation)

2.3.2 GP/GR/JL/JK Microcontroller series emulation enable (J7)

Use Configuration Header J7 to select microcontrollor series for GPGTEM to emulate. The factory configuration, with no fabricated jumper between pins 1 and 2, configure the GPGTEM to emulate MC68HC908GT16 or MC68HC908KX2/8.

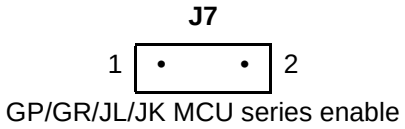


Figure 2-5. Configuration Header J7

Alternatively, a fabricated jumper on pin 1 and pin 2 will configure the GPGTEM to emulate the MC68HC908GP20/32, MC68HC908GR4/8 and MC68HC908JL3/JK3

2.3.3 JL3 ADC module Voltage Enable (J9)

Use Configuration Header J9 to connect LVDD (from GPGTEM) to VDDAD of the ADC replacement unit for JL3 ADC module emulation. Do not remove the fabricated jumper from J9 when emulating MC68HC908JL3/JK3. (For MC68HC908JL/JK MCU series emulation only)

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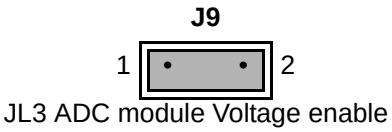

Figure 2-6. Configuration Header J9

2.3.4 Clock Source Selector (J10)

Use Configuration Header J10 to select external clock source or the internal clock signal generated by the GPGTEM for OSC1 input. The factory configuration, with a fabricated jumper between pins 1 and 2, selects target system clock signal OSC1 (PTE4 of GT16) from

pin 3 of target head connector P3. Jumper installed on pins 2 and 3 will select the internal clock signal from GPGTEM. The default setting is shown in the following figure.

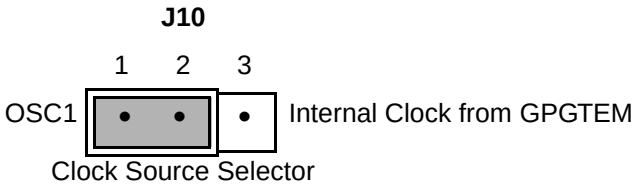

Figure 2-7. Configuration Header J10

Note - *•See Section 2.3.6 for internal clock source selection on GPGTEM*

2.3.5 PTE2/CGMXFC function selector (J11)

Use Configuration Header J11 to select PTE2 port function for MC68HC908GT16 or CFMXFC function for MC68HC908GP32. The factory configuration, with a fabricated jumper between pins 1 and 2, enables PTE2 port function for MC68HC908GT16 on GPGTEM. (with MC68HC908GT16 MCU installed on socket U29 of GPGTEM)

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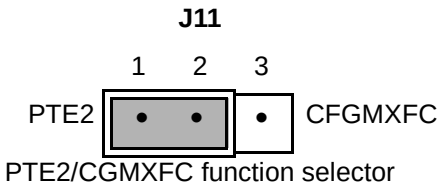

Figure 2-8. Configuration Header J11

Alternatively, install the fabricated jumper between pins 2 and 3 will enable CGMXFC pin function for MC68HC908GP32 emulation on GPGTEM. (with MC68HC908GP32 MCU installed on socket U29 of GPGTEM)

2.3.6 Internal Clock Selector (U11)

Use Configuration Header U11 to determine the internal clock signal source for GPGTEM. The factory configuration, with a fabricated jumper between pins 3 and 4, selects the clock

signal from the MMDS control board or MMEVS platform board. This default is shown in the following figure.

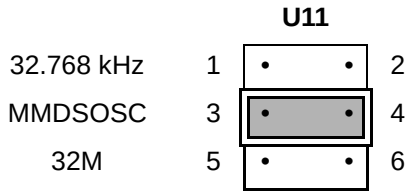

Figure 2-9. Configuration Header U11

Alternatively, as shown in the figure, two other clock signal sources can be selected:

- To select the on-board 32.768-kHz crystal oscillator, install the fabricated jumper between pin 1 and 2.
- To select the on-board 32MHz oscillator, install the fabricated jumper between pin 5 and 6.

Note - *• Users can select the target system as the clock source, by install the fabricated jumper between pins 1 and 2 (OSC1) on J10. Ensure that the clock source (OSC1) is connected to the EM through the target cable, connector P3 pin 3. (See Section 2.3.4 for clock source selection on GPGTEM)*

Caution - *Only one jumper should be inserted on jumper header U11 at a time. Inserting multiple jumpers in U11 might damage the GPGTEM.*

2.4 Completing the Installation

Once the Configuration Headers are jumpered and Microcontroller to be emulated had installed, follow these steps to complete the GPGTEM installation:

- To install the GPGTEM in an MMDS station module, remove the entire top half of the station-module enclosure. Fit together EM connectors J4 and J5 (on the bottom of the board) and control-board connectors P11 and P12. Snap the corners of the EM onto the plastic standoffs.
- To install the GPGTEM on an MMEVS platform board, fit together EM connectors J4 and J5 (on the bottom of the board) and platform-board connectors P6 and P7. Snap the corners of the EM onto the plastic standoffs.
- Copy the personality files from the provided diskette to the directory that contains the debugging software. The personality files for the GPGTEM are:
  - 00455Vxx.MEM — P&E Personality file for MC68HC908GT16 MCU
  - 00C55Vxx.MEM — MCUez Personality file for MC68HC908GT16 MCU
- To emulate other HC08 MCU series supported by GPGTEM, you have to rename the appropriate .mem file to 00455vxx.MEM and 00C55Vxx.MEM for P&E and MCUez software respectively.
- For example, if you were going to emulate a JL3 MCU by GPGTEM on MCUez software, you would rename the file 0jl3v01.mem to 00c55v01.mem. If there are 00c55vxx.mem files already existing in the directory, please save them as .bak files.
- The following personality files are included in the provided diskette for GPGTEM to emulate other supported HC08 MCUs.
  - 0gp20v01.mem — Personality file for MC68HC908GP20 MCU
  - 0gp32v01.mem — Personality file for MC68HC908GP32 MCU
  - 0gr4v01.mem — Personality file for MC68HC908GR4 MCU
  - 0gr8v01.mem — Personality file for MC68HC908GR8 MCU
  - 0jl3v01.mem — Personality file for MC68HC908JL3 MCU

At this point, make any system cable connections and restore power. For instructions, consult the MMDS or MMEVS operations manuals.

Section 3. Connector Information

3.1 Introduction

This section consists of pin assignments and signal descriptions for GPGTEM target and logic analyzer connectors. Specific topics discussed in the following paragraphs are:

- Logic Analyzer Connector (P1)
- Target Connectors (P2 and P3)
- Pin assignments for MCUs supported by GPGTEM
- Target Cable Assembly

3.2 Logic Analyzer Connector (P1)

Connector P1 is the GPGTEM logic analyzer connector. Figure 3-1. shows the pin assignments for connector P1. Table 3-1. gives the signal descriptions.

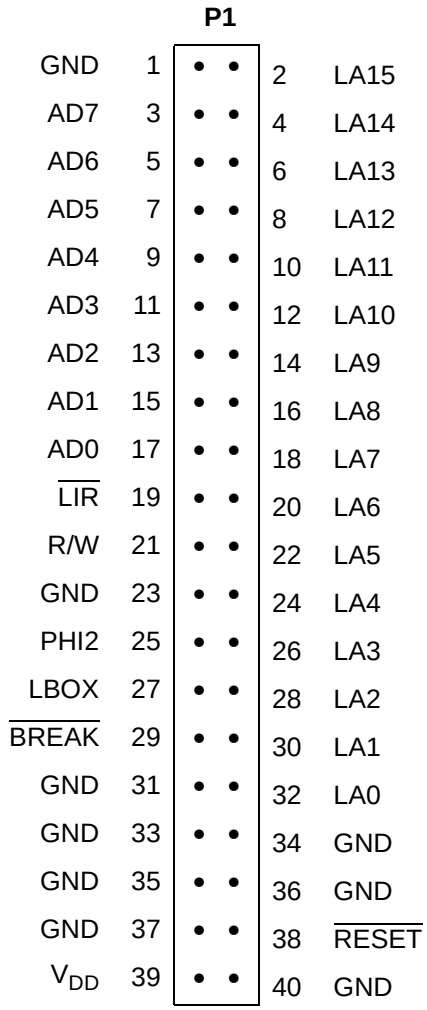

Figure 3-1. Logic Analyzer Connector (P1) Pin Assignments

Table 3-1. Logic Analyzer Connector (P1) Signal Descriptions

Pin	Mnemonic	Signal Description
1	GND	GROUND
2	LA15	Address bus bit 15 — MCU output address bus
3	AD7	Data bus bit 7 — MCU bidirectional data bus
4	LA14	Address bus bit 14 — MCU output address bus
5	AD6	Data bus bit 6 — MCU bidirectional data bus
6	LA13	Address bus bit 13 — MCU output address bus
7	AD5	Data bus bit 5 — MCU bidirectional data bus
8	LA12	Address bus bit 12 — MCU output address bus
9	AD4	Data bus bit 4 — MCU bidirectional data bus
10	LA11	Address bus bit 11 — MCU output address bus
11	AD3	Data bus bit 3 — MCU bidirectional data bus
12	LA10	Address bus bit 10 — MCU output address bus
13	AD2	Data bus bit 2 — MCU bidirectional data bus
14	LA9	Address bus bit 9 — MCU output address bus
15	AD1	Data bus bit 1 — MCU bidirectional data bus
16	LA8	Address bus bit 8 — MCU output address bus
17	AD0	Data bus bit 0 — MCU bidirectional data bus
18	LA7	Address bus bit 7 — MCU output address bus.
19	$\overline{\text{LIR}}$	Load instruction register — Active-low output signal, asserted when an instruction starts
20	LA6	Address bus bit 6 — MCU output address bus
21	R/W	Read/Write — Output signal that indicates the direction of data transfer
22	LA5	Address bus bit 5 — MCU output address bus
23	GND	GROUND
24	LA4	Address bus bit 4 — MCU output address bus
25	PHI2	PHI2 clock — Internally generated output clock signal used as a timing reference
26	LA3	Address bus bit 3 — MCU output address bus
27	LBOX	Last bus cycle — Input signal that the emulator asserts to indicate that the target system MCU is in the last bus cycle of an instruction
28	LA2	Address bus bit 2 — MCU output address bus

Table 3-1. Logic Analyzer Connector (P1) Signal Descriptions (Continued)

Pin	Mnemonic	Signal Description
29	$\overline{\text{BREAK}}$	$\overline{\text{BREAK}}$ — Active low signal that the EM asserts to stop the target system MCU from running user code
30	LA1	Address bus bit 1 — MCU output address bus
31	GND	GROUND
32	LA0	Address bus bit 0 — MCU output address bus
33	GND	GROUND
34	GND	GROUND
35	GND	GROUND
36	GND	GROUND
37	GND	GROUND
38	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ — Active-low bidirectional signal for starting an EVS reset
39	V_{DD}	+5 Vdc power — Input voltage (+5 Vdc @ 1A (max)) used by the EM logic circuits
40	GND	GROUND

3.3 Target Connectors (P2 and P3)

GPGTEM has two target connectors: P2 and P3, each a 2-row by 20-pin connector. Figure 3-2., Table 3-2., and Table 3-3. give the pin assignments and signal descriptions for these connectors

Note - *All the MCUs emulated by GPGTEM will be connected to their target heads based on different package assignments. Unless specify, all target signals in P2 and P3 support across the MCUs list in Section 1.1.*

.

P2

GND	1	• •	2	PTC1
NC	3	• •	4	GND
GND	5	• •	6	PTC4
PTA7	7	• •	8	RESERVED
PTA6	9	• •	10	PTB4 (KX8)
PTA4	11	• •	12	PTB5 (KX8)
PTA2	13	• •	14	PTA2 (KX8)
PTA0	15	• •	16	PTA3 (KX8)
V_{DDAD}	17	• •	18	NC
GND	19	• •	20	PTE2 (GT16)
PTA6 (JL3)	21	• •	22	PTB5
NC	23	• •	24	GND
NC	25	• •	26	PTB2
NC	27	• •	28	PTB0
NC	29	• •	30	PTD6
PTB7 (KX8)	31	• •	32	PTD5
NC	33	• •	34	EV_{DD}
PTE1	35	• •	36	PTD3
PTD0	37	• •	38	GND
PTD2	39	• •	40	GND

P3

$\overline{\text{RESET}}$	1	• •	2	PTC0
OSC1	3	• •	4	PTC2
NC	5	• •	6	PTC3
NC	7	• •	8	PTC5
GND	9	• •	10	PTC6
PTA5	11	• •	12	NC
PTA3	13	• •	14	GND
PTA1	15	• •	16	V_{DDA} (GT16)
V_{SSAD}	17	• •	18	V_{SSA} (GT16)
PTB7	19	• •	20	NC
OSC2 (GT16)	21	• •	22	PTB6
NC	23	• •	24	PTB4
NC	25	• •	26	PTB3
GND	27	• •	28	PTB1
NC	29	• •	30	PTD7
PTD6 (JL3)	31	• •	32	GND
PTD7 (JL3)	33	• •	34	PTD4
PTE0	35	• •	36	GND
$\overline{\text{IRQ}}$	37	• •	38	GND
PTD1	39	• •	40	GND

Figure 3-2. Target Connectors (P2 and P3) Pin Assignments

Table 3-2. Target Connector (P2) Signal Descriptions

Pin	Mnemonic	Signal Description
1	GND	EM GROUND — Ground signal of the EM board
2	PTC1	PORT C (bit 1) — General-purpose I/O lines controlled by software via data direction and data registers
3	NC	No connect
4, 5	GND	EM GROUND — Ground signal of the EM board
6	PTC4	PORT C (bit 4) — General-purpose I/O lines controlled by software via data direction and data registers
7	PTA7	PORT A (bit 7) — General-purpose I/O lines controlled by software via data direction and data registers
8	RESERVED	Reserved
9	PTA6	PORT A (bit 6) — General-purpose I/O lines controlled by software via data direction and data registers
10	PTB4 (KX8 only)	PORT B (bit 4) — General-purpose I/O lines controlled by software via data direction and data registers
11	PTA4	PORT A (bit 4) — General-purpose I/O lines controlled by software via data direction and data registers
12	PTB5 (KX8 only)	PORT B (bit 5) — General-purpose I/O lines controlled by software via data direction and data registers
13	PTA2	PORT A (bit 2) — General-purpose I/O lines controlled by software via data direction and data registers
14	PTA2 (KX8 only)	PORT A (bit 2) — General-purpose I/O lines controlled by software via data direction and data registers
15	PTA0	PORT A (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers
16	PTA3 (KX8 only)	PORT A (bit 3) — General-purpose I/O lines controlled by software via data direction and data registers
17	V_{DDAD}	GP20/32 and GR4/8: Analog supply pin and ADC voltage reference high for ADC convertor GT16: ADC voltage reference high
18	NC	No connect
19	GND	EM GROUND — Ground signal of the EM board
20	PTE2 (GT16 only)	PORT E (bit 2) — General-purpose I/O lines controlled by software via data direction and data registers

Table 3-2. Target Connector (P2) Signal Descriptions (Continued)

Pin	Mnemonic	Signal Description
21	PTA6 (JL3 only)	PORT A (bit 6) — General-purpose I/O lines controlled by software via data direction and data registers
22	PTB5	PORT B (bit 5) — General-purpose I/O lines controlled by software via data direction and data registers
23	NC	No connect
24	GND	EM GROUND – Ground signal of the EM board.
25	NC	No connect
26	PTB2	PORT B (bit 2) — General-purpose I/O lines controlled by software via data direction and data registers
27	NC	No connect
28	PTB0	PORT B (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers
29	NC	No connect
30	PTD6	PORT D (bit 6) — General-purpose I/O lines controlled by software via data direction and data registers
31	PTB7 (KX8 only)	PORT B (bit 7) — General-purpose I/O lines controlled by software via data direction and data registers
32	PTD5	PORT D (bit 5) — General-purpose I/O lines controlled by software via data direction and data registers
33	NC	No connect
34	EV_{DD}	Target system Voltage high
35	PTE1	PORT E (bit 1) — General-purpose I/O lines controlled by software via data direction and data registers
36	PTD3	PORT D (bit 3) — General-purpose I/O lines controlled by software via data direction and data registers
37	PTD0	PORT D (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers
38	GND	EM GROUND — Ground signal of the EM board
39	PTD2	PORT D (bit 2) — General-purpose I/O lines controlled by software via data direction and data registers
40	GND	EM GROUND — Ground signal of the EM board

Table 3-3. Target Connector (P3) Signal Descriptions

Pin	Mnemonic	Signal Description
1	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ — Active-low bidirectional control line that initializes the MCU
2	PTC0	PORT C (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers
3	OSC1	OSCILLATOR — Crystal oscillator amplifier input signal
4	PTC2	PORT C (bit 2) — General-purpose I/O lines controlled by software via data direction and data registers
5	NC	No connect
6	PTC3	PORT C (bit 3) — General-purpose I/O lines controlled by software via data direction and data registers
7	NC	No connect
8	PTC5	PORT C (bit 5) — General-purpose I/O lines controlled by software via data direction and data registers
9	GND	EM GROUND — Ground signal of the EM board
10	PTC6	PORT C (bit 6) — General-purpose I/O lines controlled by software via data direction and data registers
11	PTA5	PORT A (bit 5) — General-purpose I/O lines controlled by software via data direction and data registers
12	NC	No connect
13	PTA3	PORT A (bit 3) — General-purpose I/O lines controlled by software via data direction and data registers
14	GND	EM GROUND — Ground signal of the EM board
15	PTA1	PORT A (bit 1) — General-purpose I/O lines controlled by software via data direction and data registers
16	V_{DDA} (GT16 only)	GT16: Analog supply pin for ADC convertor
17	V_{SSAD}	GP20/32 and GR4/8: Analog ground pin and ADC voltage reference low for ADC convertor GT16: ADC voltage reference low
18	V_{SSA} (GT16 only)	GT16: Analog ground pin for ADC convertor
19	PTB7	PORT B (bit 7) — General-purpose I/O lines controlled by software via data direction and data registers
20	NC	No connect

Table 3-3. Target Connector (P3) Signal Descriptions (Continued)

Pin	Mnemonic	Signal Description
21	OSC2 (GT16/KX)	OSCILLATOR2 — Crystal oscillator amplifier output signal
22	PTB6	PORT B (bit 6) — General-purpose I/O lines controlled by software via data direction and data registers
23	NC	No connect
24	PTB4	PORT B (bit 4) — General-purpose I/O lines controlled by software via data direction and data registers
25	NC	No connect
26	PTB3	PORT B (bit 3) — General-purpose I/O lines controlled by software via data direction and data registers
27	GND	EM GROUND — Ground signal of the EM board
28	PTB1	PORT B (bit 1) — General-purpose I/O lines controlled by software via data direction and data registers
29	NC	No connect
30	PTD7 (GP32)	PORT D (bit 7) — General-purpose I/O lines controlled by software via data direction and data registers
31	PTD6 (JL3)	PORT D (bit 6) — General-purpose I/O lines controlled by software via data direction and data registers
32	GND	EM GROUND — Ground signal of the EM board
33	PTD7 (JL3)	PORT D (bit 7) — General-purpose I/O lines controlled by software via data direction and data registers
34	PTD4	PORT D (bit 4) — General-purpose I/O lines controlled by software via data direction and data registers
35	PTE0	PORT E (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers
36	GND	EM GROUND — Ground signal of the EM board
37	$\overline{\text{IRQ}}$	INTERRUPT REQUEST — Active-low input line for requesting MCU asynchronous non-maskable interrupt
38	GND	EM GROUND — Ground signal of the EM board
39	PTD1	PORT D (bit 1) — General-purpose I/O lines controlled by software via data direction and data registers
40	GND	EM GROUND — Ground signal of the EM board

3.4 Pin assignments for MCUs supported by GPGTEM

The GPGTEM can emulating and debugging of target systems based on the MC68HC908GP20/32, MC68HC908GR4/8, MC68HC908GT16, MC68HC908JL3/JK3 and MC68HC908KX2/8 MCUs. GPGTEM will use different pin assignment on emulating different MCUs mention above. The following sections give the pin assignments of GPGTEM on different MCU configurations.

3.4.1 Pin assignments for MC68HC908GP20/32

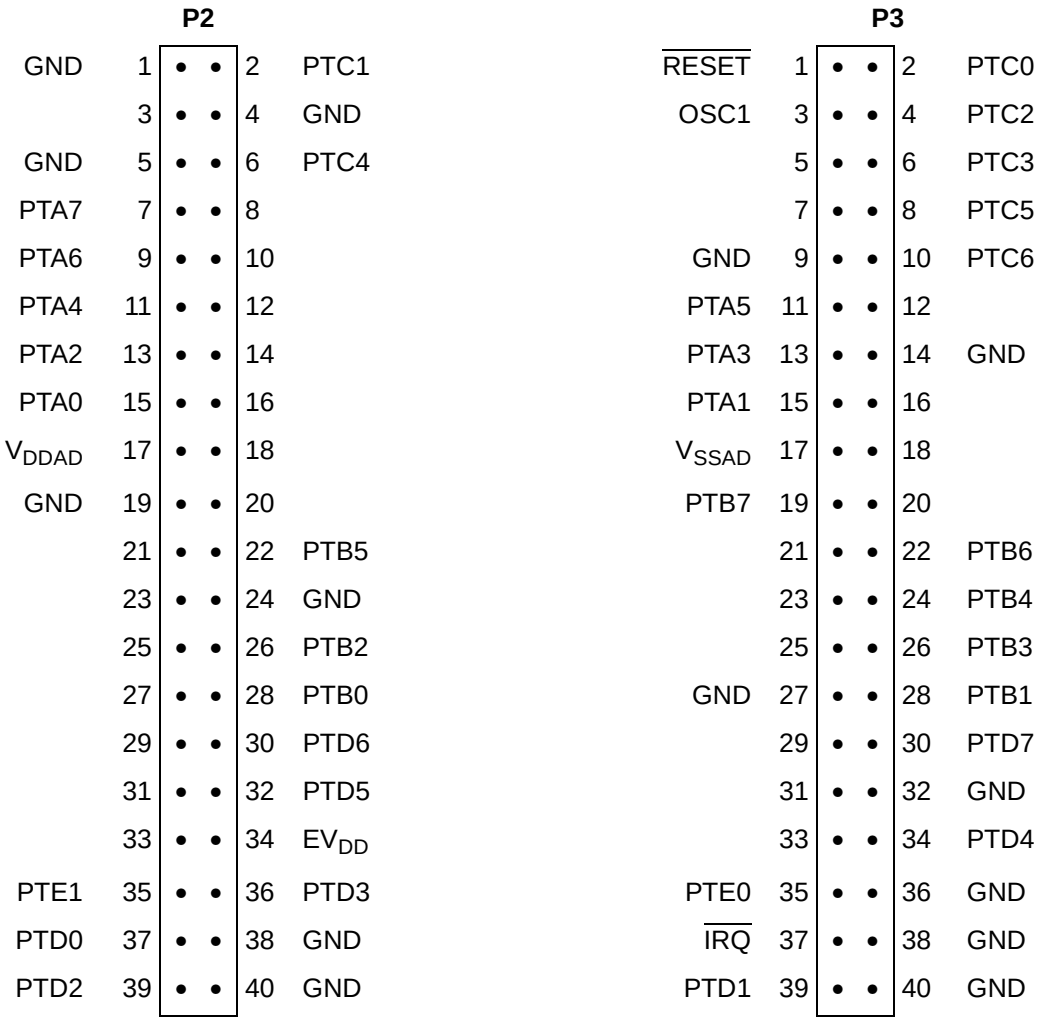

Figure 3-3. MC68HC908GP20/32 Pin Assignments

3.4.2 Pin assignments for MC68HC908GR4/8

.

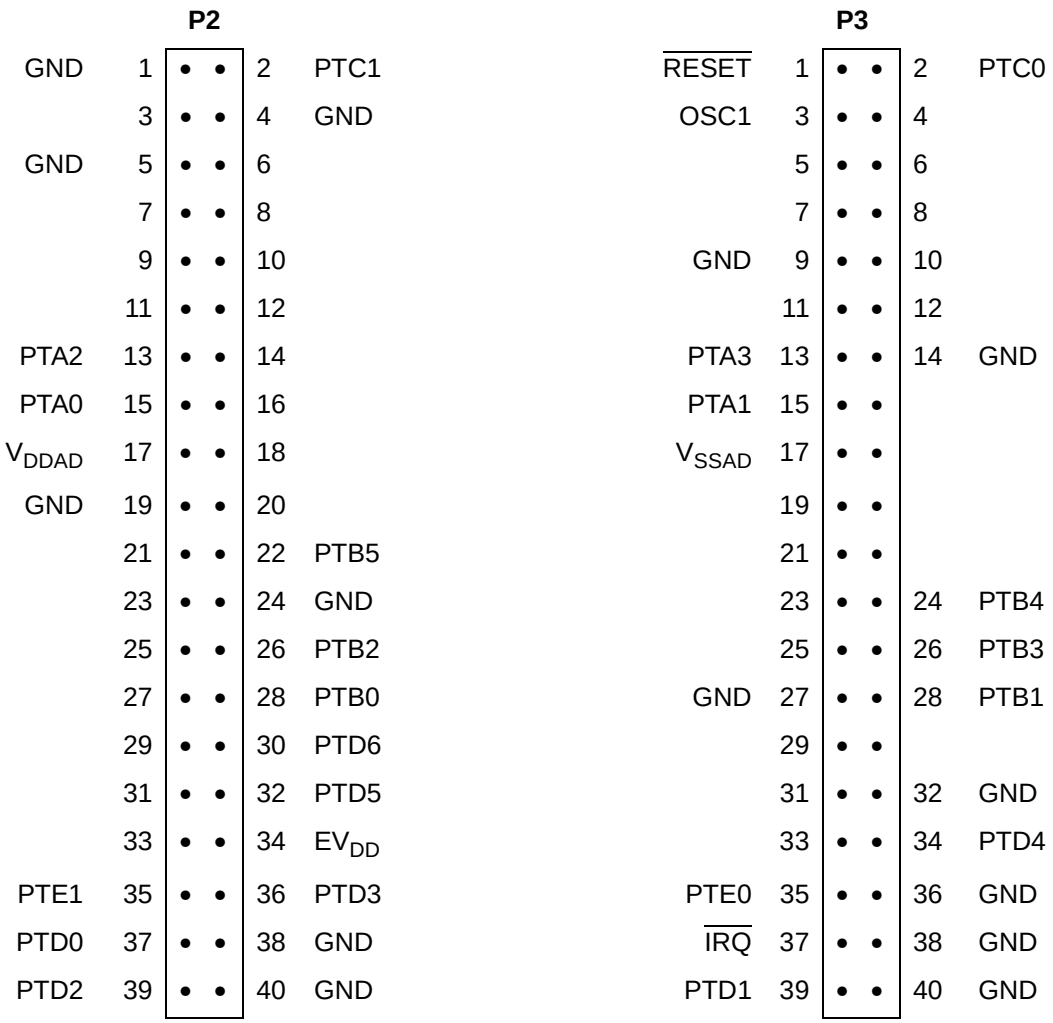

Figure 3-4. MC68HC908GR4/8 Pin Assignments

3.4.3 Pin assignments for MC68HC908GT16

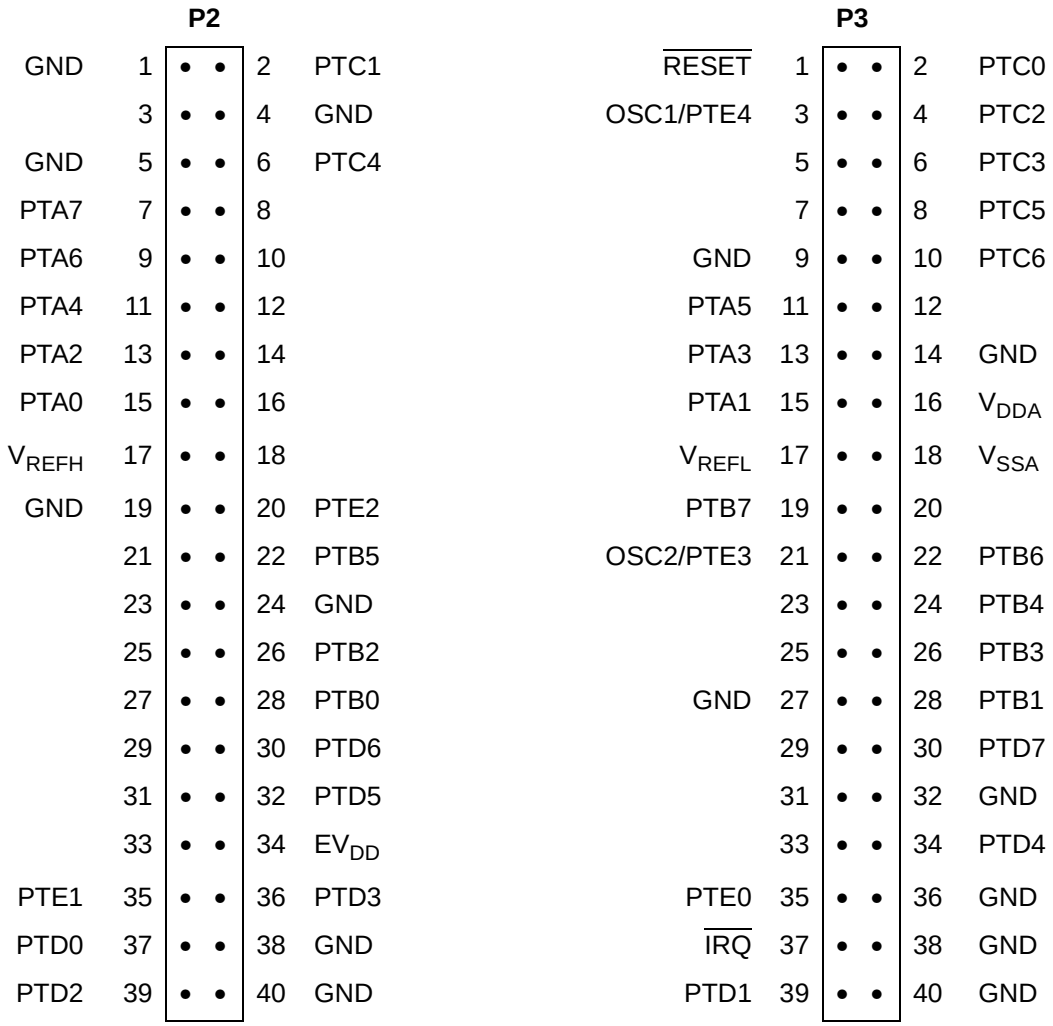

Figure 3-5. MC68HC908GT16 Pin Assignments

3.4.4 Pin assignments for MC68HC908JL3/JK3

.

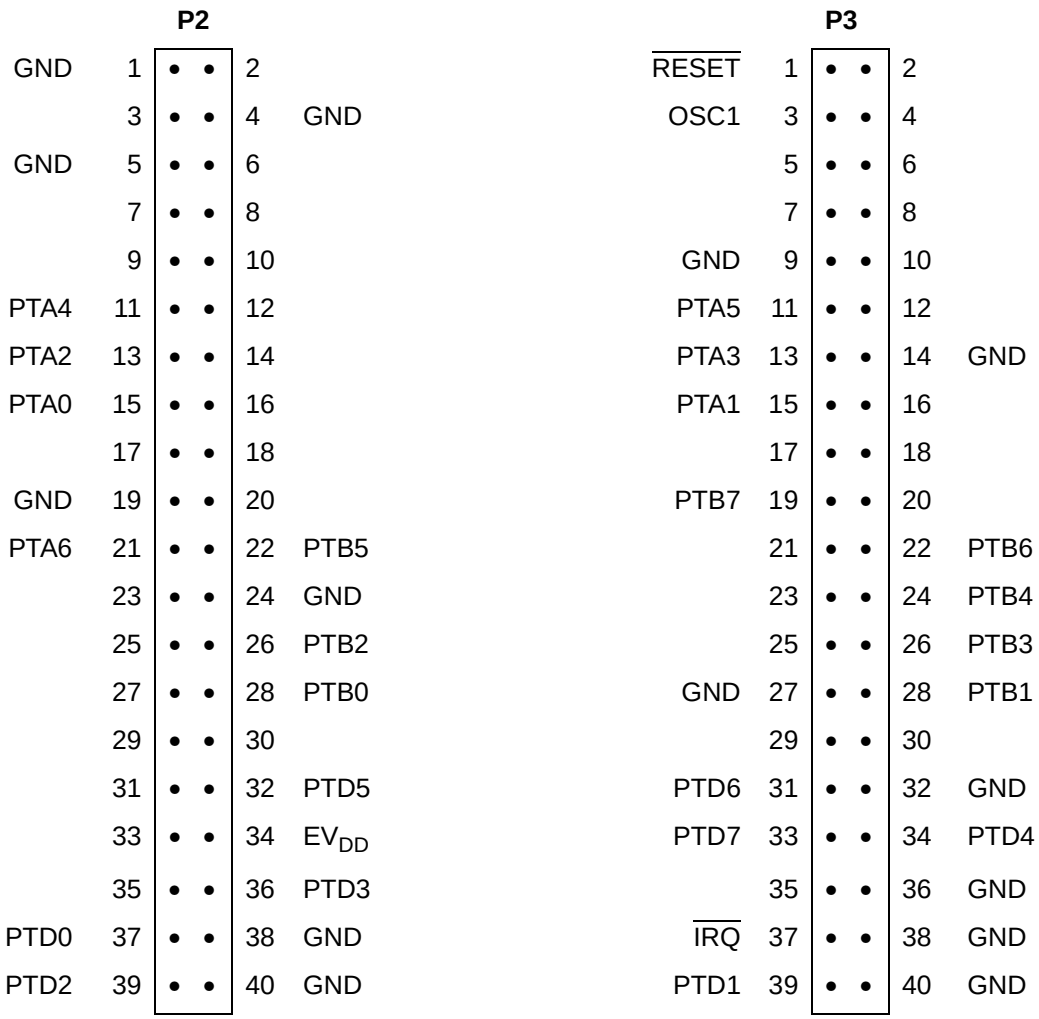

Figure 3-6. MC68HC908JL3/JK3 Pin Assignments

3.4.5 Pin assignments for MC68HC908KX2/8

.

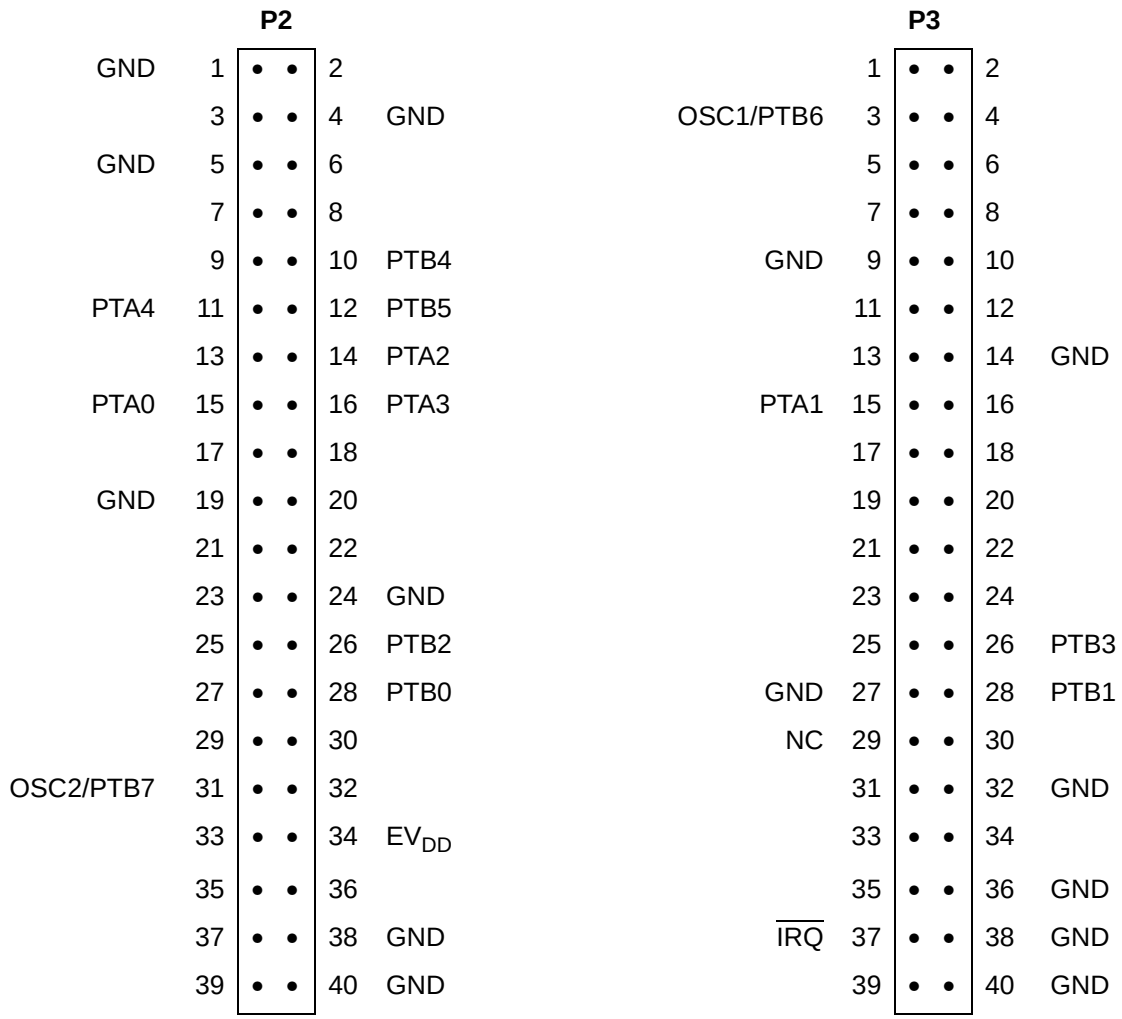

Figure 3-7. MC68HC908KX2/8 Pin Assignments

3.5 Target Cable Assembly

To connect the GPGTEM to a target system, a separately purchased target cable assembly is needed, plus the appropriate target head and target-head/adapter package.

Figure 3-8. shows how one end of the flex cable plugs into the GPGTEM module, and it also shows how the target head connects into the target system.

If the GPGTEM is installed in the MMDS station module, run the flex cable through the slit in the station-module enclosure.

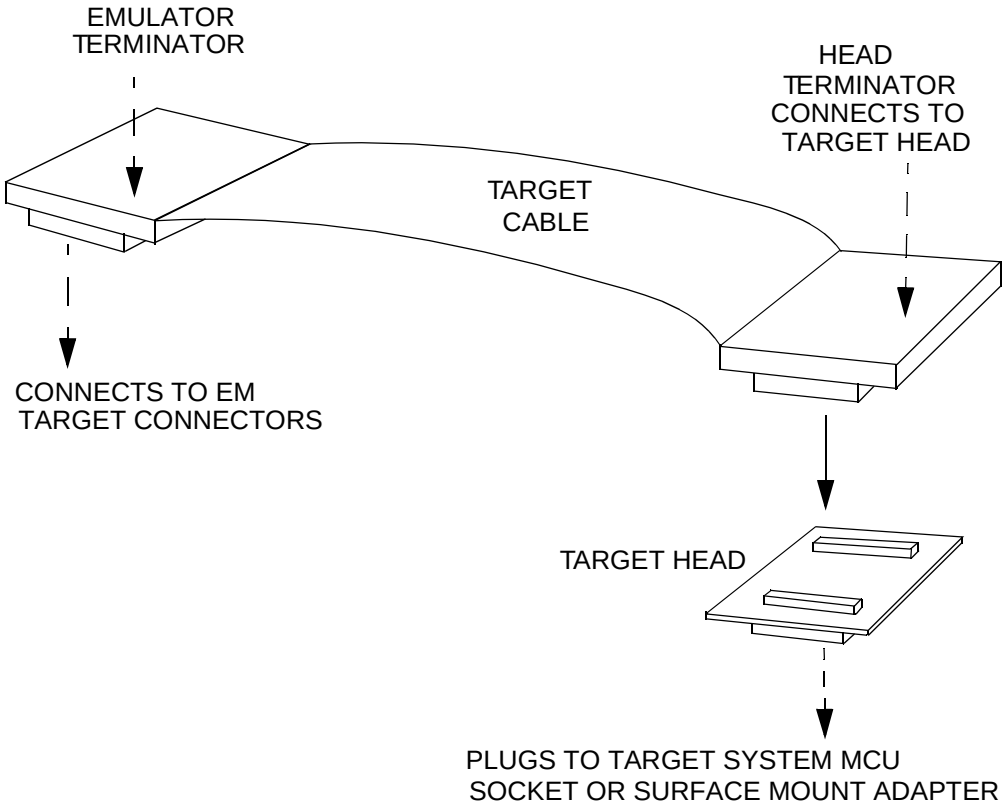

Figure 3-8. Target Cable Assembly

Connector Information

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