



*User's Manual*

*EML08LJK  
Version 0.2  
June 12, 2003*



# **M68EMIL08LJK**

## **Emulation Module**

**User's Manual**

## Important Notice to Users

While every effort has been made to ensure the accuracy of all information in this document, Motorola assumes no liability to any party for any loss or damage caused by errors or omissions or by statements of any kind in this document, its updates, supplements, or special editions, whether such errors are omissions or statements resulting from negligence, accident, or any other cause. Motorola further assumes no liability arising out of the application or use of any information, product, or system described herein: nor any liability for incidental or consequential damages arising from the use of this document. Motorola disclaims all warranties regarding the information contained herein, whether expressed, implied, or statutory, *including implied warranties of merchantability or fitness for a particular purpose*. Motorola makes no representation that the interconnection of products in the manner described herein will not infringe on existing or future patent rights, nor do the descriptions contained herein imply the granting or license to make, use or sell equipment constructed in accordance with this description.

## Trademarks

This document includes these trademarks:

Motorola and the Motorola logo are registered trademarks of Motorola, Inc.

Windows is a registered trademark of Microsoft Corporation in the U.S. and other countries.

Intel is a registered trademark of Intel Corporation.

Motorola, Inc., is an Equal Opportunity / Affirmative Action Employer.

For an electronic copy of this book, visit Motorola's web site at <http://e-www.motorola.com/>

© Motorola, Inc., 2003; All Rights Reserved



## Table of Contents

### M68EML08LJLK Quick Start Guide

1 - Set jumper W1 and W2 .....	9
2 - Install the emulation module into your development system .....	9
3 - Connect the emulation module to your target system .....	10
4 - Install the development software .....	10
5 - Copy personality files to your computer .....	10
6 - Connect MMDS or MMEVS to your computer and apply power	11

### Section 1. General Information

1.1	Introduction .....	13
1.2	Development Systems .....	13
1.2.1	Motorola Modular Development System (MMDS0508) .....	13
1.2.2	Motorola Modular Evaluation System (MMEVS0508) .....	14
1.3	System Requirements .....	15
1.4	EM Layout .....	15
1.5	Specifications .....	16
1.6	Target Cable Assemblies .....	17

### Section 2. Preparation and Operation

2.1	Introduction .....	19
2.2	Configuring Board Components .....	19
2.3	Limitations .....	20
2.4	Remaining System Installation .....	20

**Section 3. Support Information**

3.1	Introduction.....	23
3.2	Target Connectors J4 and J5.....	23
3.3	Logic Analyzer Connectors J3 and J7 .....	27
3.4	Inverted Clock Connector J11 .....	29
3.5	Board Factory Test Connector J9 .....	29
3.6	Optional crystal circuit using Y1 .....	29
3.7	Clock oscillator Y2.....	30
3.8	EM Board Socket Connectors P1 and P2 .....	30



## List of Figures

1-1	M68EML08LJLK Emulator Module . . . . .	16
1-2	Target Cable Assembly . . . . .	18
3-1	Target Connector (J4) Pin Assignments . . . . .	24
3-2	Target Connector (J5) Pin Assignments . . . . .	26
3-3	Logic Analyzer Connector J3 Pin Assignments . . . . .	27
3-4	Logic Analyzer Connector J7 Pin Assignments . . . . .	28
3-5	Connector J11 Pin Assignments . . . . .	29
3-6	EM Connector P1 Pin Assignments. . . . .	31
3-7	EM Connector P2 Pin Assignments. . . . .	33



## List of Figures



## List of Tables

1-1	Specifications . . . . .	16
1-2	M68EML08LJLK Target Cable and Head Assemblies . . . . .	17
2-1	Configuration Components . . . . .	19
3-1	Target Connector (J4) Signal Descriptions . . . . .	24
3-2	Target Connector (J5) Signal Descriptions . . . . .	26
3-3	Logic Analyzer Connector J3 Signal Descriptions . . . . .	28
3-4	Logic Analyzer Connector J7 Signal Descriptions . . . . .	28
3-5	Connector J11 Signal Descriptions . . . . .	29
3-6	EM Connector P1 Signal Descriptions . . . . .	32
3-7	EM Connector P2 Signal Descriptions . . . . .	34



## List of Tables



## M68EML08LJLK Quick Start Guide

Make sure that power is disconnected from your M68EML08LJLK Emulator Module and from your target system. Then follow these quick-start steps to make your M68EML08LJLK ready for use as quickly as possible.

### 1 - Set jumper W1 and W2

Jumper header W1 specifies the clock source for the MCU when you enable its external clock.

- Place the jumper between pins 3 and 4 (factory default) to specify the debugger-controlled oscillator from the platform board or place the jumper between pins 5 and 6 to specify the 4.9152-MHz oscillator Y2, which can be replaced with an oscillator of a different value, or place the jumper between pins 1 and 2 to specify the 32.768KHz crystal Y1.

Jumper header W2 specifies an LJ12 or LK24 MCU.

- Place the jumper between pins 2 and 3 (factory default) to specify an LK24 MCU or place the jumper between pins 1 and 2 to specify an LJ12 MCU.

Install the desired MCU, either an LJ12 or LK24 .

- Install the MCU you wish to emulate into the appropriate socket. If you wish to emulate the LJ12, you must install a QPF64 version of the LJ12 (supplied) into socket U5. If you wish to emulate an LK24, you must install a QFPF80 version of the LK24 (supplied) into the socket U6.

### 2 - Install the emulation module into your development system

To use the M68EML08LJLK in an MMDS0508 Motorola Modular Development System (MMDS) or MMEVS0508 Motorola Modular Evaluation System (MMEVS):

- Remove the access panel of the MMDS station-module enclosure.

- Insert the M68EML08LJLK through the access-panel opening.
- Fit together M68EML08LJLK connectors P1 and P2 (on the bottom of the board) to connectors P11 and P12, respectively, of the MMDS or MMEVS (P6 and P7 on some MMEVS boards) control board and snap the corners of the M68EML08LJLK onto the plastic standoffs.

### **3 - Connect the emulation module to your target system**

Use the supplied target flex cable, appropriate target head adapter, and surface mount adapter. Plug the appropriate end of the flex cable plugs into M68EML08LJLK connectors J4 and J5.

- If the M68EML08LJLK is in an MMDS station module, run the flex cable through the slit in the station-module enclosure, then replace the access panel.
- Plug the other end of the flex cable into the target head. Solder the appropriate surface mount adapter to your target if necessary. Then plug the target head into the surface mount adapter on your target system.

### **4 - Install the development software**

### **5 - Copy personality files to your computer**

The factory ships M68EML08LJLK MCU personality files on the documentation CD-ROM.

- If you're using the CodeWarrior IDE, find the installation directory and copy the personality files named 00C5CVxx.mem and 00C6CVxx.mem from the documentation CD-ROM to the . . . \prog\mem subdirectory of the CodeWarrior IDE main directory.
- If you're using the P&E debugger, copy these files to the installation directory that contains MMDS08.EXE or MMEVS08.EXE and rename them from 00C5CVxx.mem and 00C6CVxx.mem to 0045CVxx.mem and 0046CVxx.mem respectively.

## **6 - Connect MMDS or MMEVS to your computer and apply power**

This completes the quick start for your M68EML08LJLK.

When you have verified that cable connections between your development system and your computer are sound, you are ready to apply power and use your M68EML08LJLK.



# M68EML08LJK Quick Start Guide

## Section 1. General Information

### 1.1 Introduction

This user's manual explains connection and configuration of the Motorola M68EML08LJLK Emulator Module (M68EML08LJLK). The M68EML08LJLK makes possible emulation and debugging of target systems based on an MC68HC908LJ12 or MC68HC908LK24 microcontroller unit (MCU).

The M68EML08LJLK can be part of two development systems. This section describes those systems and explains the layout of the M68EML08LJLK

### 1.2 Development Systems

Your M68EML08LJLK can be part of two Motorola HC08 processor family development systems: the MMDS0508 Motorola Modular Development System (MMDS) or the MMEVS0508 Evaluation System (MMEVS). Refer to the specific development system user's manual for more information.

#### 1.2.1 Motorola Modular Development System (MMDS0508)

The MMDS is an emulator system that provides a bus state analyzer and real-time memory windows for designing and debugging a target system. A complete MMDS consists of:

- **a station module** — the metal MMDS enclosure, containing the platform board and the internal power supply. Most system cables connect to the MMDS station module.
- **an emulator module (EM)** — such as the M68EML08LJLK, a separately-purchased printed circuit board that enables system functionality for a specific set of MCUs. The EM fits into the station module through a removable panel in the enclosure top. The EM has connectors for a target cable and for cables to a logic analyzer. The cable runs to an optional target system through an aperture in the station-module enclosure, to connect directly to the emulator module.

- **two logic clip cable assemblies** — twisted-pair cables that connect the station module to your target system, a test fixture, an oscillator, or any other circuitry useful for evaluation or analysis. One end of each cable assembly has a molded connector, which fits into station-module pod A or pod B. Leads at the other end of each cable terminate in female probe tips. Ball clips come with the cable assemblies and may be attached to the female probe tips.
- **a 9-lead RS-232 serial cable** — the cable that connects the MMDS to the host computer RS-232 port.
- **system software** — development software, on CD-ROM.
- **MMDS0508 documentation** — an MMDS operations manual (MMDS0508OM/D) and the appropriate EM user's manual.

You select the MMDS baud rate: 1200, 2400, 4800, 9600, 19200, 38400, or 57600.

Substituting a different EM enables your MMDS to emulate target systems based on different MCUs or MCU families. (Your Motorola representative can explain all the EMs available.)

### 1.2.2 Motorola Modular Evaluation System (MMEVS0508)

An MMEVS is an economical tool for designing, debugging, and evaluating target systems. A complete MMEVS consists of:

- **a platform board (PFB)** — the bottom board, which supports the emulator module. The platform board has connectors for power and the terminal or host computer.
- **an emulator module (EM)** — such as the M68EML08LJLK, a separately purchased printed circuit board that enables system functionality for a specific set of MCUs. The EM fits onto the PFB. The EM has connectors for the target cable and for cables to a logic analyzer.
- **a 9-to-25-pin adapter** — a molded assembly that lets you connect the 9-pin cable to a 25-pin serial port.
- **a 9-lead RS-232 serial cable** — the cable that connects the station module to the host computer RS-232 port.
- **system software** — development software, on CD-ROM.

- **MMEVS0508 documentation** — an MMEVS operations manual (MMEVSOM/D) and the appropriate EM user's manual.

An MMEVS features automatic baud rate selection: 2400, 4800, 9600, 19200, 38400, or 57600.

Substituting a different EM enables your MMEVS to emulate target systems based on different MCUs or MCU families. (Your Motorola representative can explain all the EMs available.)

### 1.3 System Requirements

An IBM PC or compatible running Windows® 98, Windows 2000, or Windows NT® (version 4.0) with at least 32MB of RAM and an RS-232 serial port.

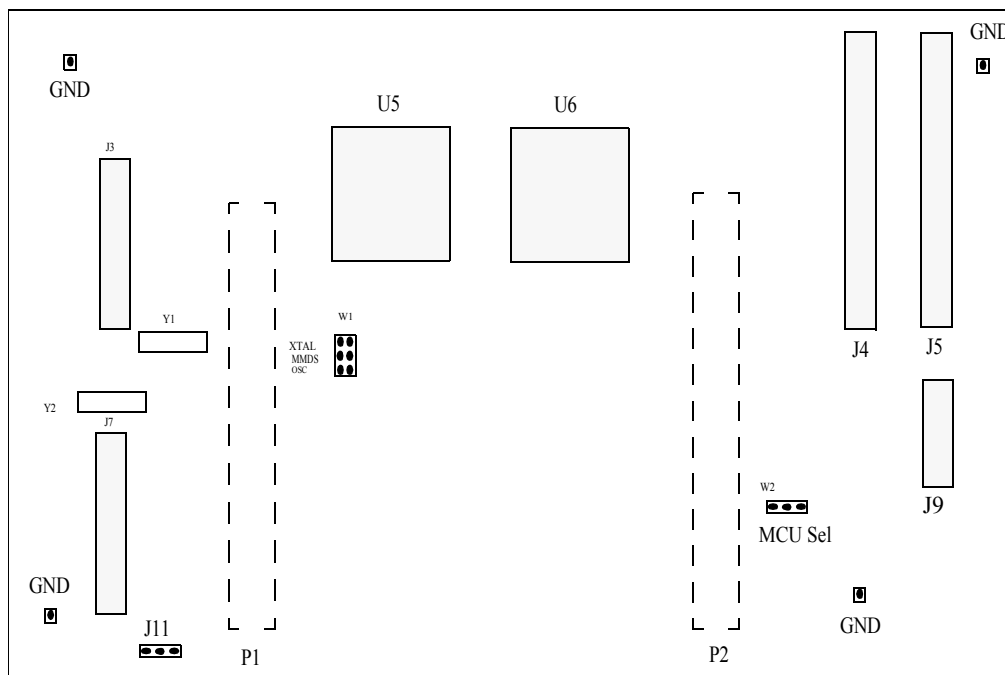
### 1.4 EM Layout

Figure 1-1 shows the layout of the M68EML08LJLK. Jumper header W1 specifies the clock signal source. Jumper W2 selects the MCU being emulated.

Target interface connectors J4 and J5 connect the M68EML08LJLK to a target system, via the included target cable assembly. If you use your M68EML08LJLK as part of an MMDS, run the target cable assembly through the slit in the station module enclosure.

Connectors J3 and J7 connect to a logic analyzer. Connector J11 is the source for an inverted clock signal. DIN connectors P1 and P2, on the bottom of the board connect the M68EML08LJLK to the platform board. The emulation MCU is at either location U5 (MC68HC908LJ12) or U6 (MC68HC908LK24).

Connector J9 is for factory test only.



**Figure 1-1 M68EML08LJK Emulator Module**

## 1.5 Specifications

Table 1-1 lists M68EML08LJK specifications

**Table 1-1 Specifications**

Characteristic	Specifications
Maximum Clock speed	8-MHz Bus at 5V (MC68HC908LJ12) 4-MHz Bus at 3.3V (MC68HC908LJ12) 8-MHz Bus at 4.5-5.5V (MC68HC908LK24) 4-MHz Bus at 2.7-3.3V (MC68HC908LK24) 2-MHz Bus) at 2.4-2.7V (MC68HC908LK24)
Target Voltage	Target Tracking if target is installed, or 5V Forced if no target. (+/-10%)
Temperature operating storage	-10° to +50° C -40° to +85° C
MCU Extension I/O	HCMOS Compatible at V <sub>mcu</sub> (5V or 3V)
Relative humidity	0 to 90% (noncondensing)
Power requirements	5VDC supplied from the MMDS or MMEVS



**Table 1-1 Specifications**

Characteristic	Specifications
Dimensions	5.5 X 8.0 X 0.75 inches (139.7 x 203.2 x 19.1 mm)

## 1.6 Target Cable Assemblies

To connect your M68EML08LJLK to a target system, you need the included target cable and adapters. See Figure 1-2.

The cable assembly for an 80-pin QFP package consists of: a flex cable, a target head adapter, a socket-saver and an 80-pin QFP surface mount adapter. The cable assembly for a 80-pin LQFP package consists of: a flex cable, a target head adapter, a socket-saver and an 80-pin LQFP surface mount adapter. The cable assembly for a 64-pin QFP package consists of: a flex cable, a target head adapter, and a 64-pin QFP surface mount adapter. The cable assembly for a 64-pin LQFP package consists of: a flex cable, a target head adapter, and a 64-pin LQFP surface mount adapter. The cable assembly for a 52-pin LQFP package consists of: a flex cable, a target head adapter, and a 52-pin LQFP surface mount adapter. One end of the target cable plugs onto M68EML08LJLK connectors J4 and J5. The other end of the flex cable plugs onto the target head adapter, which plugs onto the QFP or LQFP surface mount adapter. You should solder the QFP or LQFP surface mount adapter directly onto the target-system board in place of the MCU. The socket-saver goes between the target head adapter and surface mount adapter. If you use it, it will reduce wear on the target head adapter. After many insertions, you can replace the socket-saver without replacing the entire target head adapter.

Table 1-2 lists target cable and head part numbers appropriate for the M68EML08LJLK.

**Table 1-2 M68EML08LJLK Target Cable and Head Assemblies**

MCU Package	Flex Cable Part Number	Target Head Adapter Part Number	Surface Mount Adapter Part Number	Socket-Saver Part Number
80-pin QFP	M68CBL05E	M68TE08LJLK FQ80	M68TQP080SBM01	M68TQS080SBG1
80-pin LQFP	M68CBL05E	M68TE08LJLK PK80	M68TQP080SD1	M68TQS080SDG1
64-pin QFP	M68CBL05E	M68TE08LJLK FU64	M68TQP064SA1	M68TQS064SAG1
64-pin LQFP	M68CBL05E	M68TE08LJLK PB64	M68TQP064SD1	M68TQS064SDG1
52-pin LQFP	M68CBL05E	M68TE08LJLK FB52	M68TQP052SB1	M68TQS052SBG1

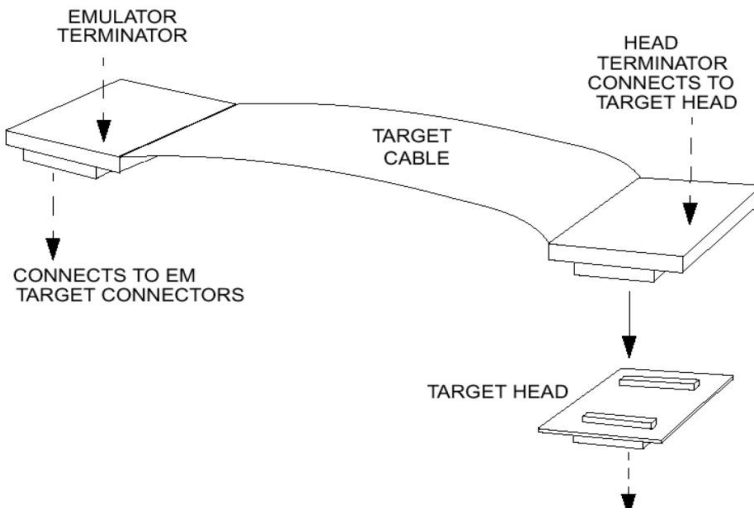


Figure 1-2 Target Cable Assembly

## Section 2. Preparation and Operation

### 2.1 Introduction

This section explains EML08LJLK preparation: how to set board jumpers and how to make system connections.

Note that you can reconfigure an EML08LJLK already installed in an MMDS0508 station module enclosure. To do so, switch off station-module power and target power, remove the panel, then follow the guidance of this section. Similarly, you can reconfigure an EML08LJLK already installed on the MMEVS platform board, provided that you disconnect platform-board power and target power.

**CAUTION: ESD Protection**

*Motorola development systems include open-construction printed circuit boards that contain static-sensitive components. These boards are subject to damage from electrostatic discharge (ESD). To prevent such damage, you must use static-safe work surfaces and grounding straps, as defined in ANSI/EOS/ESD S6.1 and ANSI/EOS/ESD S4.1. All handling of these boards must be in accordance with ANSI/EAI 625.*

### 2.2 Configuring Board Components

Table 2-1 is a summary of configuration settings.

**Table 2-1 Configuration Components**

Component	Position	Effect
Oscillator Select Header, W1  (Use only one jumper in this header.)	<p>The diagram shows a 6-pin header labeled W1. Pins 1, 2, 5, and 6 are shown as pairs of circular pins. A black jumper is placed across pins 1 and 2.</p>	<b>PFB:</b> Specifies the oscillator clock signal from the platform board (MMDS).  <b>Factory setting</b>
	<p>The diagram shows a 6-pin header labeled W1. Pins 1, 2, 5, and 6 are shown as pairs of circular pins. A black jumper is placed across pins 1 and 5.</p>	<b>EM:</b> Specifies the clock signal from the -megahertz oscillator on the EM board at Y2 (EM).

**Table 2-1 Configuration Components (Continued)**

Component	Position	Effect
		<b>XTAL:</b> Specifies the clock signal from a 32.768 crystal installed at Y1 (XTAL).
MCU Select Header, W2		<b>LK24:</b> Specifies emulation of an MC68HC908LK24. <b>Factory setting</b>
		<b>LJ12:</b> Specifies emulation of an MC68HC908LJ12.

## 2.3 Limitations

Limitations listed here apply to using your EML08LJLK versus using the actual MCU in your target system:

**Limitation 1 - Crystals:** You can use the crystal at location Y1 and associated components (refer to the schematic) to be a clock signal source. But each crystal has slightly different characteristics, and a crystal’s behavior can differ substantially in different circuits. Satisfactory performance as part of the EML08LJLK Y1 timing circuit does not guarantee that the same crystal will perform satisfactorily on a target board.

**Limitation 2 - OSC2:** The OSC2 pin function will not be available on the target cable. If you wish to use this signal on your target, you must make a connection between J11 and your target system.

**Limitation 3 - LVI Resets:** The emulator will not reset if the target voltage falls below the LVI thresholds.

## 2.4 Remaining System Installation

When you have configured jumper headers, you are ready to complete EML08LJLK installation:

- To install the EML08LJLK in an MMDS0508 station module, remove the panel from the station module top. Fit together EM connectors P1 and P2 (on the bottom of the board) and platform-board connectors P11 and P12, respectively. Snap the corners of the EM onto the plastic standoffs. Connect the target cable, if appropriate, then replace the panel.
- If your EML08LJLK already is installed in the station module, reconnect the target cable (if necessary). Replace the panel.
- To install the EML08LJLK on an MMEVS platform board, fit together EM connectors P1 and P2 (on the bottom of the board) and platform-board connectors P11 and P12 (P6 and P7 on some MMEVS boards), respectively. Snap the corners of the EM onto the plastic standoffs.
- *If you will use the P&E development system*, copy personality files 00C5CVxx.MEM and 00C6CVxx.MEM from the documentation CD-ROM to the installation directory that contains file MMDS08.EXE or MMEVS08.EXE. Then rename these files to 0045CVxx.MEM and 0046CVxx.MEM.
- *If you will use the CodeWarrior IDE development software*, copy personality files 00C5CVxx.MEM and 00C6CVxx.MEM from the documentation CD-ROM to the . . . \prog\mem subdirectory of the CodeWarrior IDE installation directory.

Additionally, if you must use CodeWarrior IDE development software, you will need to copy the EML08LJLK register files MCU0C5C.REG and MCU0C6C.REG from the documentation CD-ROM to the . . . \prog\reg subdirectory of the CodeWarrior IDE installation directory. The CodeWarrior IDE uses these files to implement optional functionality such as letting you view or modify register contents by name rather than by address. A register file is an ASCII text file, which you may customize. (The CodeWarrior IDE user's manual explains how to create and use such files.)

At this point, you are ready to make any remaining cable connections and apply power. For instructions, consult the MMDS or MMEVS operations manual.



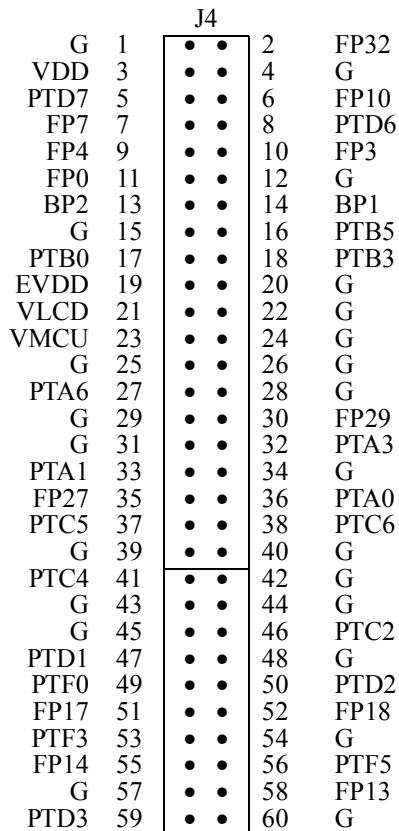
## Section 3. Support Information

### 3.1 Introduction

This section consists of connector pin assignments, connector signal descriptions, and other information that may be useful in your development activities.

### 3.2 Target Connectors J4 and J5

Connectors J4 and J5 are the M68EML08LJLK target connectors. Figure 3-1 and Table 3-1 give the pin assignments and signal descriptions for connector J4. Figure 3-2 and Table 3-2 give the pin assignments and signal descriptions for connector J5.



**Figure 3-1 Target Connector (J4) Pin Assignments**

**Table 3-1 Target Connector (J4) Signal Descriptions**

Pin	Label	Signal
1,4,12,15,20,22,24,25,26,28,29,31,34,39,40,42-45,48,54,57,60	G	GROUND
27,32,33,36	PTA0,PTA1,PTA3,PTA6	PORT A (lines 0,1,3,6) — General-purpose I/O lines controlled by software via data direction and data registers. (Other port A lines are available on connector J5.)
16-18	PB0,PTB3,PTB5	PORT B (lines 0,3,5) — General-purpose I/O lines controlled by software via data direction and data registers. (Other port B lines are available on connector J5.)
37,38,41,46	PTC2,PTC4,PTC5,PTC6,	PORT C (lines 2,4—6) — General-purpose I/O lines controlled by software via data direction and data registers. (Other port C lines are available on connector J5.)



**Table 3-1 Target Connector (J4) Signal Descriptions (Continued)**

Pin	Label	Signal
5,8,47,50,59	PTD1,PTD2, PTD3,PTD6, PTD7,	PORT D (lines 1-3,6,7) — General-purpose I/O lines controlled by software via data direction and data registers. (Other port D lines are available on connector J5.)
49,53,56	PTF0, PTF3,PTF5	PORT F (lines 0,3,5) — General-purpose I/O lines controlled by software via data direction and data registers. (Other port F lines are available on connector J5.)
2,6,7,9-11,30, 35,51,52,55,58	FP0,FP3,FP4, FP7,FP10, FP13,FP14, FP17,FP18, FP27,FP29, FP32	Front Plane (lines 0,3,4,7,10,13,14,17,18,27,29,32) — LCD driver lines controlled by data registers. (Other front plane lines are available on connector J5.)
13,14	BP1,BP2	Back Plane (lines 1,2) — LCD driver lines controlled by data registers. (Other back plane lines are available on connector J5.)
21	VLCD	LCD voltage supply
19	EVDD	EVDD sense voltage from target to control emulator mcu voltage.)
3	VDD	VDD - 5 volts, supplied only for test purposes - does not go to target.
23	VMCU	VMCU - variable, supplied only for test purposes - does not go to target.

		J5			
G	1	• •	2	FP31	
FP12	3	• •	4	G	
FP9	5	• •	6	FP11	
G	7	• •	8	FP8	
FP6	9	• •	10	FP5	
FP2	11	• •	12	FP1	
PTD4	13	• •	14	PTD5	
PTB4	15	• •	16	BP0	
PTB2	17	• •	18	G	
G	19	• •	20	PTB1	
G	21	• •	22	G	
G	23	• •	24	G	
PTB7	25	• •	26	G	
PTA7	27	• •	28	PTB6	
PTA5	29	• •	30	FP30	
PTA4	31	• •	32	G	
G	33	• •	34	PTA2	
G	35	• •	36	FP28	
G	37	• •	38	PTC7	
PTD0	39	• •	40	G	
TRESET	41	• •	42	G	
IRQ_B	43	• •	44	G	
PTC3	45	• •	46	G	
G	47	• •	48	PTC1	
G	49	• •	50	G	
PTF1	51	• •	52	PTC0	
FP16	53	• •	54	PTF2	
FP15	55	• •	56	PTF4	
G	57	• •	58	PTF6	
PTF7	59	• •	60	G	

**Figure 3-2 Target Connector (J5) Pin Assignments**

**Table 3-2 Target Connector (J5) Signal Descriptions**

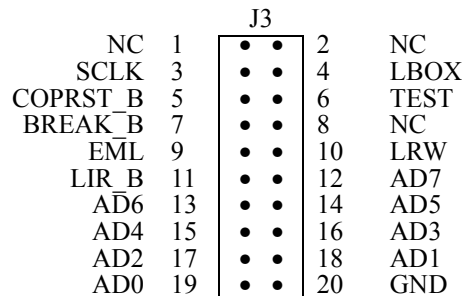
Pin	Label	Signal
1,4,7,18,19, 21-24,26,32,33,35,37,40,42,44,46, 47,49,50,57,60,	G	GROUND
27,29,31,34	PTA2,PTA4, PTA5,PTA7	PORT A (lines 0--7) — General-purpose I/O lines controlled by software via data direction and data registers. (Other port A lines are available on connector J4.)
15,17,20,25,28	PTB1,PTB4— PTB7	PORT B (lines 1,4—7) — General-purpose I/O lines controlled by software via data direction and data registers. (Other port B lines are available on connector J4.)
38,45,48,52	PTC0,PTC1, PTC3,PTC7	PORT C (lines 0,1,3,7)— General-purpose I/O lines controlled by software via data direction and data registers. (Other port C lines are available on connector J4.)

**Table 3-2 Target Connector (J5) Signal Descriptions (Continued)**

Pin	Label	Signal
1,4,7,18,19, 21-24,26,32,33,3 5,37,40,42,44,46, 47,49,50,57,60,	G	GROUND
13,14,39,	PTD0,PTD4, PTD5	PORT D (lines 0,4,5) —General-purpose I/O lines controlled by software via data direction and data registers. (Other port D lines are available on connector J4.)
51,54,56,58,59	PTF1,PTF2, PTF4,PTF6, PTF7,	PORT F (lines 1,2,4,6,7) — General-purpose I/O lines controlled by software via data direction and data registers.(Other port F lines are available on connector J4.)
2,3,5,6,8,9,10, 11,12,30,36,53, 55	FP1,FP2,FP5, FP6,FP8,FP9, FP11,FP12, FP15,FP16, FP28,FP30, FP31	Front Plane (lines 1,2,5,6,8,9,11,12,15,16,28,30,31) — LCD driver lines controlled by data registers. (Other front plane lines are available on connector J4)
16	BP0	Back Plane (line 0) — LCD driver lines controlled by data registers. (Other back plane lines are available on connector J4.)
41	T_RESET_B	Target reset
43	IRQ_B	TARGET INTERRUPT — Active-low input line for requesting a target interrupt.

### 3.3 Logic Analyzer Connectors J3 and J7

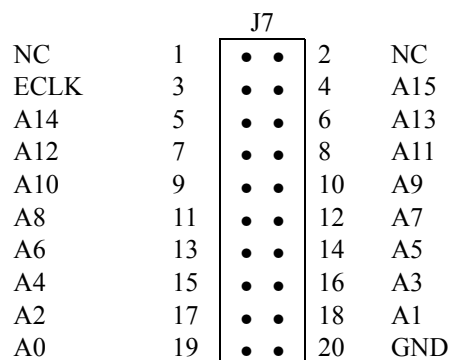
Connectors J3 and J7 are the M68EML08LJLK logic analyzer connectors. Figure 3-3 and Table 3-3 give pin assignments and signal descriptions for connector J3, which has pod 1 signals. Figure 3-4 and Table 3-4 give pin assignments and signal descriptions for connector J7, which has pod 2 signals.



**Figure 3-3 Logic Analyzer Connector J3 Pin Assignments**

**Table 3-3 Logic Analyzer Connector J3 Signal Descriptions**

Pin	Label	Signal
1, 2,	NC	No connection
3	SCLK	SYSTEM BUS CLOCK — Clock that matches the internal emulation MCU bus clock
4	LBOX	LAST BUS CYCLE — Output signal that the emulator asserts to indicate that the target system MCU is in the last bus cycle of an instruction.
5	RST_B	COP RESET — Active-low output signal indicating (1) the target driving its reset pin, or (2) the platform board driving a reset to the emulator module.
6,8	TEST	Test pins are used only during system development and factory test.
7	BREAK_B	Break
9	EMUX	MUXED CONTROL — Output from the emulation MCU that, during different phases of the clock, drives R/W, LIR_B, and LAST signals.
10	LRW	LATCHED READ/WRITE — Output signal from the target MCU. If high, the target MCU is reading. If low, the target MCU is writing.
11	LIR_B	LOAD INSTRUCTION REGISTER — Active-low output signal indicating that the target MCU is fetching an instruction.
12 — 19	AD7 — AD0	PFB DATA BUS (lines 7—0) — Outputs the data lines going to the platform board.
20	GND	GROUND



**Figure 3-4 Logic Analyzer Connector J7 Pin Assignments**

**Table 3-4 Logic Analyzer Connector J7 Signal Descriptions**

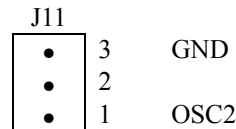
Pin	Label	Signal
1, 2	NC	No connection
3	ECLK	EM CLOCK — Output clock signal for the emulator module.

**Table 3-4 Logic Analyzer Connector J7 Signal Descriptions (Continued)**

Pin	Label	Signal
4 — 19	A15 — A0	LATCHED ADDRESS BUS (lines 15—0) — Output showing the address of the current bus cycle.
20	GND	GROUND

### 3.4 Inverted Clock Connector J11

Connector J11 is the source for an inverted clock signal. Figure 3-5 and Table 3-5 gives the pin assignments and signal descriptions for this connector. Because the OSC2 signal is not present on the target cable, you should connect this signal to your target system if you will use the OSC2 signal.



**Figure 3-5 Connector J11 Pin Assignments**

**Table 3-5 Connector J11 Signal Descriptions**

Pin	Label	Signal
3	GND	Ground
2		No connection
1	OSC2	INVERTED CLOCK OUTPUT — Provides the Inversion of the EMLCLK, which is the equal of the OSC2 output on the MCU..

### 3.5 Board Factory Test Connector J9

Factory tests use this connector. No user functions provided.

### 3.6 Optional crystal circuit using Y1

When you select the XTAL option on jumper W1 (jumper on pins 1-2), the clock signal generated by Y1 is supplied to the external inputs of the MCU. This circuit does not necessarily represent a crystal attached to the MCU.

### 3.7 Clock oscillator Y2

When you select the OSC option on jumper W1 (jumper on pins 3-4), the clock signal generated by Y2 is supplied to the external inputs of the MCU. You can

replace Y2 with another compatible clock oscillator to provide a different clock frequency (see schematic page 10).

### 3.8 EM Board Socket Connectors P1 and P2

Connectors P1 and P2 connect the M68EML08LJK to the platform board. Figure 3-6 and Table 3-6 give pin assignments and signal descriptions for connector P1. Figure 3-7 and Table 3-7 give pin assignments and signal descriptions for connector P2.

			P1					
A			B			C		
•	A1	LA[14]	•	B1	PFB_AD[7]	•	C1	GND
•	A2	LA[13]	•	B2	PFB_AD[6]	•	C2	GND
•	A3	LA[12]	•	B3	PFB_AD[5]	•	C3	GND
•	A4	LA[11]	•	B4	PFB_AD[4]	•	C4	GND
•	A5	LA[10]	•	B5	PFB_AD[3]	•	C5	GND
•	A6	LA[9]	•	B6	PFB_AD[2]	•	C6	GND
•	A7	LA[8]	•	B7	PFB_AD[1]	•	C7	GND
•	A8	LA[7]	•	B8	PFB_AD[0]	•	C8	GND
•	A9	LA[6]	•	B9	LIR_B	•	C9	GND
•	A10	LA[5]	•	B10	LRW	•	C10	GND
•	A11	LA[4]	•	B11	SCLK	•	C11	GND
•	A12	LA[3]	•	B12	T12CLK	•	C12	GND
•	A13	LA[2]	•	B13	NC	•	C13	GND
•	A14	LA[1]	•	B14	NC	•	C14	GND
•	A15	LA[0]	•	B15	NC	•	C15	GND
•	A16	LA[15]	•	B16	NC	•	C16	GND
•	A17	NC	•	B17	INTERNAL_B	•	C17	GND
•	A18	NC	•	B18	NC	•	C18	GND
•	A19	PFB_IRQ_B	•	B19	SWITCH_B	•	C19	GND
•	A20	CHRGPM	•	B20	NC	•	C20	GND
•	A21	NC	•	B21	NC	•	C21	GND
•	A22	NC	•	B22	NC	•	C22	GND
•	A23	PFB_OSC	•	B23	NC	•	C23	GND
•	A24	NC	•	B24	LBOX	•	C24	GND
•	A25	NC	•	B25	BREAK_B	•	C25	GND
•	A26	NC	•	B26	NC	•	C26	GND
•	A27	NC	•	B27	NC	•	C27	GND
•	A28	NC	•	B28	NC	•	C28	GND
•	A29	NC	•	B29	NC	•	C29	GND
•	A30	NC	•	B30	NC	•	C30	GND
•	A31	PFB_VCC	•	B31	PFB_VCC	•	C31	GND
•	A32	GND	•	B32	GND	•	C32	GND

**Figure 3-6 EM Connector P1 Pin Assignments**

**Table 3-6 EM Connector P1 Signal Descriptions**

Pin	Mnemonic	Signal
A1 — A16	LA[15] — LA[0] (not in exact order)	LATCHED ADDRESS BUS (lines 15—0) — Output lines for addressing external devices.
A17, A18, A21, A22, A24 — A30	NC	No connection
A19	PFB_IRQ_B	PFB INTERRUPT — Active-low signal that requests an interrupt of the platform board.
A20	CHRGPM	CHARGE PUMP — 12-volt signal (from the platform board).
A23	PFB_OSC	PFB OSCILLATOR — Oscillator clock signal from the platform board.
A31	PFB_VCC	PFB POWER — Operating voltage signal from the platform board.
A32	GND	GROUND
B1 — B8	PFB_AD[7] — PFB_AD[0]	PFB ADDRESS (lines 7—0) — Address of the current bus cycle.
B9	LIR_B	LOAD INSTRUCTION REGISTER — Active-low signal that the target MCU is fetching an instruction.
B10	LRW	LATCHED READ/WRITE — Input signal from the target MCU. If high, the target MCU is reading. If low, the target MCU is writing.
B11	SCLK	SERIAL CLOCK — Output clock signal to the platform board.
B12	T12CLK	T12 CLOCK — Matches the internal bus clock of the emulation MCU.
B13 — B16, B18, B20 — B23, B26 — B30	NC	No connection
B17	INTERNAL_B	INTERNAL RESOURCE — Active-low input signal indicating (1) that the current address is a target-MCU internal resource, or (2) that the EM board recreated the current address.
B19	SWITCH_B	SWITCH CONTROL — Active-low input signal that controls switches into the foreground map.
B24	LBOX	LAST BUS CYCLE — Input signal that the emulator asserts to indicate that the target system MCU is in the last bus cycle of an instruction.
B25	BREAK_B	BREAK REQUEST — Active-low output signal that requests a switch to background logic.
B31	PFB_VCC	PFB POWER — Operating voltage signal from the platform board.
B32	GND	GROUND
C1 — C32	GND	GROUND



			P2					
A			B			C		
•	A1	GND	•	B1	GND	•	C1	GND
•	A2	GND	•	B2	VCC	•	C2	VCC
•	A3	GND	•	B3	PTC[0]	•	C3	PTA[0]
•	A4	GND	•	B4	PTC[1]	•	C4	PTA[1]
•	A5	GND	•	B5	PTC[2]	•	C5	PTA[2]
•	A6	GND	•	B6	PTC[3]	•	C6	PTA[3]
•	A7	GND	•	B7	PTC[4]	•	C7	PTA[4]
•	A8	GND	•	B8	NC	•	C8	PTA[5]
•	A9	GND	•	B9	NC	•	C9	PTA[6]
•	A10	GND	•	B10	NC	•	C10	NC
•	A11	GND	•	B11	LOCKOUT_B	•	C11	PTB[7]
•	A12	GND	•	B12	T_RESET_5V_B	•	C12	PTB[6]
•	A13	GND	•	B13	NC	•	C13	PTB[5]
•	A14	GND	•	B14	PORTS_B	•	C14	PTB[4]
•	A15	GND	•	B15	NC	•	C15	PTB[3]
•	A16	GND	•	B16	PFB_RST_B	•	C16	PTB[2]
•	A17	GND	•	B17	COP_RST_B	•	C17	PTB[1]
•	A18	GND	•	B18	NC	•	C18	PTB[0]
•	A19	GND	•	B19	NC	•	C19	ID9
•	A20	GND	•	B20	NC	•	C20	ID8
•	A21	GND	•	B21	NC	•	C21	ID7
•	A22	GND	•	B22	NC	•	C22	ID6
•	A23	GND	•	B23	NC	•	C23	NC
•	A24	GND	•	B24	NC	•	C24	NC
•	A25	GND	•	B25	NC	•	C25	ID3
•	A26	GND	•	B26	NC	•	C26	ID2
•	A27	GND	•	B27	NC	•	C27	MCU_ID1
•	A28	GND	•	B28	VPRU	•	C28	MCU_ID0
•	A29	GND	•	B29	NC	•	C29	NC
•	A30	GND	•	B30	EVDD	•	C30	DAVINCI
•	A31	GND	•	B31	PFB_VCC	•	C31	PFB_VCC
•	A32	GND	•	B32	GND	•	C32	GND

**Figure 3-7 EM Connector P2 Pin Assignments**

**Table 3-7 EM Connector P2 Signal Descriptions**

Pin	Mnemonic	Signal
A1 — A32	GND	GROUND
B1, B32	GND	GROUND
B2	VCC	POWER — Operating voltage.
B3 — B7	PTC[0] — PTC[4]	PORT C (lines 0—4) — General-purpose I/O lines controlled by software via data direction and data registers.
B8 — B10, B13, B15, B18 — B27, 29	NC	No connection
B11	LOCKOUT_B	Used by the platform board to block the IRQ_B signal during reset recovery.
B12	T_RESET_5V_B	Target reset used to sense and drive resets to and from the target.
B14	PORTS_B	Indicates a port-related register access, which is routed to the PRU on the platform board.
B16	PFB_RST_B	PFB RESET — Active-low signal that requests a reset of the platform board.
B17	COP_RST_B	COP RESET — Active-low signal that resets the EM board.
B28	VPRU	Emulation MCU voltage used by the port replacement unit on the platform board.
B31	PFB_VCC	PFB POWER — Operating voltage signal from the platform board.
C1, C32	GND	GROUND
C2	VCC	POWER — Operating voltage.
C3 — C9	PTA[0] — PTA[7]	PORT A (lines 0—7) — General-purpose I/O lines controlled by software via data direction and data registers.
C10, C23, C24, C29	NC	No connection
C11 — C18	PTB[7] — PTB[0]	PORT B (lines 0—7) — General-purpose I/O lines controlled by software via data direction and data registers.
C19 — C22, C25 — C28	ID9 — ID6, ID3, ID2, MCU_ID1, MCU_ID0	MCU identification signals used by the platform board to detect which EM board is inserted.
C30	DAVINCI	Used to indicate HC05 or HC08 EM boards.
C31	PFB_VCC	PFB POWER — Operating voltage signal from the platform board.



**HOW TO REACH US:**

**World Wide Web Address**

**Motorola:** <http://www.motorola.com/General/index.html>

Information in this document is provided solely to enable system and software implementers to use Motorola products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part.



Motorola and the Stylized M Logo are registered in the U.S. Patent and Trademark Office. digital dna is a trademark of Motorola, Inc. All other product or service names are the property of their respective owners. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

© Motorola, Inc. 2003