M68MPB332UM/D
REV 1

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Freescale Semiconductor, Inc.

M68MPB332

MCU PERSONALITY BOARD

USER'S MANUAL

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CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides general information, hardware preparation, installation instructions, a quick start guide, and support information for the M68MPB332 MCU Personality Board (MPB). The MPB is one component of Motorola's modular approach to MC68332 Microcontroller Unit-based product development. This modular approach lets you easily configure our development systems to fit your requirements.

The MPB may be used in either the MMDS1632 Motorola Modular Development System (MMDS) or the modular evaluation board (MEVB). The MEVB consists of the M68MPFB Modular Platform Board (MPFB) and an MPB. Alternately, you may install the MPB directly in your target system if the target system includes a modular active probe interconnect (MAPI) interface. The MCU device on the MPB defines which MCU is emulated/evaluated by the MMDS or evaluated by the MEVB. Both systems are invaluable tools for designing, debugging, and evaluating MCU operation of the M68HC12, M68HC16, and M68300 MCU families. By providing the essential MCU timing and I/O circuitry, these systems simplify user evaluation of prototype hardware/software products.

The MPB includes:

- M68MPB332 MCU Personality Board (MPB)
- Plastic overlay for use with the MEVB – pin outs for the logic analyzer connectors on the MPFB (specifically for the MC68332 MCU)
- Documentation (this manual)

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1.2 SPECIFICATIONS

Table 1-1 lists MPB specifications.

Table 1-1. MPB Specifications

Characteristic	Specifications
On-Board Clock	Case style: 14- or 8-pin hybrid crystal clock oscillator (frequency as required by MCU).
External Clock	32 kHz – 16.78 MHz (or maximum MCU allows).
MCU I/O ports	HCMOS compatible
Temperature Operating Storage	 0° to +40° C -40° to +85° C
Relative humidity	0 to 90% (non-condensing)
Power requirements	+5Vdc ± 5% @ 500 mA (max.)
Dimensions MCU Personality Board	 3.25 x 3.25 in. (82.6 x 82.6 mm)

1.3 EQUIPMENT REQUIRED

The external requirements for MPB operation are either an MPFB or MMDS system. For MMDS operation requirements, see the MMDS1632 Motorola Modular Development System User's Manual,MMDS1632UM/D. For operation requirements for the MEVB, see this manual and the M68MPFB1632 Modular Platform Board User's Manual,M68MPFB1632UM/D.

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CHAPTER 2
HARDWARE PREPARATION AND INSTALLATION

2.1 INTRODUCTION

This chapter provides unpacking instructions, hardware preparation information, and installation instructions for the MPB.

When you unpack the MPB from its shipping carton, verify that all items are in good condition. Save packing material for storing and shipping the MPB.

NOTE

Should the MPB arrive damaged, save all packing material, and contact the carrier's agent.

2.2 HARDWARE PREPARATION

This portion of the manual explains how to prepare the MPB before use, as well as how to configure the MPB for system operation. This section also explains MPB installation in the MMDS and MEVB.

The MPB has been factory tested and is shipped with installed jumpers. A jumper installed on a jumper header provides a connection between two points in the MPB circuit. The MPB has four jumper headers (for which Table 2-1 is a quick reference guide). You may re-configured these jumper headers to customize MPB functionality. The following paragraphs explain each jumper header function. There is also an insertion point (E1) for connecting an external ground. Figure 2-1 shows the location of the MPB jumper headers and the insertion point.

NOTE

Verify that all socketed parts are seated in their sockets.

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CAUTION

Depending on your application, it may be necessary to cut the W2 wiring trace short (cut-trace short). Be careful not to cut adjacent PCB traces, nor cut too deep into the multi-layer circuit board.

If the cut-trace short on a jumper header is already cut, you can return the MPB to its default setting by installing a user-supplied fabricated jumper.

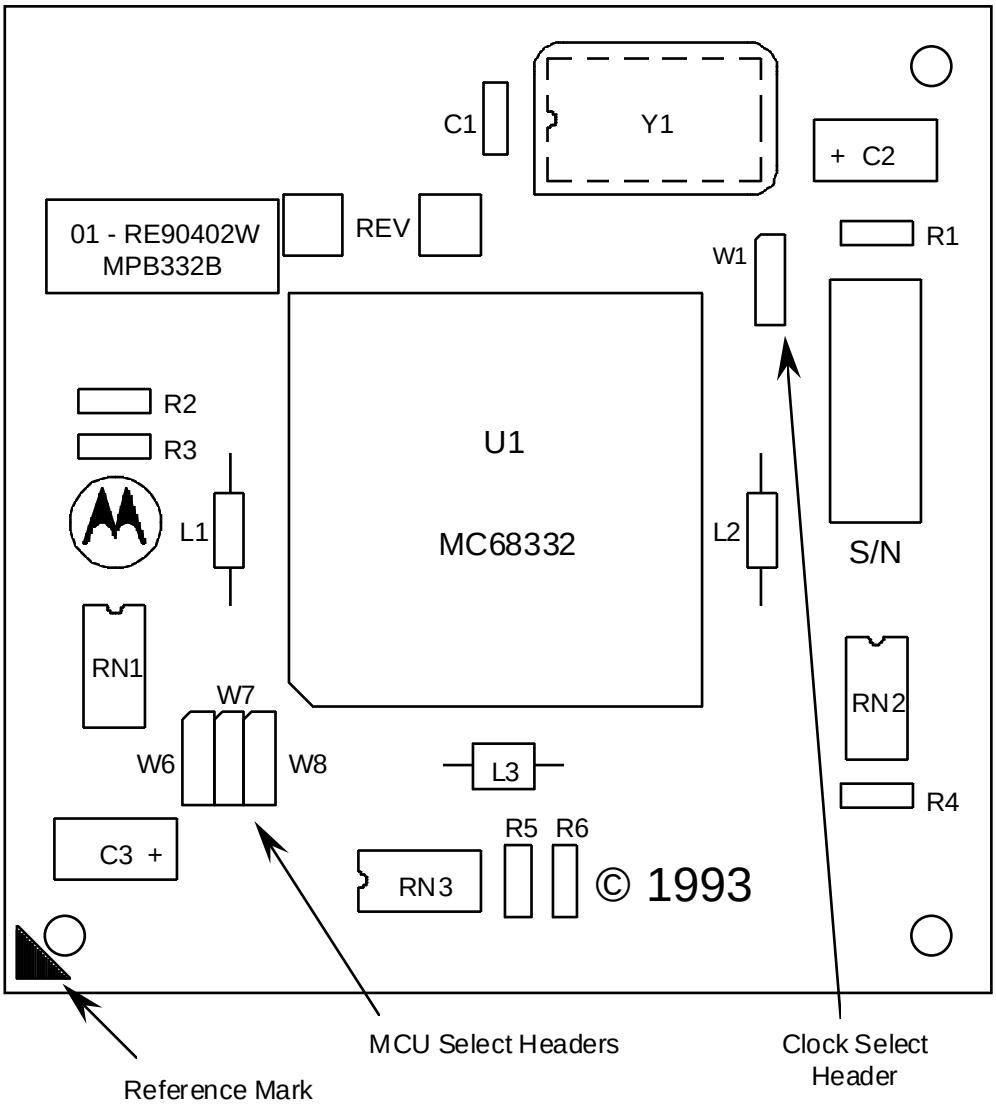

Figure 2-1. MPB Parts Location Diagram (top view)

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Table 2-1. MPB Jumper Header Descriptions

Jumper Header	Type	Description
W1		Jumper between pins 1 and 2 (factory default); selects the MPB on-board crystal clock source. Jumper between pins 2 and 3; selects an external clock source to be the MCU EXTAL input signal.
W6 W7 W8		Jumper headers W6, W7, and W8 configure the MPB for use with an MCU; either an MC68331, MC68332, or MC68335. To use an MC68332 MCU set the jumper headers: W6 pins 2 and 3, W7 pins 1 and 2, and W8 pins 2 and 3.

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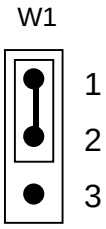
2.2.1 Clock Select Header (W1)

Jumper header W1 connects the MCU external clock (EXTAL) pin to either an on-board or external (target-system) clock source. The drawing below shows the factory configuration: a fabricated jumper on pins 1 and 2. This configuration selects the MPB on-board clock source; crystal oscillator in the Y1 socket. (This crystal provides for operation at the maximum rate the MCU allows via the internal phase-locked loop or direct clock input.)

If you install the MPB in the active probe or directly on a target system, and use the target system clock as the MPB clock, move the fabricated jumper to W1 pins 2 and 3. This connects the MCU EXTAL pin to the MAPI bus input pin. The frequency of the external clock signal can be from 32 kHz to 16.78 MHz (or to the maximum the MCU allows).



NOTE

You cannot drive the MPB clock circuit from an external source (target system) with a discrete crystal. If you use a target system clock source to drive the MPB clock circuit, always use a logic-driven clock such as a hybrid oscillator.

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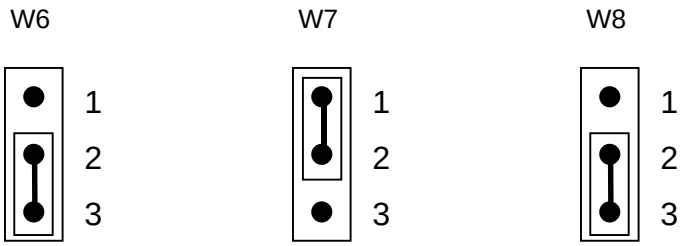
2.2.2 MCU Select Headers (W6, W7, W8)

Jumper headers W6, W7, and W8 select the MCU type supported by the MPB; either MC68331, MC68332, or MC68335. The drawing below shows the factory configuration: fabricated jumpers on W6 pins 2 and 3, W7 pins 1 and 2, and W8 pins 2 and 3. This configuration selects the MC68332 MCU. To use an MC68331 or MC68335 MCU refer to the appropriate MPB user's manual.



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2.3 MEVB CONFIGURATION

The MEVB contains:

- MPB – MCU-device-specific board that defines the MCU to be evaluated.
- M68MPFB Modular Platform Board (MPFB) – which provides the interface connections to the host computer, logic analyzer connections, and the platform for installing the MPB. For more information about the MPFB and MEVB system connections refer to the M68MPFB Modular Platform Board User's Manual, M68MPFBUM/D. Chapter 3 contains information to help you get started using your MEVB.

CAUTION

Turn OFF MPFB power when installing the MPB on the MPFB or removing the MPB from the MPFB. Sudden power surges could damage MEVB integrated circuits.

To install the MPB on the MPFB (refer to Figure 2-2):

1. Inspect all connectors for bent or damaged pins.
2. Align the MPB reference mark with the MPFB reference mark.
3. Rotate the MPB until the four MAPI bus connectors on its bottom mate with the MAPI bus connectors on the top of the MPFB. (There is only one way to connect the MPB and the MPFB.)
4. Firmly press the MPB onto the MPFB.

CAUTION

Support the bottom side of MPFB when installing the MPB on the MPFB. Excessive flexing of the MPFB could damage the printed circuit.

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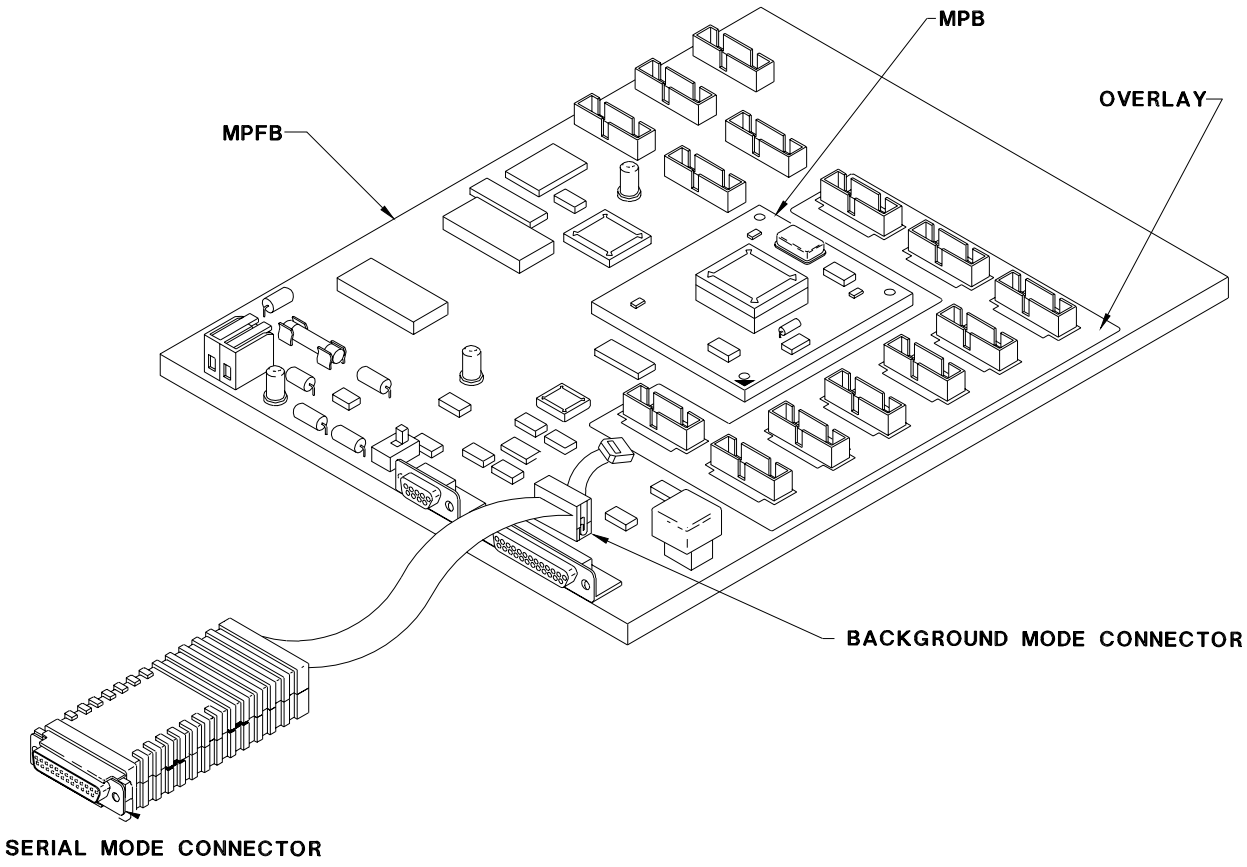

Figure 2-2. MPB – MPFB Interconnection (with SDI Interface)

After you have installed the MPB, install the plastic overlay on the MPFB: place the overlay over logic analyzer connectors J12 through J20 and press down. Holes in the overlay slide down over plastic clips on the MPFB. These clips hold the overlay in place.

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2.4 ACTIVE PROBE CONFIGURATION

The M68MMDS1632 Motorola Modular Development System (MMDS) consists of the station module and an active probe. The active probe consists of a three board set, two cables, and a box:

- MPB – MCU-device-specific board that defines the MCU to be evaluated.
- Target Control Board (TCB) – the interface between the MPB, target system, and the station module. The TCB is supplied with the MMDS. For more information about the TCB refer to the M68MMDS1632 Motorola Modular Development System User's Manual, MMDS1632UM/D.
- Package Personality Board (PPB) – the board that connects the active probe to the target system. The PPB must be purchased separately. For more information about the PPB refer to the appropriate user's manual.
- Active probe cables (2) – the interface between the active probe and the station module. 01-RE90340W01 REV 0 and 01-RE90341W01 REV 0 are printed on the active probe cables. The active probe cables come with the MMDS. For more information about the active probe cables refer to the M68MMDS1632 Motorola Modular Development System User's Manual, MMDS1632UM/D.
- Active probe box – the protective enclosure for the TCB.

CAUTION

Turn off MMDS and target system power when installing or removing MMDS components. Sudden power surges could damage MMDS and target system integrated circuits.

To configure an active probe:

1. Inspect all connectors for bent or damaged pins.
2. Rotate the MPB until the four MAPI bus connectors on its bottom mate with the MAPI bus connectors on the top of the TCB. (There is only one way to connect the MPB and the TCB.) Firmly press the MPB and the TCB together.
3. Rotate the PPB until the four MAPI bus connectors on its top mate with the MAPI bus connectors on the bottom of the TCB. (There is only one way to connect the PPB and the TCB.) Firmly press the PPB and the TCB together.

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4. Connect one end of the 01-RE90341W01 REV 0 active probe cable to connector P6 on the MMDS control board; connect the other end to connector J6 on the TCB. Connect one end of the 01-RE90340W01 REV 0 active probe cable to connector P5 on the MMDS control board; connect the other end to connector J5 on the TCB. Secure the connector clamps on TCB connectors J5 and J6.

The active probe is now ready to connect to the target system (refer to the PPB configuration guide for information on connecting the active probe to the target system.)

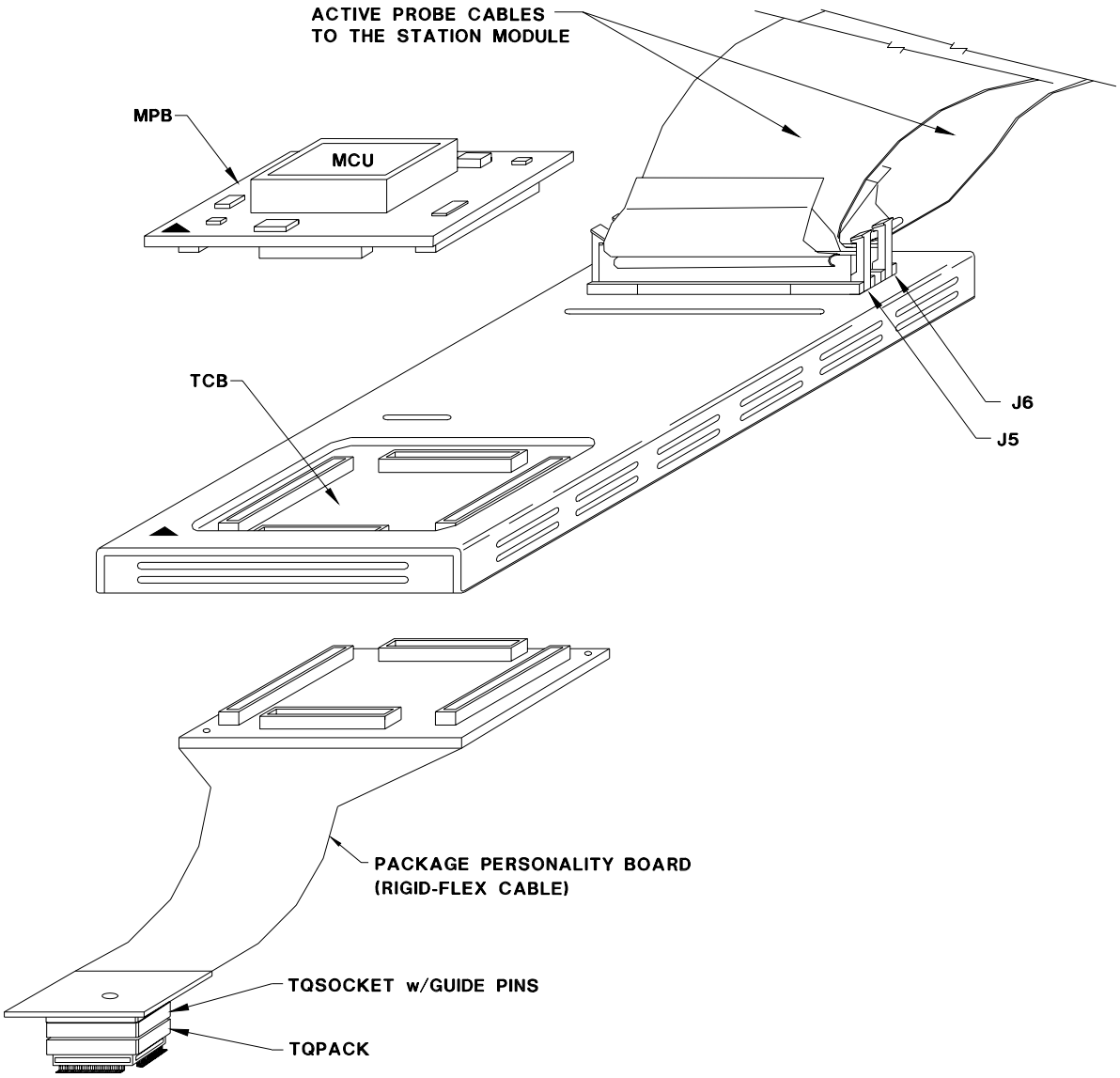

Figure 2-3. Active Probe Interconnection (with Active Probe Box)

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CHAPTER 3
MEVB QUICK START GUIDE

3.1 INTRODUCTION

This quick start guide is intended for the user who may not be familiar with Motorola's development tools. This chapter explains the MEVB hardware and software set up for M68MEVB332 operation. Hardware set up consists of configuring the MPB and MPFB jumper headers; software set up consists of installing and running the appropriate macro script file within the debugger.

For the purpose of this quick start guide the MPB jumper headers should be configured in their default positions. Chapter 2 of this manual contains the default jumper header settings for the MPB.

3.2 CONFIGURING THE MPFB

The MPFB includes jumper-selectable options such as chip select usage, memory type selection and memory size selection for the pseudo ROM sockets, and reset data control.

3.2.1 MPFB Memory Devices

Pseudo ROM refers to memory locations U2 & U4. The two pseudo ROM sockets are generic memory sockets that accept a variety of RAM, EPROM, or EEPROM devices. The pseudo ROM sockets, as shipped from the factory, contain two 32K x 8 RAM devices. These memories are 28-pin package devices.

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3.2.2 MPFB Jumper Headers

Configure your MPFB jumper headers per the instructions in Table 3-1. Table 3-1 contains information exclusively intended for quick start and ignores the other jumper headers.

Table 3-1. MPFB Quick Start Jumper Header Configuration

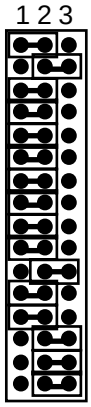
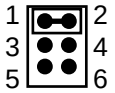
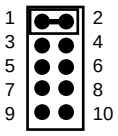
Jumper Header	Type	Description
W2		Install a jumper on pins 1 and 2 to configure pin 1 of the memory devices in the pseudo ROM sockets (U2 & U4) as a standard address line.
W3		Install a jumper on pins 1 and 2 to indicate that the memory devices in the pseudo ROM sockets (U2 & U4) have 28 pins.
W4		Install a jumper on pins 1 and 2 to set the pseudo ROM port size (memory data width) as word.
W5		Install a jumper on pins 1 and 2 to disable the PRU.
W6		W6 selects the MCU operation mode. Each 3-pin jumper header set corresponds to an MCU data line. While the reset pin is low, the reset data values are driven on the data bus (D0 – D15). (The MEVB reset data circuit is open drain; a high state is provided via a pull-up resistor.) Each reset data line may be set high (H) or low (L). Consult the appropriate MCU user's manual, data book, or technical summary for reset data information. The default setting configures the MC68332 MCU as 16-bit, expanded mode with these functions: • CSBOOT = 16-bit port • Chip select active
W10		Install a jumper on pins 1 and 2 to indicate that RAM is installed in the pseudo ROM sockets (U2 & U4).
W12		Install a jumper on pins 3 and 4 to indicate that the two devices installed in the pseudo ROM sockets (U2 & U4) are 32K x 8.

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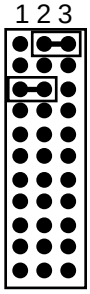
Table 3-1. MPFB Quick Start Jumper Header Configuration (continued)

Jumper Header	Type	Description
W14	1 2 3 	Jumper header W14 selects the MCU signal for the memory devices in the fast RAM sockets (U9 & U10) and pseudo ROM sockets (U2 & U4). Pins 1 and 2 select the MCU chip select for the memory devices in the fast RAM sockets. Pins 2 and 3 of jumper header W14 select the chip select for the memory devices in the pseudo ROM sockets. Jumper installed on CSBOOT pins 2 and 3 (factory default); use CSBOOT as the memory device chip enable for memory devices in the pseudo ROM sockets.
W16	1 2	No jumper installed; the MCU MODCLK signal is pulled high (logic 1) via a resistor during reset.
W17	1 2	No jumper installed; the BERR signal is pulled high (logic 1) via a resistor during reset.
W18	1 2 3	Install a jumper on pins 1 and 2 for unrestricted writes to the memory devices in the pseudo ROM sockets (U2 & U4).
W19	1 2 3	Install a jumper on pins 1 and 2 to ground the A19 signal to the MPFB memory arrays.
W22	1 2 3	Install a jumper on pins 1 and 2 to select the evaluation MCU (on the MPB) as an M68300 MCU device.

3.3 MEVB INSTALLATION INSTRUCTIONS

MEVB installation requires a user-supplied power supply and host computer. The host computer must have a parallel port and must run MS-DOS, as required by ICD32. The following paragraphs explain MPFB connections. Refer to Chapter 2 for instructions to connect the MPB and MPFB.

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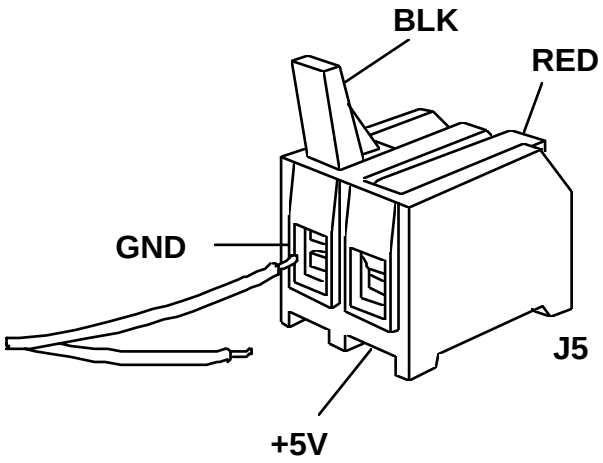
3.3.1 Power Supply – MPFB Connection

Use MPFB connector J5 to connect a user-supplied power supply to the MEVB. Contact 1 is ground; black lever. Contact 2 is VDD (+5 volts); red lever. Use 20 or 22 AWG wire for power connections. For each wire, trim back the insulation 1/4 in. (.635 cm), lift the appropriate lever of J5 to release tension on the contacts, then insert the bare wire into J5 and close the lever. The MEVB requires a +5Vdc @ 1.0 amp power supply for operation. A 1.5 amp fuse is installed on the MPFB +5Vdc power supply input line.



CAUTIONS

Do not use wire larger than 20 AWG in connector J5. Such wire could damage the connector.

Turn off MEVB power when installing or removing the MPB from the MPFB. Sudden power surges could damage MEVB integrated circuits.

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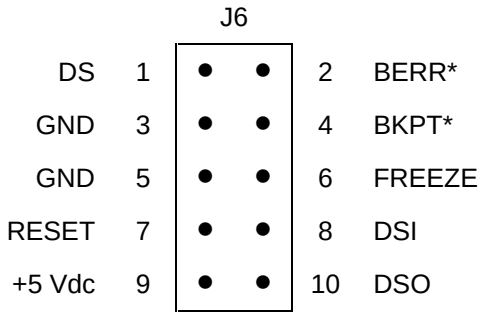
3.3.2 Personal Computer – BDM Connection

Personal computer communication with the MEVB requires background debug mode (BDM) hardware. Connect your BDM hardware between your computer's I/O port and the BDM header on the MPFB (MPFB connector J6). The drawing below shows signal assignments for connector J6. For additional information about your BDM software/hardware, including debugging and assembly information, see the appropriate user's manual.



3.4 SOFTWARE INSTALLATION AND MCU INITIALIZATION

After you have set up the MEVB hardware you must install the software on your computer. Follow the installation procedure in the appropriate software operations manual.

The MCU must be initialized before the MEVB will function. The following is one possible initialization for the MPB332. You may adapt this example to your debugger. This initialization enables the maximum system clock frequency and disables the software watchdog while enabling the bus monitor. CSBOOT is set to zero-wait state and the block size set to 64K starting at $00000. A7 is initialized to $101FE and the program counter (PC) is initialized to $00200 (A7=101FE, PC=200). Load your program at address $00200.

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Below is the MPB332.ICD initialization macro program listing.

```
reset
pc=400
a7=400
mdf6 400
mdf3 400
symbol SIMCR FFFA00
symbol SYNCR FFFA04
symbol CSBARBT FFFA48
symbol CSORBT FFFA4A
symbol START 00400
mm.w SIMCR 40CF          Set module mapping to $FFF000-$FFFFFF
mm.b SYNCR 7F            Set system clock frequency to 16.78 MHz
watchdog                 Disable watchdog timer
mm.w CSBARBT 0003        Change CSBOOT block size to 64K
mm.w CSORBT 7830         Change wait state to zero
mdf6 START               Display program in PMM window
D0=00000000
D1=00000000
D2=00000000
D3=00000000
D4=00000000
D5=00000000
D6=00000000
D7=00000000
A0=00000000
A1=00000000
A2=00000000
A3=00000000
A4=00000000
A5=00000000
A6=00000000
A7=000101FE
symbol RAMBAR FFFB04
symbol RAMMCR FFFB00
mmw RAMBAR 0100          Set SRAM base address
mmw RAMMCR 0000          Turn on SRAM
mml 10000 4D6F746F       Check SRAM: Write Motorola 68300 Advanced MCUs
mml 10004 726F6C61
mml 10008 20363833
mml 1000C 30302020
mml 10010 41647661
mml 10014 6E636564
mml 10018 20204D43
mml 1001C 55732020
mdf3 10000               Display SRAM in DMM window
```

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```
var.w CSORBT          Show variables in F6 area
var.w CSBARBT
var.w SIMCR           Show variables in F6 area
var.w SYNCR
asciiF3               Show F3 area as ASCII characters
bf 400 2000 0         Using block fill to pause macro execution
mdf6                  Now show memory values in F6 area
asciiF3               Now show memory values in F3 area
PC=START              Enter your program here
```

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CHAPTER 4
MEVB SUPPORT INFORMATION

4.1 INTRODUCTION

This chapter's information is pertains to using the MPB in an MEVB (the MPB installed on a MPFB). Signals on the MPFB logic analyzer connectors are defined by the MPB type.

4.2 LOGIC ANALYZER CONNECTOR SIGNALS

The tables of this chapter describe MPFB logic analyzer connector signals if you install an M68MPB332 on the MPFB. The signal descriptions on J12 – J20 are the logic analyzer pin-outs on the plastic overlay supplied with the MPB.

NOTE

The signal descriptions in the following tables are for quick reference only. The MC68332 User's Manual, MC68332UM/AD, contains a complete description of the MC68332 MCU signals.

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Table 4-1. Logic Analyzer Connector J7 Pin Assignments

Pin	Mnemonic	Signal
1, 2	SPARE	No connection
3	OE(ALL)	I/O PRU OUTPUT ENABLE – Input, active high; when low disables *all* PRU outputs. **NOTE** The SCIM PRU is not used by the M68MPB332 MCU Personality Board. For information on using the PRU on the MPFB refer to the MPFB1632 Modular Platform Board User's Manual, M68MPFB1632/D.
4 – 11	PEPAR7 – PEPAR0	PEPAR OUTPUTS – Output signals that show the *complement* (negated contents) of the PEPAR register. **NOTE** These signals are unused – the PRU is disabled on the MPFB. They are placed in a high impedance state by jumper header W5 on the MPFB.
12 – 19	PE7 – PE0	PORT E I/O SIGNALS – PRU replacement of the port E function. **NOTE** These signals are unused – the PRU is disabled on the MPFB. They are placed in a high impedance state by jumper header W5 on the MPFB.
20	GND	GROUND

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Table 4-2. Logic Analyzer Connector J8 Pin Assignments

Pin	Mnemonic	Signal
1, 2	SPARE	No connection
3	OE(ABG)	I/O PRU OUTPUT ENABLE – Input, active high; when low disables port A, port B, and port G outputs. **NOTE** The SCIM PRU is not used by the M68MPB332 MCU Personality Board. For information on using the PRU on the MPFB refer to the MPFB1632 Modular Platform Board User's Manual, M68MPFB1632/D.
4 – 11	PA7 – PA0	PORT A I/O SIGNALS – PRU replacement of the Port A function. **NOTE** These signals are unused – the PRU is disabled on the MPFB. They are placed in a high impedance state by jumper header W5 on the MPFB.
12 – 19	PB7 – PB0	PORT B I/O SIGNALS – PRU replacement of the Port B function. **NOTE** These signals are unused – the PRU is disabled on the MPFB. They are placed in a high impedance state by jumper header W5 on the MPFB.
20	GND	GROUND

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Table 4-3. Logic Analyzer Connector J9 Pin Assignments

Pin	Mnemonic	Signal
1, 2	SPARE	No connection
3	OE(H)	I/O PRU OUTPUT ENABLE – Input, active high; when low disables the port H outputs. **NOTE** The SCIM PRU is not used by the M68MPB332 MCU Personality Board. For information on using the PRU on the MPFB refer to the MPFB1632 Modular Platform Board User's Manual, M68MPFB1632/D.
4 – 11	PH7 – PH0	PORT H I/O SIGNALS – PRU replacement of the Port H function. **NOTE** These signals are unused – the PRU is disabled on the MPFB. They are placed in a high impedance state by jumper header W5 on the MPFB.
12 – 19	PG7 – PG0	PORT G I/O SIGNALS – PRU replacement of the Port G function. **NOTE** These signals are unused – the PRU is disabled on the MPFB. They are placed in a high impedance state by jumper header W5 on the MPFB.
20	GND	GROUND

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Table 4-4. Logic Analyzer Connector J10 Pin Assignments

Pin	Mnemonic	Signal
1	+5V	+5 VDC POWER – Input voltage (+5Vdc @ 1.0 A) used by the MEVB logic circuits. (To make this pin a no connection, remove the jumper from jumper header W9 on the MPFB.)
2	SPARE	No connection
3	AS	ADDRESS STROBE – Active-low output signal that indicates whether a valid address is on the address bus.
4 – 19	A15 – A0	ADDRESS BUS BITS 15 – 0 – Sixteen bits of the 24-bit address bus.
20	GND	GROUND

Table 4-5. Logic Analyzer Connector J11 Pin Assignments

Pin	Mnemonic	Signal
1	+5V	+5 VDC POWER – Input voltage (+5Vdc @ 1.0 A) used by the MEVB logic circuits. (To make this pin a no connection, remove the jumper from jumper header W9 on the MPFB.)
2	SPARE	No connection
3	DS	DATA STROBE – Active-low output signal. During a read cycle, indicates that an external device should place valid data on the data bus. During a write cycle, indicates that valid data is on the data bus.
4 – 19	D15 – D0	DATA BUS 15 – 0 – 16 bits of the MCU bi-directional data bus lines.
20	GND	GROUND

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Table 4-6. Logic Analyzer Connector J12 Pin Assignments

Pin	Mnemonic	Signal
1, 2	SPARE	No connection
3	CLKOUT	SYSTEM CLOCK OUT – Output signal that is the MCU internal system clock.
4	BERR	BUS ERROR – Active-low signal that indicates that a memory access error has occurred.
5	BKPT / DSCLK	BREAKPOINT – Active-low input signal that signals a hardware breakpoint to the CPU. Development Serial Clock – Clock input signal for the background debug mode.
6	FREEZE QUOT	FREEZE – Output signal that indicates the CPU has acknowledged a breakpoint. QUOTIENT OUT – Output signal that furnishes the quotient bit of the polynomial divider for test purposes.
7	LAT-DSO (Latched IPIPE0)	LATCHED INSTRUCTION PIPE 0 – Latched output signal of the first state of IPIPE0 for CPU16-based MCUs; indicates instruction pipeline activity. Logic low for CPU32-based MCUs.
8	LAT-DSI (Latched IFETCH)	LATCHED INSTRUCTION FETCH (INVERTED) – Latched output signal of the inverted state of IFETCH for CPU32-based MCUs; indicates instruction pipeline activity.
9	DSO	DEVELOPMENT SERIAL OUT – Serial data output signal for background debug mode. INSTRUCTION PIPE for CPU32-based MCUs.
10	DSI	DEVELOPMENT SERIAL IN – Serial data input signal for background debug mode. INSTRUCTION FETCH for CPU32-based MCUs.
11	DSACK1	DATA AND SIZE ACKNOWLEDGE 1 – Active-low input signal that allows asynchronous data transfers and dynamic bus sizing between the MCU and external devices.

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Table 4-6. Logic Analyzer Connector J12 Pin Assignments (continued)

Pin	Mnemonic	Signal
12	DSACK0	DATA AND SIZE ACKNOWLEDGE 0 – Active-low input signal that allows asynchronous data transfers and dynamic bus sizing between the MCU and external devices.
13	FC2 /	FUNCTION CODE 2 – Output signal that identifies the processor state and address space of the current bus cycle.
	CS5	CHIP SELECT 5 – Output signal that selects peripheral or memory devices at programmed addresses.
14	FC1 /	FUNCTION CODE 1 – Output signal that identifies the processor state and address space of the current bus cycle.
	CS4	CHIP SELECT 4 – Output signal that selects peripheral or memory devices at programmed addresses.
15	FC0 /	FUNCTION CODE 0 – Output signal that identifies the processor state and address space of the current bus cycle.
	CS3	CHIP SELECT 3 – Output signal that selects peripheral or memory devices at programmed addresses.
16	SIZ1	TRANSFER SIZE – Active-high output signals that Indicates the number of bytes to be transferred during a bus cycle.
17	SIZ0	TRANSFER SIZE 0 – Active-high output signals that Indicates the number of bytes to be transferred during a bus cycle.
18	R/W	READ/WRITE – Output signal that indicates the direction of data transfer on the bus.
19	BGACK /	BUS GRANT ACKNOWLEDGE – Active-low input signal that indicates that an external device has assumed bus mastership.
	CS2	CHIP SELECT 2 – Output signal that selects peripheral or memory devices at programmed addresses.
20	GND	GROUND

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Table 4-7. Logic Analyzer Connector J13 Pin Assignments

Pin	Mnemonic	Signal
1	+5V	+5 VDC POWER – Input voltage (+5Vdc @ 1.0 A) used by the MEVB logic circuits. (To make this pin a no connection, remove the jumper from jumper header W21 on the MPFB.)
2	SPARE	No connection
3	DSACK1	DATA AND SIZE ACKNOWLEDGE 1 – Active-low input signal that allows asynchronous data transfers and dynamic bus sizing between the MCU and external devices.
4	AVEC	AUTOVECTOR – Active-low input signal that requests an automatic vector during interrupt acknowledge.
5	HALT	HALT – Active-low input/output signal that suspends external bus activity, to request a retry when used with BERR, or for single-step operation.
6	AS	ADDRESS STROBE – Active-low output signal that indicates that a valid address is on the address bus.
7	DS	DATA STROBE – Active-low output signal. During a read cycle, indicates that an external device should place valid data on the data bus. During a write cycle, indicates that valid data is on the data bus.
8	BR / CS0	BUS REQUEST – Active-low input signal that indicates that an external device requires bus mastership. CHIP SELECT 0 – Output signal that selects peripheral or memory devices at programmed addresses.
9	BG / CS1	BUS GRANT – Active-low output signal that indicates that the MCU has relinquished the bus. CHIP SELECT 1 – Output signal that selects peripheral or memory devices at programmed addresses.
10	CSBOOT	BOOT CHIP SELECT – An active-low output chip select for external boot startup ROM.
11	CLKOUT	SYSTEM CLOCK OUTPUT – MCU internal clock output signal.

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Table 4-7. Logic Analyzer Connector J13 Pin Assignments (continued)

Pin	Mnemonic	Signal
12	A23 / CS10	ADDRESS BUS BIT 23 – One bit of the 24-bit address bus. CHIP SELECT 10 – Output signal that selects peripheral or memory devices at programmed addresses.
13	A22 / CS9	ADDRESS BUS BIT 22 – One bit of the 24-bit address bus. CHIP SELECT 9 – Output signal that selects peripheral or memory devices at programmed addresses.
14	A21 / CS8	ADDRESS BUS BIT 21 – One bit of the 24-bit address bus. CHIP SELECT 8 – Output signal that selects peripheral or memory devices at programmed addresses.
15	A20 / CS7	ADDRESS BUS BIT 20 – One bit of the 24-bit address bus. CHIP SELECT 7 – Output signal that selects peripheral or memory devices at programmed addresses.
16	A19 / CS6	ADDRESS BUS BIT 19 – One bit of the 24-bit address bus. CHIP SELECT 6 – Output signal that selects peripheral or memory devices at programmed addresses.
17 – 19	A18 – A16	ADDRESS BUS 18 – 16 – Three bits of the 24-bit address bus.
20	GND	GROUND

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Table 4-8. Logic Analyzer Connector J14 Pin Assignments

Pin	Mnemonic	Signal
1, 2	SPARE	No connection
3	DSACK0	DATA AND SIZE ACKNOWLEDGE 0 – Active-low input signal that allows asynchronous data transfers and dynamic bus sizing between the MCU and external devices.
4	MODCLK	CLOCK MODE SELECT – Input signal that configures the MCU internal clock at reset.
5	TSTME / TSC	TEST MODE ENABLE – Input signal that enables hardware for test mode. THREE STATE CONTROL – When TSC is logic high, this input signal forces all output drivers to a high-impedance state.
6	RESET	RESET – Active-low, bi-directional signal to start a system reset.
7	RMC	READ-MODIFY-WRITE CYCLE – Active-low output signal that identifies the bus cycle as part of an indivisible read-modify-write operation.
8	SPARE	No connection
9 – 15	GND	GROUND
16 – 19	SPARE	No connection
20	GND	GROUND

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Table 4-9. Logic Analyzer Connector J15 Pin Assignments

Pin	Mnemonic	Signal
1 – 3	SPARE	No connection
4	GND	GROUND
5	T2CLK	TPU CLOCK – External input clock source to the TPU.
6	GND	GROUND
7 – 10	TP15 – TP12	TIME PROCESSOR UNIT CHANNELS – TPU input/output channels.
11	GND	GROUND
12 – 15	TP11 – TP8	TIME PROCESSOR UNIT CHANNELS – TPU input/output channels.
16, 17	GND	GROUND
18, 19	SPARE	No connection
20	GND	GROUND

Table 4-10. Logic Analyzer Connector J16 Pin Assignments

Pin	Mnemonic	Signal
1 – 4	SPARE	No connection
5 – 12	TP0 – TP7	TIME PROCESSOR UNIT CHANNELS – TPU input/output channels.
13 – 19	SPARE	No connection
20	GND	GROUND

Table 4-11. Logic Analyzer Connector J17 Pin Assignments

Pin	Mnemonic	Signal
1 – 4	SPARE	No connection
5 – 16	GND	GROUND
17 – 19	SPARE	No connection
20	GND	GROUND

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Table 4-12. Logic Analyzer Connector J18 Pin Assignments

Pin	Mnemonic	Signal
1 – 4	SPARE	No connection
5	GND	GROUND
6	MISO	MASTER-IN, SLAVE-OUT – Serial input to SPI in master mode; serial output from SPI in slave mode.
7	MOSI	MASTER-OUT, SLAVE-IN – Serial output from SPI in master mode; serial input to SPI in slave mode.
8	SCK	SPI SERIAL CLOCK – In master mode, the clock signal from the SPI; in slave mode the clock signal to the SPI.
9	PCS0 / SS	PERIPHERAL CHIP SELECT 0 – Active-low output SPI peripheral chip select signal. SLAVE SELECT – Bi-directional, active-low signal that initiates serial transmission when SPI is in slave mode; causes mode fault in master mode.
10 – 12	PCS1 – PCS3	PERIPHERAL CHIP SELECT 1 through 3 – Active-low output SPI peripheral chip select signal.
13	TXD	TRANSMIT DATA – Serial data output line to serial communication interface.
14	RXD	RECEIVE DATA – Serial data input line to serial communication interface.
15, 16	GND	GROUND
17 – 19	SPARE	No connection
20	GND	GROUND

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Table 4-13. Logic Analyzer Connector J19 Pin Assignments

Pin	Mnemonic	Signal
1 – 4	SPARE	No connection
5 – 12	GND	GROUND
13 – 19	SPARE	No connection
20	GND	GROUND

Table 4-14. Logic Analyzer Connector J20 Pin Assignments

Pin	Mnemonic	Signal
1 – 4	SPARE	No connection
5	GND	GROUND
6 – 12	IRQ1 – IRQ7	TARGET INTERRUPT REQUEST 1 – 7 - Active-low input signals from the target that asynchronously provides an interrupt priority level to the CPU. IRQ1 has the lowest priority, IRQ7 has the highest.
13 – 18	GND	GROUND
19	SPARE	No connection
20	GND	GROUND

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CHAPTER 5
MAPI SUPPORT INFORMATION

5.1 INTRODUCTION

The information in this chapter is relevant when the MPB is to be installed on a target system. The figures in this chapter show the MAPI interface connector layout and pin assignments for MPB connectors P1, P2, P3, and P4 (Figures 5-1 through 5-5).

The connectors required to interface to the MAPI bus are:

2 – Robinson Nugent, 2 X30 plugs, P50L-060P-AS-TGF

2 – Robinson Nugent, 2 X40 plugs, P50L-080P-AS-TGF

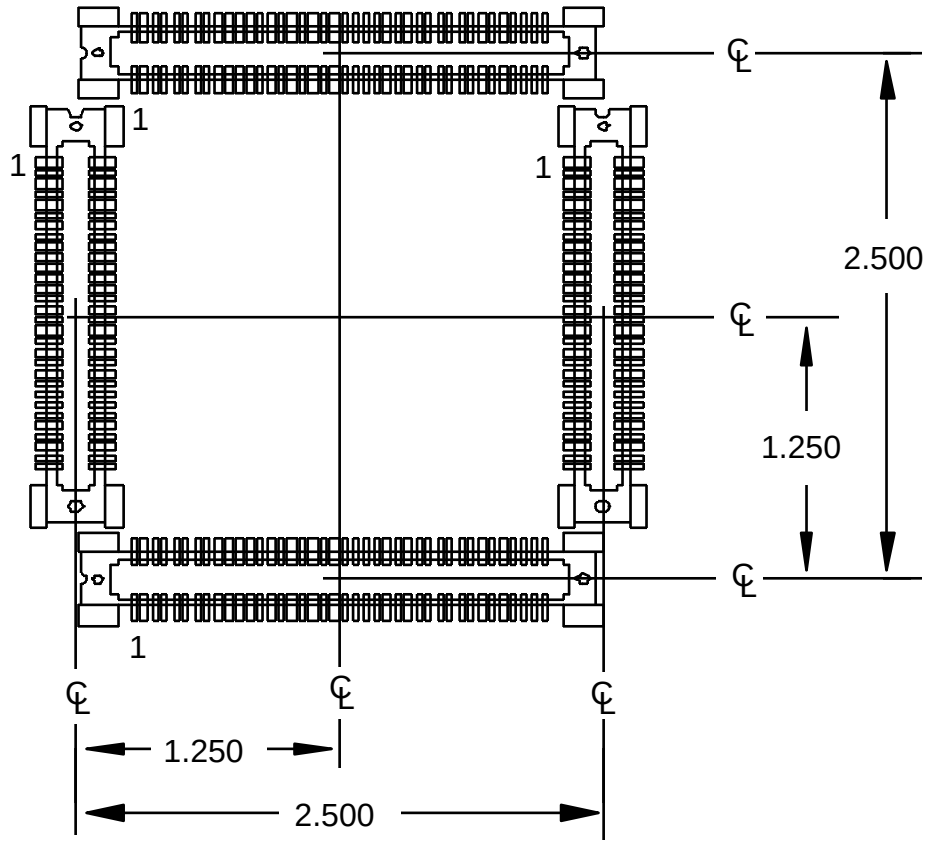

Figure 5-1. MAPI Interface Connector Layout

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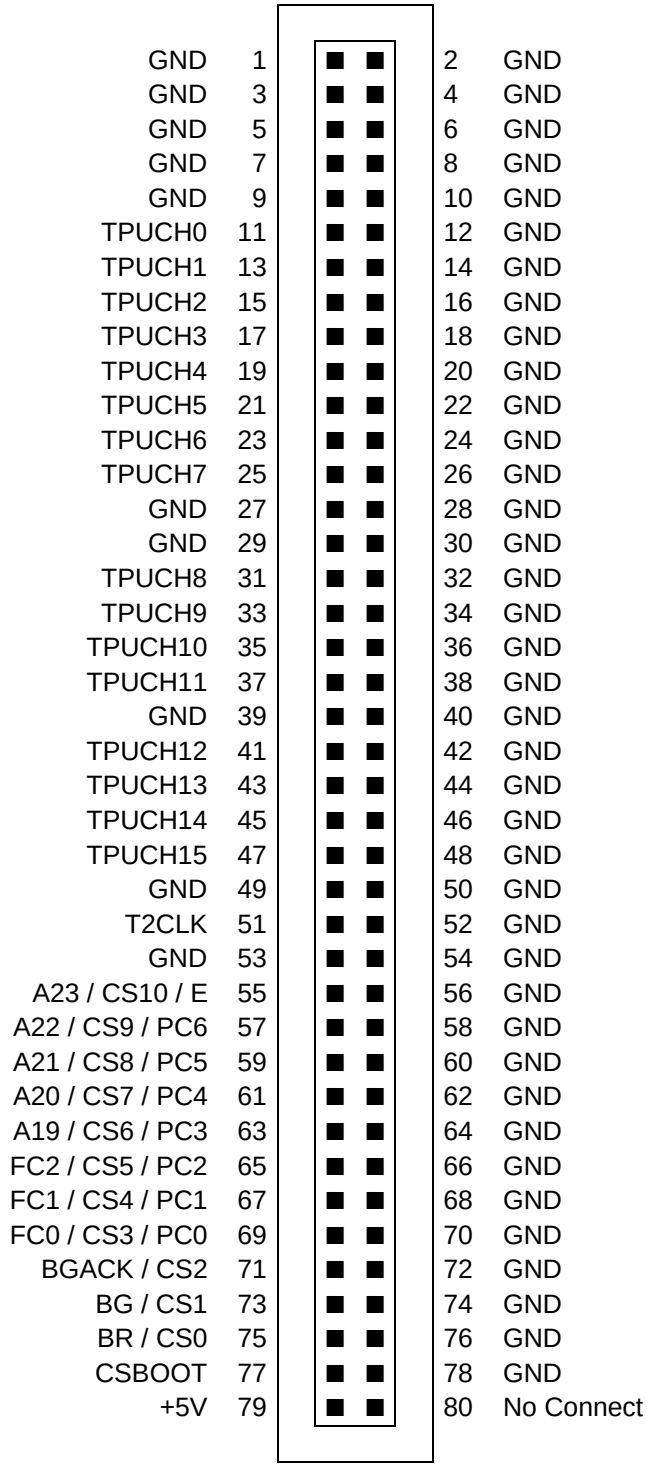

Figure 5-2. MAPI Interface Connector P1 Pin Assignments

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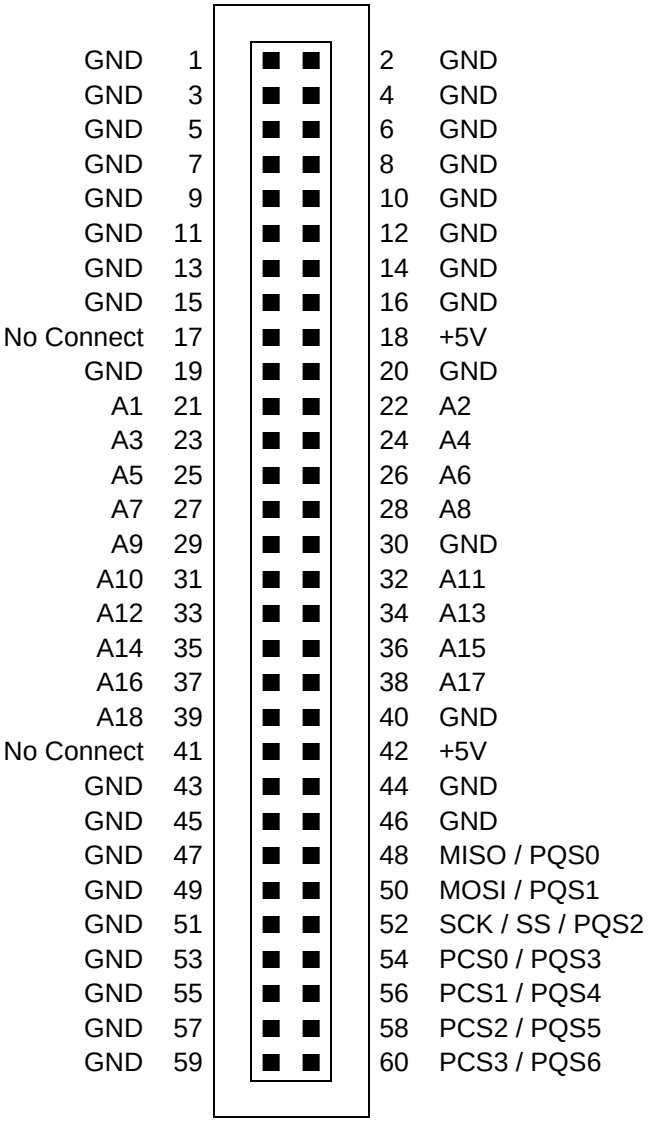

Figure 5-3. MAPI Interface Connector P2 Pin Assignments

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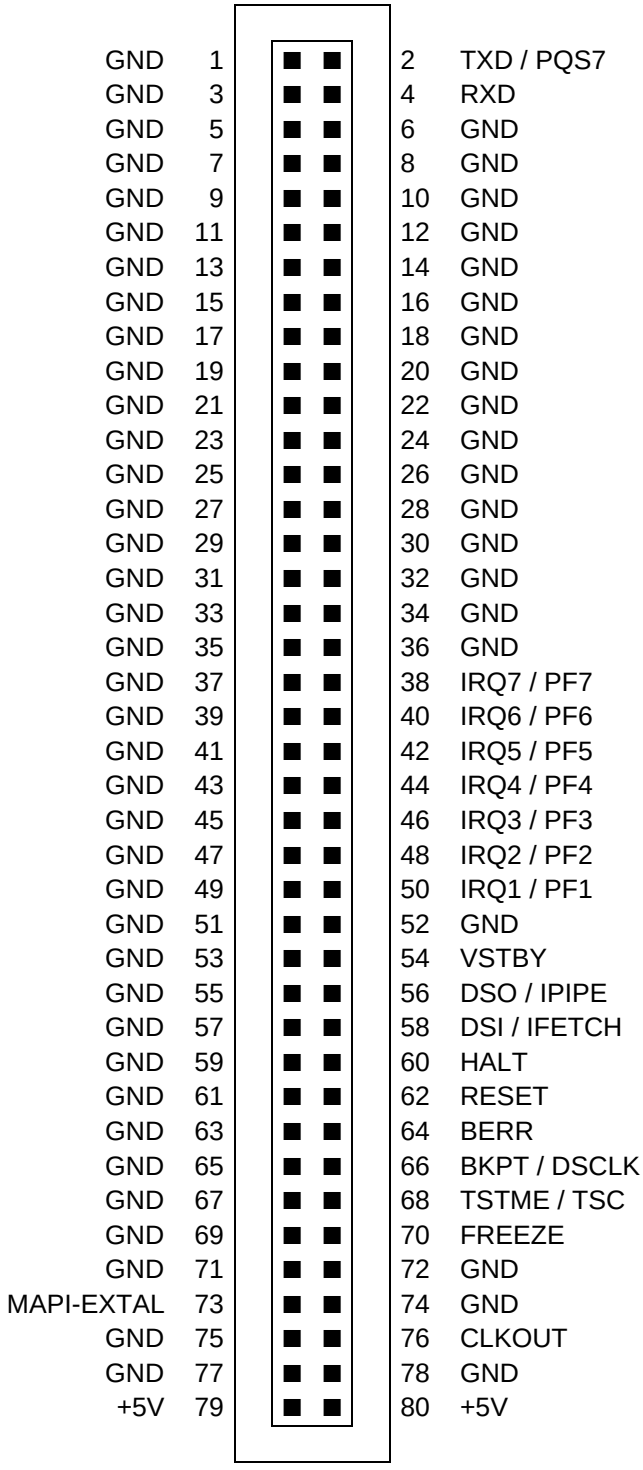

Figure 5-4. MAPI Interface Connector P3 Pin Assignments

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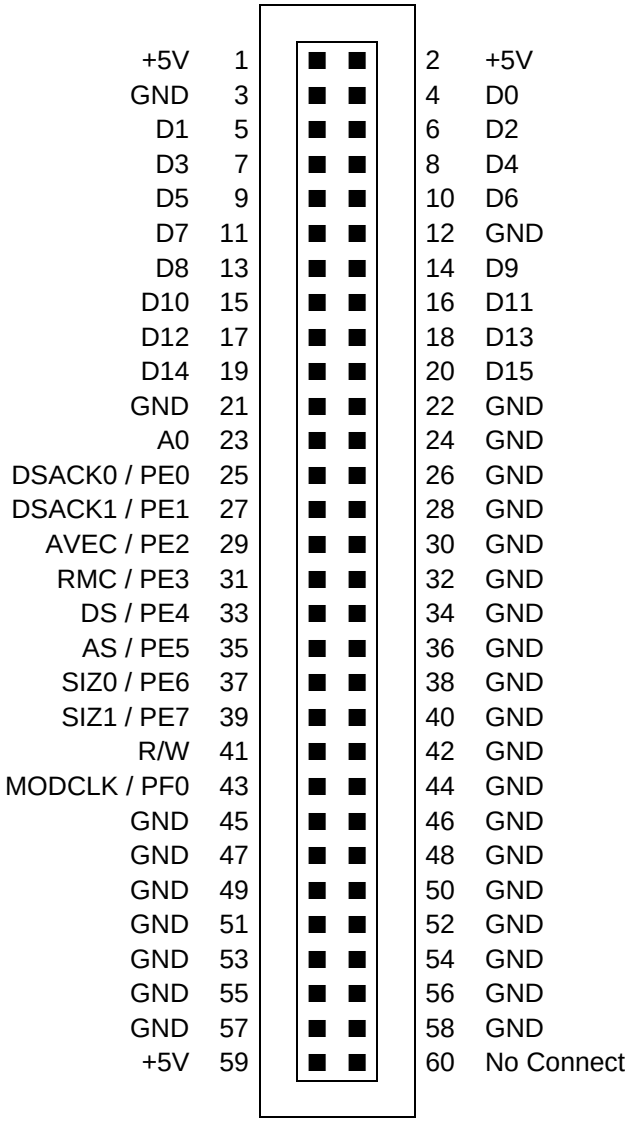

Figure 5-5. MAPI Interface Connector P4 Pin Assignments

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CHAPTER 6
SCHEMATIC DIAGRAMS

6.1 INTRODUCTION

This chapter contains the M68MPB332 MCU Personality Board (MPB) schematic diagrams. These schematic diagrams are for reference only and may deviate slightly from the circuits on your MPB.

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6B	MCU & CLOCK - MC68331
7	PULLUPS/PULLDOWNS/PERSONALITY ID
8	SIGNAL CROSS REFERENCES

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED
	0	ORIGINAL RELEASE	05/31/94	R.G.
	A	FIX CS0,2,3,5 <SHEET 6>		

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DRAWN BY: R. G.	DATE: 5/26/93
DESIGN ENGINEER: G. P.	DATE: 5/07/94
PROJECT LEADER: R. G.	DATE: 5/26/94

MOTOROLA INC.
MICROPROCESSOR AND MEMORY TECHNOLOGIES GROUP
6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA

TITLE: SCHEMATIC - MPB331B,MPB332B,MPB335B

SIZE		DWG. NO.	REV:
A	GEDTTL: BOARD GEDABV: MPB332B_B	63ASE90402W	A

LAST_MODIFIED=Wed Jun 29 11:13:48 1994 SHEET 1 OF 8

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63ASE90402W REV: A

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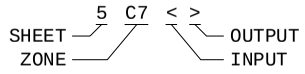
NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, 5%, 1/8 WATT.
   ALL CAPACITORS ARE IN UF. 50V.
   ALL VOLTAGES ARE DC.
2. INTERRUPTED LINES CODED WITH THE SAME LETTER OR LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.
3. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH THE MANUFACTURER.
4. SPECIAL SYMBOL USAGE:
   * DENOTES - ACTIVE LOW SIGNAL.
   <> DENOTES - VECTORED SIGNALS.
5. INTERPRET DIAGRAM IN ACCORDANCE WITH AMERICAN NATIONAL STANDARDS INSTITUTE SPECIFICATIONS, CURRENT REVISION, WITH THE EXCEPTION OF LOGIC BLOCK SYMBOLOGY.
6. CODE FOR SHEET TO SHEET REFERENCES IS AS FOLLOWS:



7. VCC LOCATIONS
   UNLESS OTHERWISE SPECIFIED, VCC IS APPLIED TO:
   PIN 8 OF ALL 8-PIN ICS
   PIN 14 OF ALL 14-PIN ICS
   PIN 16 OF ALL 16-PIN ICS
   PIN 20 OF ALL 20-PIN ICS, ETC.
8. GROUND LOCATIONS
   UNLESS OTHERWISE SPECIFIED, GROUND IS APPLIED TO:
   PIN 4 OF ALL 8-PIN ICS
   PIN 7 OF ALL 14-PIN ICS
   PIN 8 OF ALL 16-PIN ICS
   PIN 10 OF ALL 20-PIN ICS, ETC.

NOTES

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LAST_MODIFIED=Wed Jun 1 18:16:49 1994		SHEET 2 OF 8	

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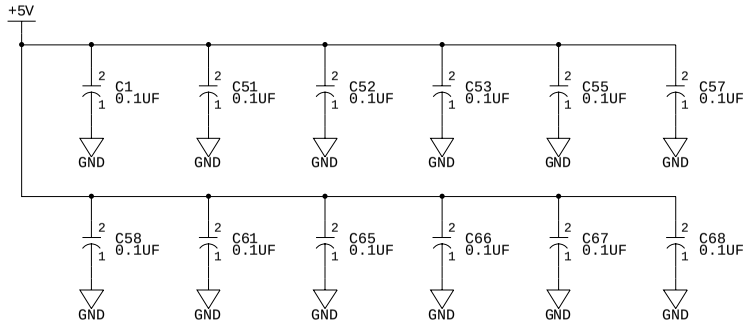
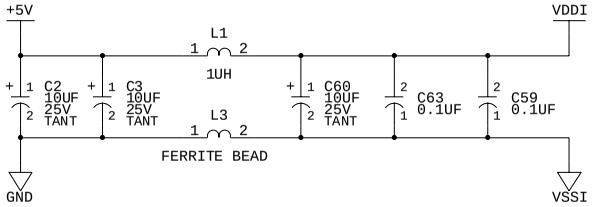
+5V AND GND DECOUPLING
FOR VDDE OF MCU AND OSCILLATOR



VDDI/VSSI GENERATION



BYPASS CAPACITORS, CLEAN POWER FILTERS

SIZE		DWG. NO.	REV:
A	GEDTTL: BOARD GEDABV: MPB332B_B	63ASE90402W	A
LAST_MODIFIED=Tue Jun 14 16:24:44 1994		SHEET 3 OF 8	

63ASE90402W
REV: A

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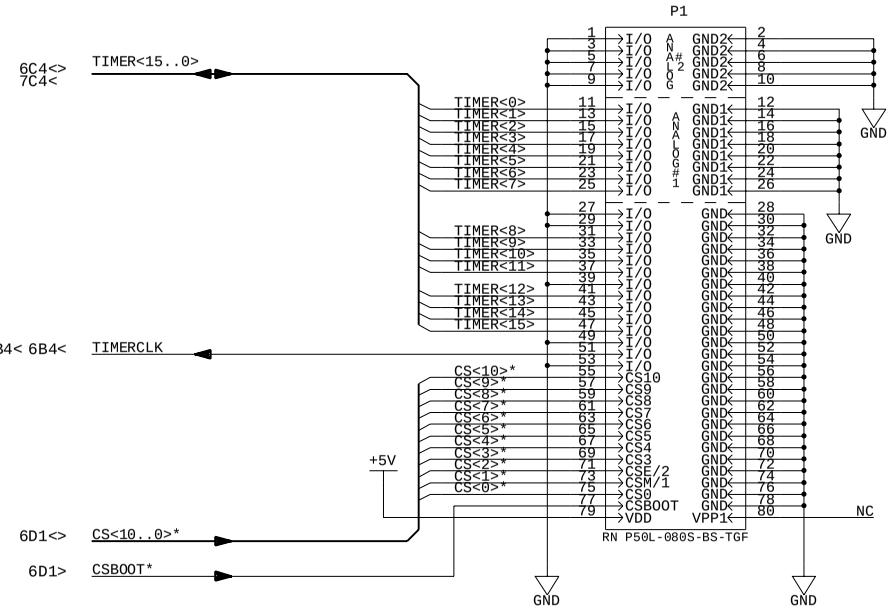
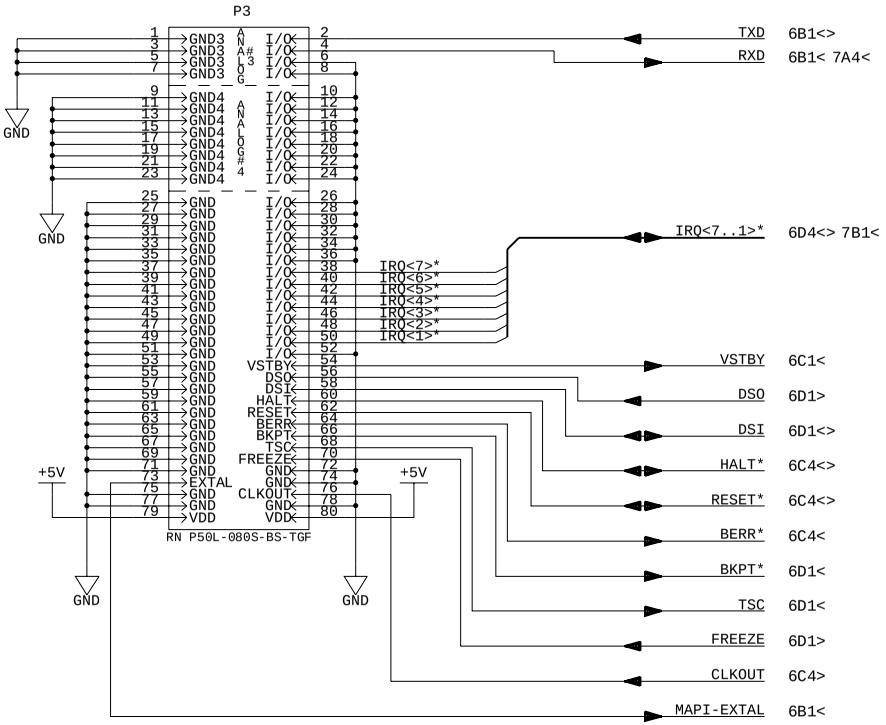
MAPI BUS P1



MAPI BUS P3



MODULAR ACTIVE PROBE INTERCONNECT P1 & P3

SIZE		DWG. NO.	REV:
A	GEDTTL: BOARD GEDABV: MPB332B_B	63ASE90402W	A
LAST_MODIFIED=Tue Jun 14 16:24:47 1994		SHEET 4 OF 8	

63ASE90402W REV: A

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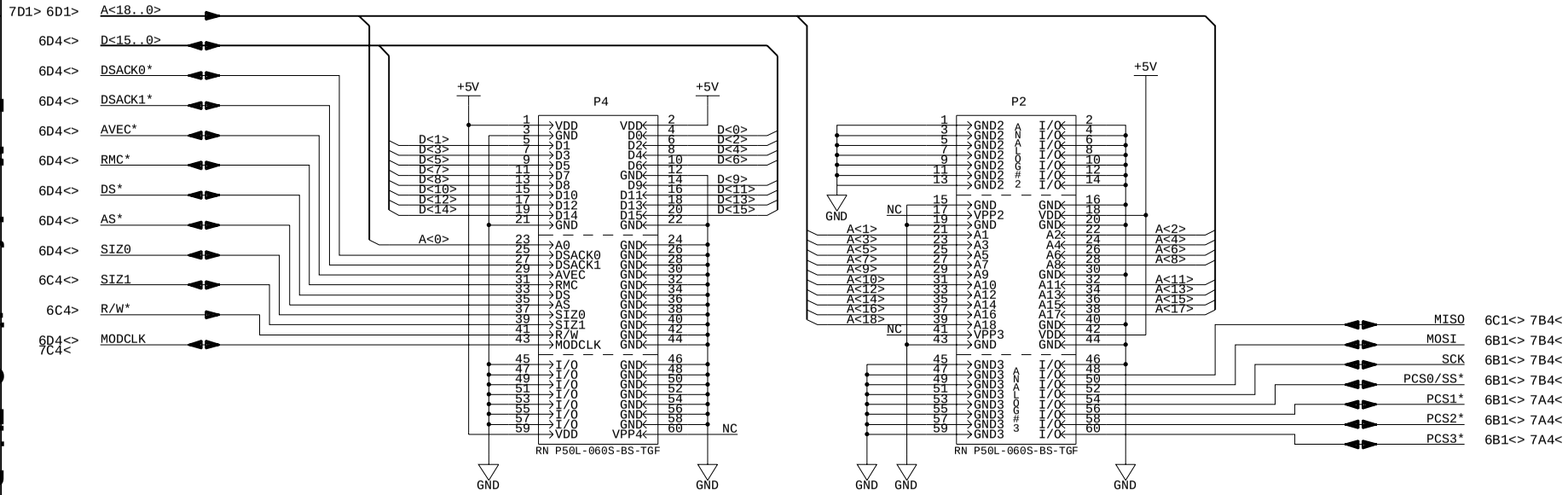
Go to: www.freescale.com



MODULAR ACTIVE PROBE INTERCONNECT P2 & P4

SIZE		DWG. NO.	REV:
A	GEDTTL: BOARD GEDABV: MPB332B_B	63ASE90402W	A
LAST_MODIFIED=Tue Jun 14 16:24:50 1994		SHEET 5 OF 8	

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63ASE90402W
REV: A

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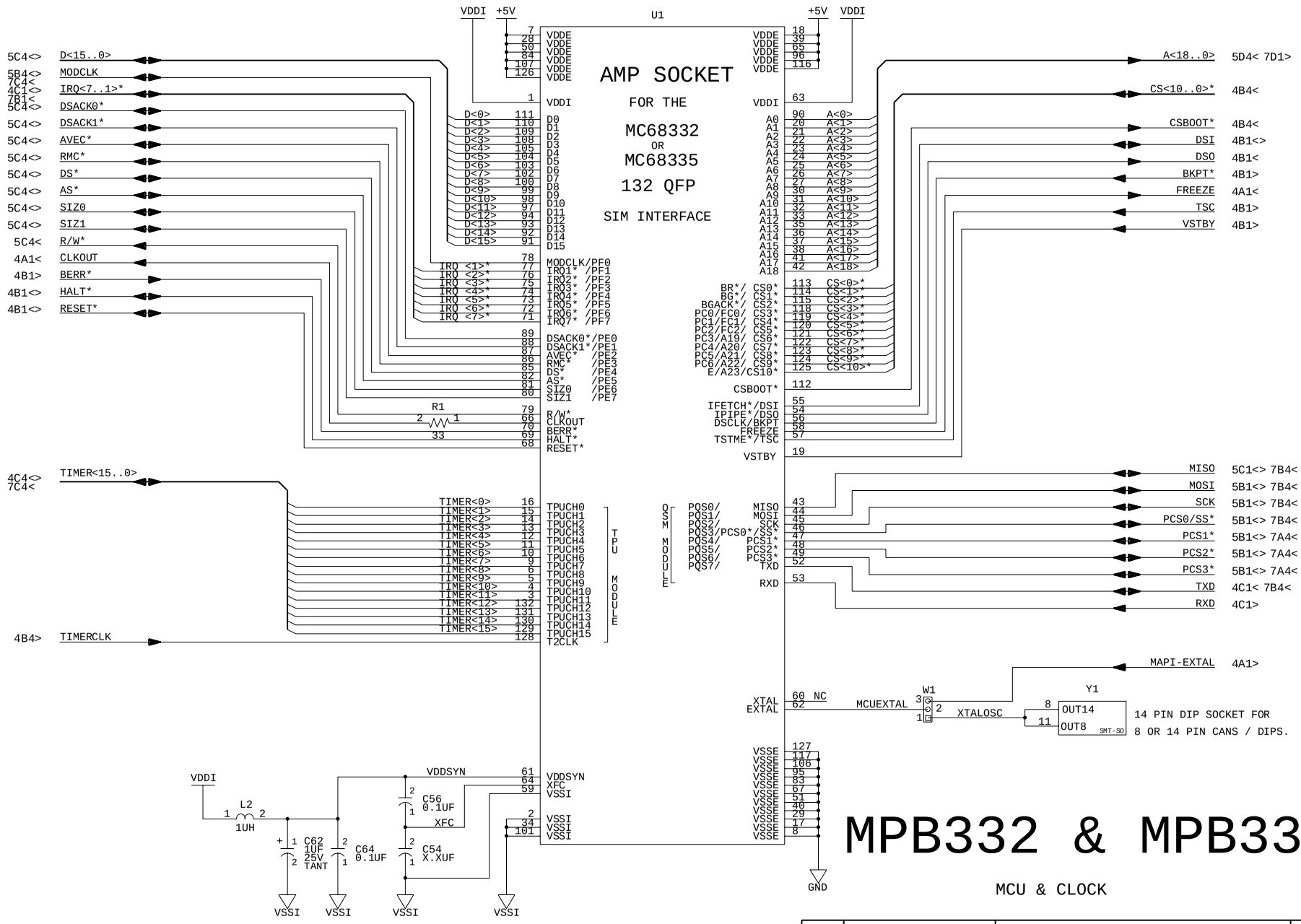

NOTE: 1) PLACE THE CAP BETWEEN VDDSYN & XFC AS CLOSE TO MCU PINS AS POSSIBLE.
2) THE CAP BETWEEN XFC & VSSI IS OPTIONAL.

MPB332 & MPB335

MCU & CLOCK

SIZE		DWG. NO.	REV:
A	GEDTTL: BOARD GEDABV: MPB332B_B	63ASE90402W	A
LAST_MODIFIED=Tue Jun 14 16:24:54 1994		SHEET 6A OF 8	

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63ASE90402W

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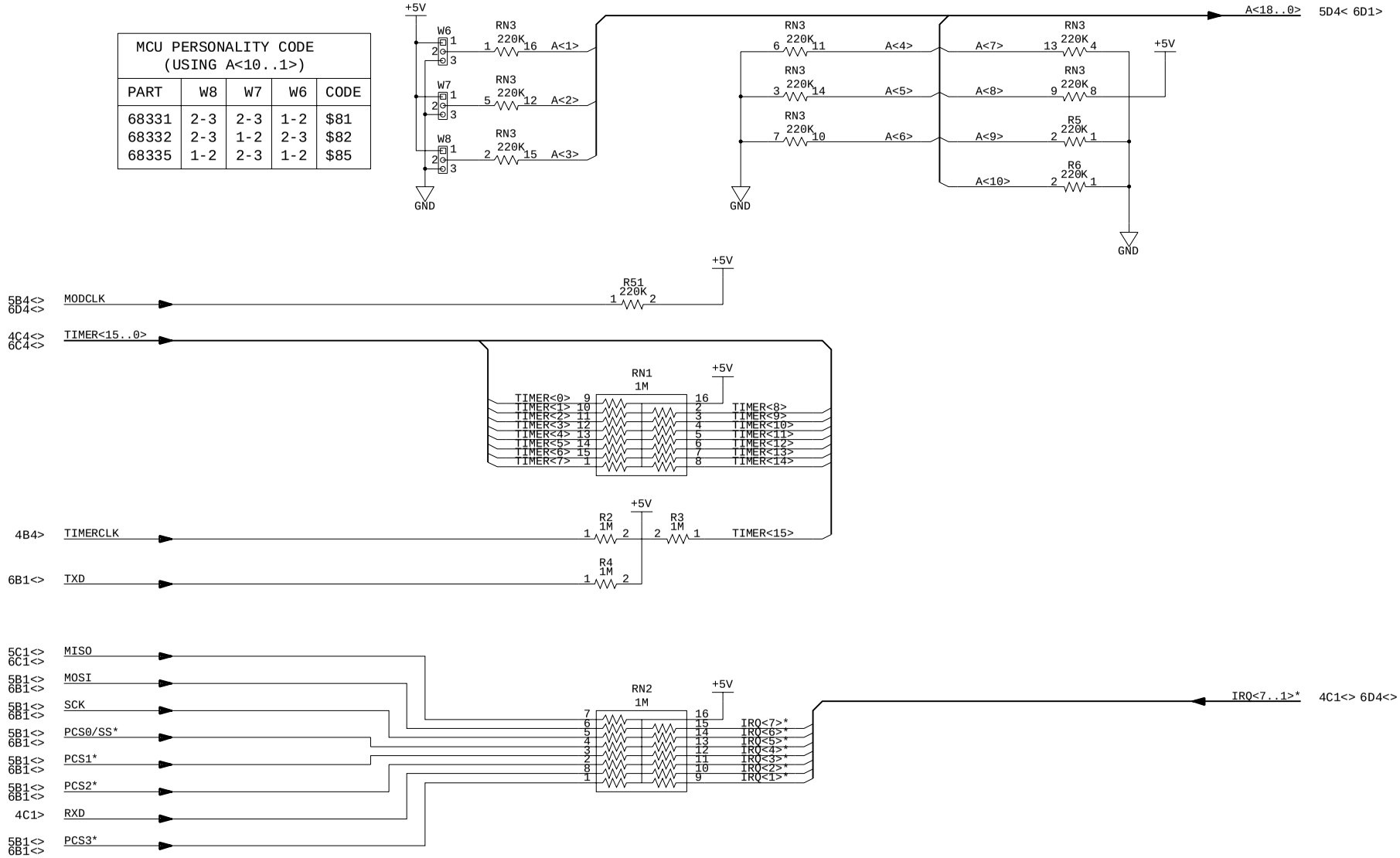
MCU PERSONALITY CODE (USING A<10..1>)				
PART	W8	W7	W6	CODE
68331	2-3	2-3	1-2	$81
68332	2-3	1-2	2-3	$82
68335	1-2	2-3	1-2	$85



PULL-UPS / PULL-DOWNS / PERSONALITY ID

SIZE		DWG. NO.	REV:
A	GEDTTL: BOARD GEDABV: MPB332B_B	63ASE90402W	A
LAST_MODIFIED=Tue Jun 14 16:24:57 1994		SHEET 7 OF 8	

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63ASE90402W
REV: A

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*** Signal Cross-Reference ***
--- for the entire design --

A <18..0>	5D4< 6D1> 7D1>
AS *	5C4<> 6D4<>
AVEC *	5C4<> 6D4<>
BERR *	4B1> 6C4<
BKPT *	4B1> 6D1<
CLKOUT	4A1< 6C4>
CS <10..0> *	4B4< 6D1<>
CSBOOT *	4B4< 6D1>
D <15..0>	5C4<> 6D4<>
DS *	5C4<> 6D4<>
DSACK0 *	5C4<> 6D4<>
DSACK1 *	5C4<> 6D4<>
DSI	4B1<> 6D1<>
DSO	4B1< 6D1>
FREEZE	4A1< 6D1>
HALT *	4B1<> 6C4<>
IRQ <7..1> *	4C1<> 6D4<> 7B1<
MAPI-EXTAL	4A1> 6B1<
MISO	5C1<> 6C1<> 7B4<
MODCLK	5B4<> 6D4<> 7C4<
MOSI	5B1<> 6B1<> 7B4<
PCS0/SS *	5B1<> 6B1<> 7B4<
PCS1 *	5B1<> 6B1<> 7A4<
PCS2 *	5B1<> 6B1<> 7A4<
PCS3 *	5B1<> 6B1<> 7A4<
R/W *	5C4< 6C4>
RESET *	4B1<> 6C4<>
RMC *	5C4<> 6D4<>
RXD	4C1> 6B1< 7A4<
SCK	5B1<> 6B1<> 7B4<
SIZ0	5C4<> 6D4<>
SIZ1	5C4<> 6C4<>
TIMER <15..0>	4C4<> 6C4<> 7C4<
TIMERCLK	4B4> 6B4< 7B4<
TSC	4B1> 6D1<
TXD	4C1< 6B1<> 7B4<
VSTBY	4B1> 6C1<

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63ASE90402W REV: A

SIGNAL CROSS REFERENCES

SIZE		DWG. NO.	REV:
A	GEDTTL: BOARD GEDABV: MPB332B_B	63ASE90402W	A
LAST_MODIFIED=Wed Jun 1 18:34:10 1994		SHEET 8 OF 8	

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