Rev 1.1 November 1998

# MC145576

## Flexible ISDN NT1



*This document contains information on a new product. Specifications and information herein are subject to change without notice.*

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# 1 Introduction

## 1.1 Background

Since the development of the computer, there has been pressure to use the existing telephone network infrastructure to send digital data transmissions. The explosive evolution of digital technology not only converted the telephone system itself to a digital switching system (starting in the 1960s), but also encouraged the development of the modem and related technology that has in turn, along with the information revolution and the internet, created a ravenous demand for access. Anticipating the industry growth and demands by private and public users, the International Telecommunications Union (ITU), under its former United Nations title CCITT, initiated a recommendation for the development of international standards for an Integrated Services Digital Network (ISDN) in 1984. In the United States, however, competing interests slowed the acceptance and development of such a system due to different implementation standards. Finally, in the 1990's, U.S. manufacturers agreed upon a national ISDN standard NI1. This has recently been replaced with the more comprehensive NI2 standard.

A single ISDN connection uses a 2-wire User-interface (U-interface) from the incoming telephone system switch. The ISDN line must be connected through a device called a Network Termination 1 (NT1) that converts the U-interface signal into a 4-wire S/T signal that connects to an ISDN Terminal Equipment 1 (TE1) device. This is different from a standard telephone which is classified as a Terminal Equipment 2 (TE2) device. A Terminal Adapter (TA) is required to convert the S/T signal to an R signal to connect to a standard telephone device (i.e., a TE2).

An earlier Motorola solution for the NT1 interface used a chip-set with an MC145574 (for the S/T-Interface) and an MC145572 (for the U-Interface). The Motorola MC145576 is a single-chip Integrated ISDN NT1 that offers a low cost, highly integrated solution for the design of a Network Termination Equipment. With a flexible interface compatible with other Motorola ISDN components, the MC145576, when combined with Motorola's controller family, becomes the heart of a powerful and cost-effective Smart NT1 solution.

## 1.2 Features

Key features of the MC145576 transceiver include :

- Full compliance with appropriate USA and European recommendations, including:
  - U-Interface (ANSI T1.601-1992, ETSI ETR 080, FT CS3211) in NT mode using 2B1Q line coding
  - S/T-Interface (ITU .430, ETSI ETS 300012 and ANSI T1.605) in NT mode
- MC145572 and MC145574 (U and S/T-Interfaces) conformant, meeting and exceeding all loop performance requirements according to US and European standards
- Supports Micro-linebreaks according to ETSI ETR 080
- Warm start capability
- Fully automatic activation in GCI mode
- Automatic handling of basic maintenance functions
- Automatic Internal Compliance with the Embedded Operations Channel (EOC) Protocol as specified in ANSI and ETSI standards
- Flexible system interface, pin selectable (IDL+SCP) or GCI interface
- NT Terminal Interface
- Dedicated pins for Pulse test signal generation, Power Modes select PS1/2, Fixed/Adaptive timing selection for S bus, Loopback active and LED activation pins in GCI mode
- Complete set of loopbacks
- NT synchronizes to and operates with 80 kHz ± 32 ppm received signal from LT
- Low power consumption (250 mW typical)
- S and Q multiframe capability via external micro-controller connection
- High Performance CMOS Process Technology
- Compatible with 3 V devices
- Single 5 V power supply
- GCI and IDL/SCP interfaces, allowing for compatibility with previous designs based on MC145574 (S/T-Interface) and MC145572 (U-Interface) chip-set. The SCP serial interface allows connection to the extensive family of Motorola controllers.
- When combined with a member of the MC68302 family of multiprotocol controllers, a MC145484 PCM codec, and an analog line interface (SLIC), provides an optimal Smart NT1 or Smart Terminal Adaptor (U-Interface based TA with a S/T bus access). The same architecture can be used with a second codec and SLIC to allow for a dual analog interface design.

## 1.3 Block Diagram

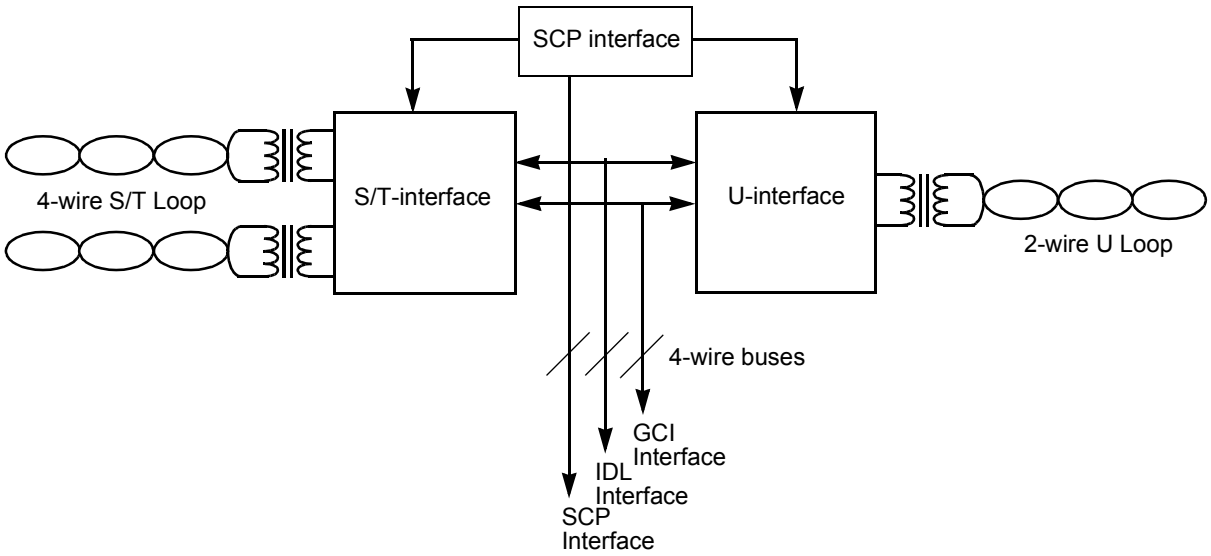


**Figure 1-1.** MC145576 Block Diagram

As shown in **Figure 1-1**, the MC145576 dual transceiver offers a single chip NT-1 solution by combining support for a two-wire U interface connected through the chip to a four-wire S/T interface. This can offer a cost reduction for designs with a two-chip implementation (one for the U interface and one for the S/T interface). The Serial Control Port (SCP) allows configuration and control of both external interfaces. The MC145576 can be configured for Motorola Interchip Digital Link (IDL) or General Circuit Interface (GCI) operation.

## 1.4 NT1 Functional Overview

When combined with a microcontroller, such as the Motorola MC68LC302, the MC145576 can be used to provide a complete Smart NT-1 solution that incorporates a Terminal Adapter (TA) to interface between the Plain Old Telephone System (POTS) R interface and the S/T interface. The microcontroller provides two serial communication controllers that can support asynchronous or synchronous communication that are used to connect to the MC145576 IDL or GCI serial interfaces. A system typically uses the IDL mode or the GCI mode.

## 1.5 Manual Organization

This manual uses the following organizational structure:

- Section 1 Introduction
- Section 2 ISDN Basic Access System Overview
- Section 3 Signal Descriptions
- Section 4 Modes of Operation
- Section 5 Register Description Reference
- Section 6 SCP Mode Device Functionality
- Section 7 IDL Interface Mode Device Functionality
- Section 8 GCI Mode Device Functionality
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- Section 10 Transmission Line Interface Circuitry
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- Appendix A MC145576 Evaluation Board
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- Appendix C Printed Circuit Board Layout
- Appendix D Line Interface Circuit Component Value Calculations
- Appendix E Glossary of Terms and Abbreviations
- Appendix F Standards Bodies
- Index (not included in this release)

## 1.6 Notation Conventions

The following notation conventions are used in this document:

- Signal representations:
  - Active high signals (Logic One) use the signal name (e.g., A0).
  - Active low signals (Logic Zero) use the signal name with an overbar (e.g., $\overline{WE}$ or $\overline{OE}$).
- Numeric representations:
  - Hexadecimal values start with a "$" sign (e.g., $0FF0 or $80).
  - Decimal values have no symbol attached to the number (e.g., 10 or 34).
  - Binary values start with the letter "b" (e.g., b1010 or b0011).
- Register/bit designators:
  - NR2(b3) refers to Nibble Register 2, Bit 3.
  - BR2(b6) refers to Byte Register 2, Bit 6.
  - OR1(b1) refers to Overlay Register 1, Bit 1.

# 2

# ISDN Basic Access System Overview

## 2.1 ISDN Reference Model

The ISDN reference model is shown in Figure 2-1. This is a general model that can be adapted to many different implementations of the ISDN. The diagram indicates the position of the U-reference point between the LT and the Network Termination 1 (NT1) blocks and the T-reference point between the NT2 and the NT1 in the model.

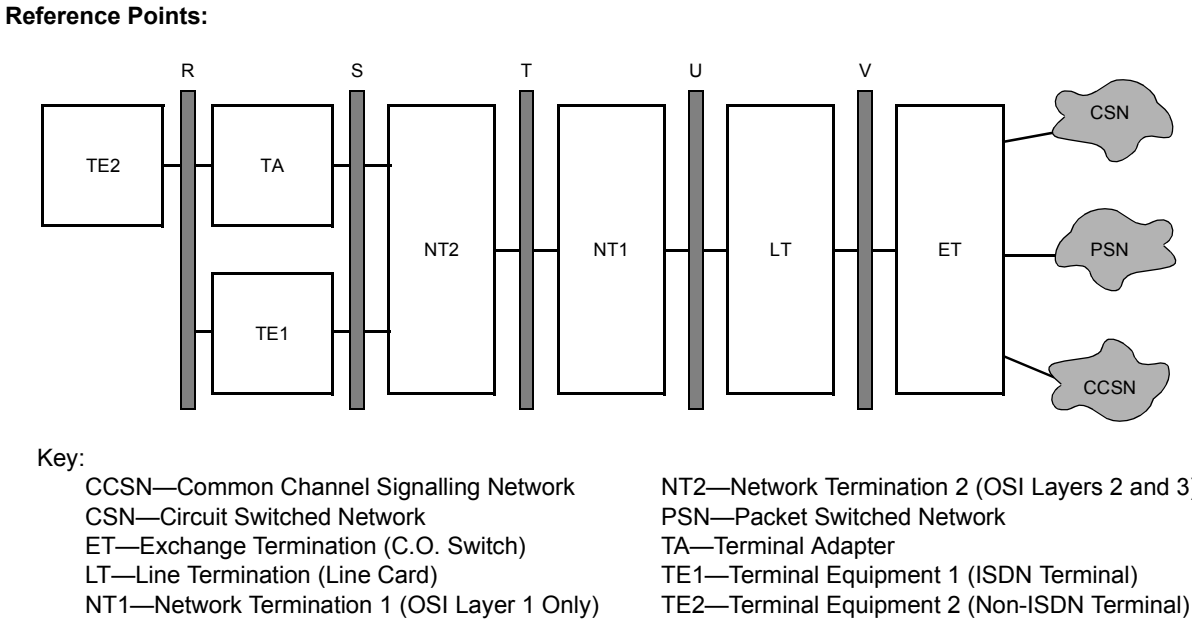



**Figure 2-1.** ISDN Reference Model

The U-interface is the physical access point to the ISDN at the U-reference point. This interface is a single twisted wire pair supporting full-duplex transmission of digital information at a rate of 160 kbps. The twisted wire pair can extend up to 18,000 feet and may include bridge taps. This interface is often referred to as a Digital Subscriber Line.

The S-interface and T-interface are the physical access points at the S- and T-reference points, respectively. The interface supports full duplex communications between printed circuit board integrated circuits (ICs) using two 64 kbps B channels and one 16 kbps D channel. The chip is programmable to support several four-wire communication protocols described in detail in **Sections 6–8.**

## 2.2 ISDN Applications

**Figure 2-2** shows a typical ISDN application using Motorola semiconductor solutions. The NT1 converts the 2-wire U-interface to the 4-wire S/T-interface as shown by using an MC145576. Also shown is a highly integrated U-interface ISDN terminal, designated NT1/TE1, which implements a complete voice and data terminal with a U-interface for immediate and cost effective access to the ISDN. The MC145572 is shown interfaced to the M68000 core-based MC68302 Integrated Multiprotocol Processor (IMP), which handles layers 2–7 of the OSI reference model. Voice is supported with a conventional codec-filter device, such as the MC14LC5480. The network is completed with a TA and an S/T-interface ISDN terminal (TE1). Two different architectures are shown: the TA is implemented with the MC68LC302 IMP, and the TE1 is shown implemented with the MC68QH302 IMP.

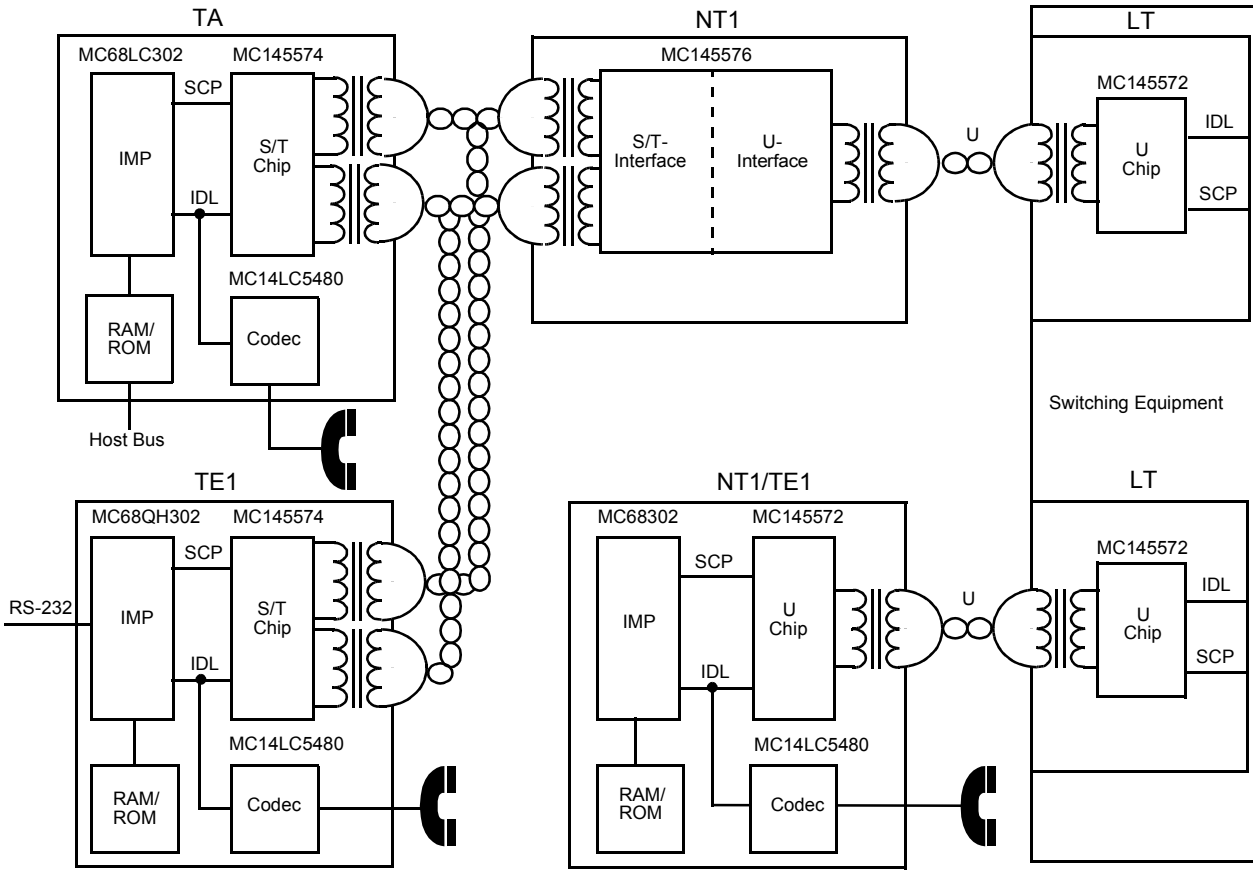



**Figure 2-2.** Typical ISDN Application

# 3

# Signal Descriptions

## 3.1 Introduction

The Motorola MC145576 ISDN Single Chip NT1 Transceiver is available in a 44-pin TQFP package (see **Figure 3-1**).

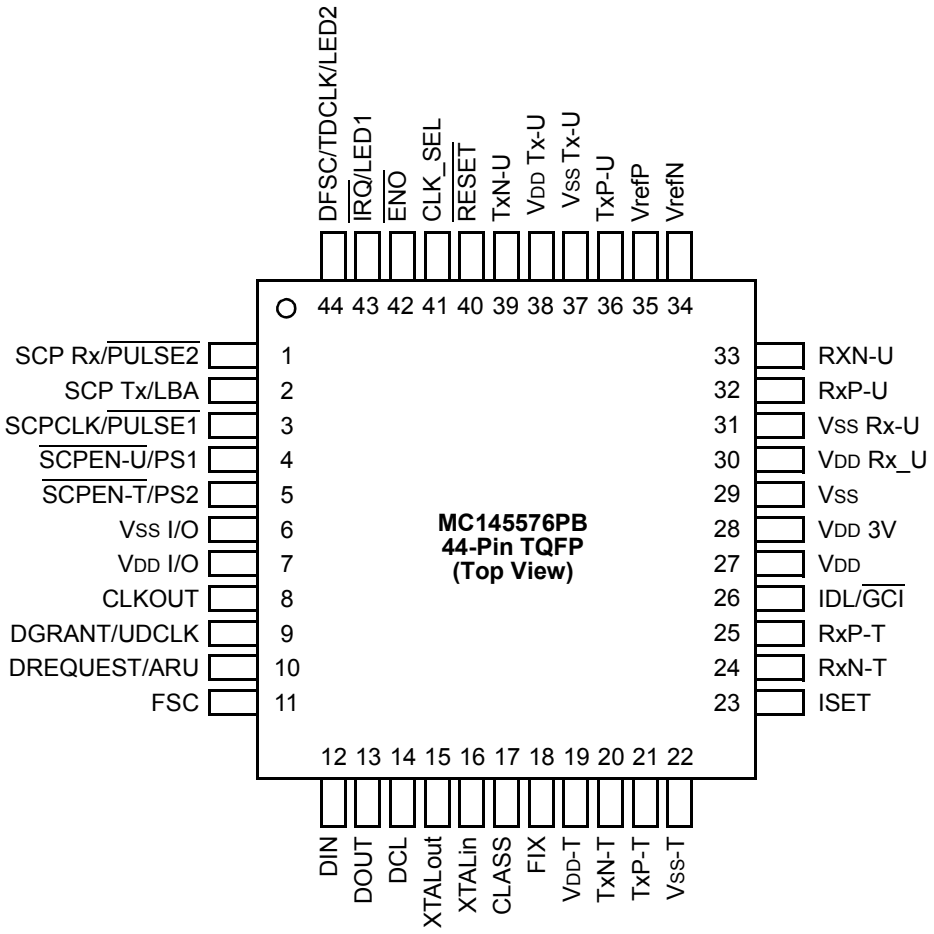



**Figure 3-1.** MC145576 Pinout Drawing

revised 8/28/1998

## 3.2 Signal Descriptions

The connections to the MC145576 are organized into six functional groupings, as shown in **Table 3-1** and illustrated in **Figure 3-2**.

**Table 3-1.** MC145576 Functional Signal Groupings

| Functional Group | No. of Signals | Reference Table |
|---|---|---|
| Power Supply | 11 | **Table 3-2** |
| Phase Lock Loop (PLL) and Clock | 2 | **Table 3-3** |
| Mode Select | 5 | **Table 3-4** |
| Time Division Multiplex (TDM) Data Interface | 4 | **Table 3-5** |
| Digital Data Interface | 11 | **Table 3-6** |
| Line Interface | 11 | **Table 3-10** |

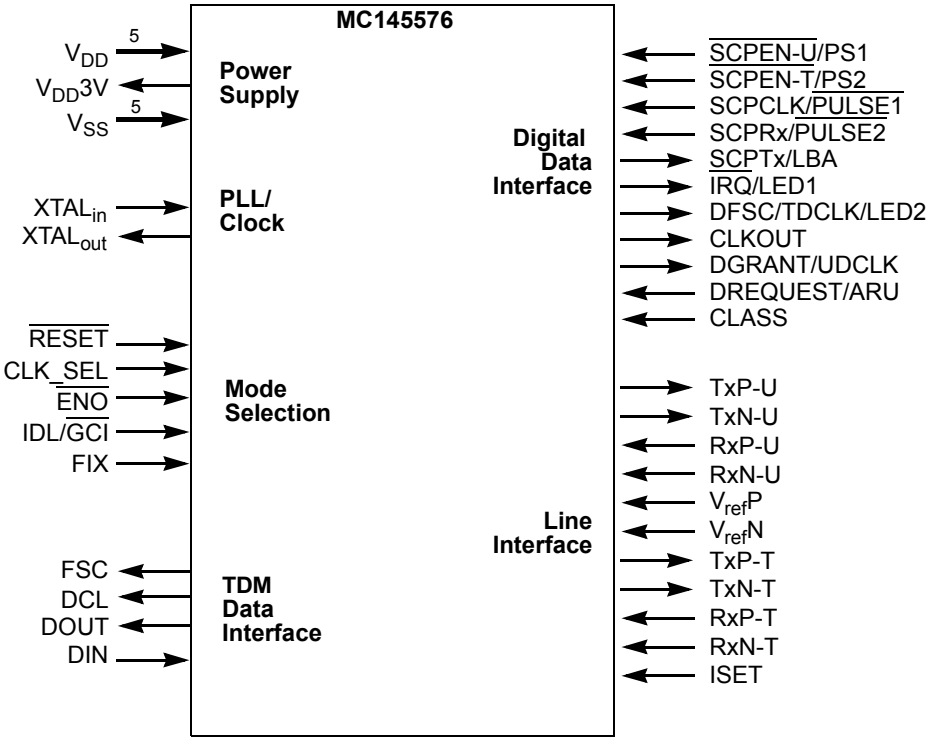



**Figure 3-2.** Signals Identified by Functional Group

### 3.2.1 Power Supply

The MC145576 has five pairs of $V_{DD}$ and $V_{SS}$ power supply pins. Each pair provides power to a specific portion of the integrated circuit to minimize interaction between the various high performance subsystems on the device. All of the negative power supply pins should be connected to the same ground reference point and all of the positive power supply pins should be connected to the same +5 V power supply source. The MC145576 also provides a 3 V output $V_{DD}$ generated by an internal voltage regulator.

**Table 3-2.** Power Supply Pins

| Signal Name | Pin No. TQFP | Pin Description |
|---|---|---|
| $V_{DD}$ | 27 | **Positive Power Supply (nominally +5 V)** — Connect $V_{DD}$ to +5 V. $V_{DD}$ provides power to the internal digital circuits of the device. Decouple $V_{DD}$ with a 0.1 µF ceramic capacitor to $V_{SS}$. |
| $V_{SS}$ | 29 | **Negative Power Supply (nominally 0 V)** — Connect $V_{SS}$ to ground. $V_{SS}$ provides a ground reference for the internal digital circuits of the device. Decouple with separate 0.1 µF ceramic capacitors connected to $V_{DD}$. |
| $V_{DD}$ Rx-U, $V_{DD}$ Tx-U | 30, 38 | **Positive Power Supply for U-Interface Analog Circuits (nominally +5 V)** — Connect $V_{DD}$ Rx-U and $V_{DD}$ Tx-U to +5 V. These pins provide power to the analog U-Interface receive and transmit subsystems in the MC145576. Decouple each with separate 0.1 µF ceramic capacitors connected to VSS Rx-U and VSS Tx-U, respectively. These two pins are not tied together internally. |
| $V_{SS}$ Rx-U, $V_{SS}$ Tx-U | 31, 37 | **Negative Power Supply for U-Interface Analog Circuits (nominally 0 V)** — Connect $V_{SS}$ Rx-U and $V_{DD}$ Tx-U to ground. These pins provide a ground reference to the U-Interface analog receive and transmit subsystems. Decouple each with separate 0.1 µF ceramic capacitors to $V_{DD}$ Rx-U and $V_{DD}$ Tx-U, respectively. |
| $V_{DD}$-T | 19 | **Positive Power Supply for the S/T-Interface Analog Circuits (nominally +5 V)** — Connect $V_{DD}$-T to +5 V. This pin provides power to the S/T-Interface analog subsystem in the MC145576. Decouple $V_{DD}$-T with separate 0.1 µF ceramic capacitors to $V_{SS}$-T. |
| $V_{SS}$-T | 22 | **Negative Power Supply for the S/T-Interface Analog Circuits (nominally 0 V)** — Connect $V_{SS}$-T to ground. This pin provides a ground reference to the S/T-Interface analog subsystem. Decouple with separate 0.1 µF ceramic capacitors connected to $V_{DD}$-T. |
| $V_{DD}$ I/O | 7 | **Positive Power Supply for Input and Output Circuits (nominally +5 V)** — Connect $V_{DD}$ I/O to +5 V or +3 V (for 3V I/O interface compatibility). This pin provides power to the digital input and output circuits of the device. Decouple with a 0.1 µF ceramic capacitor connected to $V_{SS}$ I/O. |
| $V_{SS}$ I/O | 6 | **Negative Power Supply for Input and Output Circuits, (nominally 0 V)** — Connect $V_{SS}$ I/O to ground. This pin provides a ground reference to the digital input and output circuits of the device. Decouple with separate 0.1 µF ceramic capacitors connected to $V_{DD}$ I/O. |
| $V_{DD}$3V | 28 | **Output from the Internal 3 V Regulator** — $V_{DD}$3V is the 3 V regulated supply output used to power the internal digital circuitry. Connect an external 1.0 µF decoupling capacitor between this pin and ground.<br>**CAUTION:** Do NOT connect $V_{DD}$3V to $V_{DD}$ I/O for 3 V interface compatibility. |

### 3.2.2 Phase Lock Loop and Clock Pins

A 20.48 MHz pullable crystal is connected between $XTAL_{in}$ and $XTAL_{out}$ to form a voltage–controlled crystal oscillator. No other external components are required.

**Table 3-3.** Phase Lock Loop and Clock Pins

| Pin Name | Pin No. TQFP | Pin Description |
|---|---|---|
| $XTAL_{in}$, $XTAL_{out}$ | 16, 15 | **Crystal Input/Output**—Input and output signals of the 20.48 MHz crystal oscillator amplifier. Detailed specifications for the crystal are listed in **Appendix B.2.1**. |

### 3.2.3 Mode Selection Pins

These inputs define the mode of operation for the MC145576.

**Table 3-4.** Mode Selection Pins

| Signal Name | Pin No. TQFP | Pin Description |
|---|---|---|
| $\overline{\text{RESET}}$ | 40 | **Hardware Reset**—A logic 0 applied to this Schmitt trigger input pin holds the device in a hardware reset condition. A logic 1 puts the device into the normal operating state. Register NR0(3) provides a similar software reset function, thereby allowing control of this mode from the external microcontroller.<br>**Note:** A 20.48 MHz clock must be applied to the MC145576 when $\overline{\text{RESET}}$ is asserted.<br>During a hardware reset condition, all Serial Control Port Registers are reset to their default state, and the signals output from the DCL and FSC pins are halted. In addition, the Tx Driver is put into a low impedance state to terminate the U–Interface part and the 2B1Q receiver is unable to detect the activation wake–up tone. $\overline{\text{RESET}}$ must be asserted low for at least six 20.48 MHz clock periods. |
| CLK_SEL | 41 | **DCL Input Select**—This pin is used to select the clock frequency of the IDL/GCI Interface of the MC145576. Pulling the signal high selects 2.048 MHz clock frequency; pulling it low selects 512 kHz.<br>**Note:** When $\overline{\text{ENO}}$ = 1, this input is disabled and can be left unconnected. |

**Table 3-4.** Mode Selection Pins (Continued)

| Signal Name | Pin No. TQFP | Pin Description |
|---|---|---|
| $\overline{\text{ENO}}$ | 42 | **Enable Digital Outputs**—A logic low on this pin enables all the digital inputs and outputs. In a simple NT1 application where no terminal interface is required and where the minimum possible power consumption is desired, a logic high on this pin disables certain specified digital outputs, placing them in a High-Impedance state and also disables certain digital inputs which can be left unconnected (i.e., floating), as follows:<br>• CLK_SEL, CLKOUT, DGRANT, GCI_LBA, DREQUEST/ AR-U, FSC, DIN, DOUT, DCL, and CLASS are disabled.<br>• GCI_PULSE1, GCI_PULSE2, GCI_PS1, GCI_PS2, GCI_LED1, GCI_LED2, FIX, and IDL/GCI remain active. |
| IDL/$\overline{\text{GCI}}$ | 26 | **IDL/SCP versus GCI Mode Select**—This pin controls the mode of operation of the System Interface. A logic high applied to this pin selects the (IDL+SCP) mode of operation. Pulling the signal low selects the GCI time division bus mode. In GCI mode 2B+D data and control/status information is interfaced to the MC145576 by a single four signal time division multiplexed bus. The SCP interface is not used and those pins are redefined.<br>**Note:** When $\overline{\text{ENO}}$ = 1, this input remains active. |
| FIX | 18 | **Fixed Timing Select**—This input signal allows the selection of the fixed (pulled high) or adaptive timing (pulled low) mode used by the S/T-Interface circuitry as the timing recovery method used by the transceiver's demodulator to sample the incoming transmission from the TE/TEs.<br>• In adaptive timing mode, a Digital Phase Lock Loop (DPLL) is used to position the demodulator clock optimally relative to the incoming baud from the S/T-Interface part.<br>• In fixed timing mode, the demodulator clock is maintained at a fixed position relative to the transmitted baud from the MC145576.<br>**Note:** When $\overline{\text{ENO}}$ = 1, this input remains active. |

### 3.2.4 Time Division Multiplex Data Interface Pins

This section describes the Time Division Multiplex (TDM) data interface pins.

**Table 3-5.** Time Division Multiplex Interface Pins

| Signal Name (by mode) | | Pin No. TQFP | Pin Description |
|---|---|---|---|
| IDL/ GCI TDM / MULTIPLEX | TSA | | |
| FSC | FSC | 11 | **Frame Synchronization**—FSC is the 8 kHz frame sync output for the TDM interface data transfers. The signal is phase-locked to the signal received by the U–Interface part of the MC145576.<br>• In IDL mode, the signal at this pin is high for one cycle of the DCL signal and is rising edge aligned with the rising edge of the DCL signal.<br>• In GCI mode, the signal is high for two cycles of the DCL signal and the rising edge is aligned with the rising edge of the DCL signal. FSC indicates a superframe boundary by going high for one DCL clock. This happens once every 12 ms.<br>**Note:** When $\overline{\text{ENO}}$ = 1, this output is in High impedance state. |
| DCL | DCL | 14 | **Data Clock Output**—DCL is the output bit clock for the IDL interface or 2 times bit clock for the GCI Interface. The signal provides one of two clock outputs (i.e., 2.048 MHz or 512 kHz), selected by CLK_SEL. Recovered timing is conveyed by adjusting the width of the clock. The adjustment is made by the internal digital PLL and occurs during two consecutive 8 kHz frames once per U-Interface basic frame. The adjustment consists of adding or subtracting a single 20.48 MHz clock period during the high time of DCL. Since this occurs during two consecutive 8 kHz frames, the total adjustment is ± 97 ns once every basic frame. See electrical specifications for the locations of the timing adjustment.<br>**Note:** When $\overline{\text{ENO}}$ = 1, this output is in High impedance state. |
| DOUT | DOUT | 13 | **Serial Data Out (IDL/GCI)**—The formatting of the data is mode dependent. Refer to **Section 4** for more information. In GCI mode, DOUT is an open drain output and must be connected to VDD I/O through a 5 kΩ pullup resistor.<br>**Note:** When $\overline{\text{ENO}}$ = 1, this output is in High impedance state. |

**Table 3-5.** Time Division Multiplex Interface Pins (Continued)

| Signal Name (by mode) | | Pin No. TQFP | Pin Description |
|---|---|---|---|
| IDL/ GCI TDM / MULTIPLEX | TSA | | |
| DIN | DIN | 12 | **Serial Data In (IDL/GCI)**—The formatting of the data is mode dependent. Refer to **Section 4** for more information. In GCI mode, DIN must be connected to $V_{DD}$ I/O through a pullup resistor.<br>**Note:** When $\overline{ENO}$ = 1, this input is disabled and can be left floating. |

## 3.2.5 Digital Data Interface Pins

These pins provide a digital transfer interface for the MC145576 when configured for MCU mode. In GCI mode, control and status information is provided over the GCI interface.

**Table 3-6.** Digital Data Interface Pins

| Signal Name (by mode) | | Pin No. TQFP | Pin Description |
|---|---|---|---|
| IDL/SCP | GCI | | |
| $\overline{SCPEN-U}$ (NT Terminal, TDM, TSA) | PS1 (NT Terminal, MUX) | 4 | **Serial Control Port Enable for U-Interface**—In IDL mode, when $\overline{SCPEN-U}$ is held low, this input selects the Serial Control Port (SCP) for transferring control, status, and M channel data information into and out of the U–Interface Transceiver. $\overline{SCPEN-U}$ should be held low for 8 or 16 periods of the SCPCLK signal to transfer information into or out of the MC145576. The SCP Interface disregards any operation that is not exactly 8 or 16 SCPCLK clock pulses long. If the MC145576 is the only SCP device in the system, this pin can be tied low and bursted SCP CLKs can be used to access the register.<br>**PS1**—In full GCI mode, defined when IDL/GCI = 0, this is an input pin. PS1 is transmitted in the M4 maintenance bits.<br>**Note:** When $\overline{ENO}$ = 1, this input remains active. |

**Table 3-6.** Digital Data Interface Pins (Continued)

| Signal Name (by mode) | | Pin No. TQFP | Pin Description |
|---|---|---|---|
| IDL/SCP | GCI | | |
| $\overline{\text{SCPEN-T}}$ (NT Terminal, TDM, TSA) | | 5 | **Serial Control Port Enable for S/T-Interface**—In IDL mode, when $\overline{\text{SCPEN-T}}$ is held low, this input selects the Serial Control Port (SCP) for transferring control, status, and M channel data information into and out of the S/T–Interface Transceiver. $\overline{\text{SCPEN-T}}$ should be held low for 8 or 16 periods of the SCPCLK signal to transfer information into or out of the MC145576. The SCP Interface disregards any operation that is not exactly 8 or 16 SCPCLK clock pulses long. If the MC145576 is the only SCP device in the system, this pin can be tied low and bursted SCP CLKs can be used to access the register. |
| | PS2 (NT Terminal, MUX) | | **PS2**—In full GCI mode, defined when IDL/GCI = 0, this is an input pin. PS2 is transmitted in the M4 maintenance bits.<br>**Note:** When $\overline{\text{ENO}}$ = 1, this input remains active. |
| SCPCLK (NT Terminal, TDM, TSA) | | 3 | **Serial Control Port Clock Input**—In IDL mode, this input is SCP Interface clock. Data is clocked into the MC145576 from SCP Rx on rising edges of SCPCLK. Data is shifted out of the MC145576 SCP Tx pin on falling edges of SCPCLK. SCPCLK can be any frequency from 0 up to 4.096 MHz. An SCP transaction takes place when $\overline{\text{SCPEN}}$ is brought low. |
| | $\overline{\text{PULSE1}}$ (NT Terminal, MUX) | | **Test Pulse 1**—In full GCI mode, defined when IDL/GCI = 0, $\overline{\text{PULSE1}}$ and $\overline{\text{PULSE2}}$ control the test pulses transmitted by the U and S/T-Interfaces. See **Table 3-8** for more information.<br>**Note:** When $\overline{\text{ENO}}$ = 1, this output remains active. |

**Table 3-6.** Digital Data Interface Pins (Continued)

| Signal Name (by mode) | | Pin No. TQFP | Pin Description |
|---|---|---|---|
| IDL/SCP | GCI | | |
| SCP Rx (NT Terminal, TDM, TSA) | $\overline{\text{PULSE2}}$ (NT Terminal, MUX) | 1 | **Serial Control Port Receive Input**—In IDL mode, SCP Rx is used to input control, status, and M–channel data information to the device. Data is shifted into the MC145576 on rising edges of SCPCLK. SCP Rx is ignored when data is being shifted out of SCP Tx or when $\overline{\text{SCPEN}}$ is high.<br>**Test Pulse 2**—In full GCI mode, defined when IDL/GCI = 0, $\overline{\text{PULSE1}}$ and $\overline{\text{PULSE2}}$ control the test pulses transmitted by the U and S/T-Interfaces. See **Table 3-8** for more information.<br>**Note:** When $\overline{\text{ENO}}$ = 1, this output remains active. |
| SCP Tx (NT Terminal, TDM, TSA) | LBA (NT Terminal, MUX) | 2 | **Serial Control Port Transmit Output**—In IDL mode, SCP Tx is used to output control, status, and M channel data information from the MC145576. Data is shifted out of SCP Tx on the falling edge of SCPCLK, most significant bit first.<br>**Loopback Active**—In full GCI mode, defined when IDL/GCI = 0, this pin is the LoopBack Active (LBA) signal and drives the output high when a 2B+D Loopback 2 (Definition from CCITT I.603) has been activated at the S/T-Interface.<br>**Note:** When $\overline{\text{ENO}}$ = 1, this output is in High impedance state. |

**Table 3-6.** Digital Data Interface Pins (Continued)

| Signal Name (by mode) | | Pin No. TQFP | Pin Description |
|---|---|---|---|
| **IDL/SCP** | **GCI** | | |
| $\overline{\text{IRQ}}$ (NT Terminal, TDM, TSA) | | 43 | **Interrupt Request Output**—In IDL mode, $\overline{\text{IRQ}}$ is an active low, open drain output used to signal an external microcontroller that an interrupt condition exists in the MC145576. When this pin transitions low, the microcontroller should poll the status registers of the U and S/T-Interfaces to determine the reason for the interrupt. Upon clearing the interrupt condition, the pin is returned to the high–impedance state. See the description for U NR3 (**Section 5.3.1.4**) and S/T NR3 (**Section 5.4.1.4**) for descriptions of the sources of interrupt conditions. |
| | LED1 (NT Terminal, MUX) | | **LED Control 1**—In full GCI mode, defined when IDL/GCI = 0, this pin is an open drain active low output that is used to control an LED that indicates the status of the SCNT1. Refer to **Table 3-9** for a summary of the LED control values.<br>**Note:** When $\overline{\text{ENO}}$ = 1, this output remains active. |

**Table 3-6.** Digital Data Interface Pins (Continued)

| Signal Name (by mode) | | Pin No. TQFP | Pin Description |
|---|---|---|---|
| IDL/SCP | GCI | | |
| DFSC (TDM) | | 44 | **Data Frame Synchronization**—In IDL/GCI TDM/MULTIPLEX mode, this pin is an output frame sync signal that indicates the start of the data frame for the S/T-Interface part of the MC145576. Refer to **Section 4** for more information. |
| DCLK (NT Terminal) | | | **D-Channel Clock (gated)**—In IDL NT Terminal mode, this pin is the output for the D-Channel clock. |
| TDCLK (TSA) | | | **S/T-Interface D-Channel Clock (gated)**—In Time Slot Assigner Mode (enabled when the following register programming of the S/T-Interface is performed : BR12 = $90 and OR6 = $10), this pin is the output for the S/T-Interface D-channel clock. This clock is gated (i.e., available only when the D-channel is available). Refer to **Section 7.5** for more information on the TSA Mode. |
| | LED2 (NT Terminal, MUX) | | **LED Control 2**—In full GCI mode, defined when IDL/$\overline{\text{GCI}}$ = 0, this pin is an open drain active low output that is used to control an LED which indicates the status of the MC145576. Refer to **Table 3-9** for a summary of the LED control values.<br>**Note:** When $\overline{\text{ENO}}$ = 1, this output remains active. |
| CLKOUT (NT Terminal, TDM, TSA) | CLKOUT (NT Terminal, MUX) | 8 | **Clock Output**—This signal is a programmable clock output that can be used as a microprocessor clock source. The default clock frequency is 20.48 MHz. The clock frequency is register programmable via the SCP or GCI Monitor channel to provide 10.24 MHz, 5.12 MHz or disabled following (see **Table 3-7** for programming of S/T BR8(b6) and BR8(b5) values). CLKOUT is also under control of the $\overline{\text{ENO}}$ signal.<br>**Notes: 1.** When $\overline{\text{ENO}}$ = 1, this output is in High impedance state.<br>**2.** During a hardware reset (i.e., $\overline{\text{RESET}}$ is low), CLKOUT outputs a 20.48 MHz clock. |

**Table 3-6.** Digital Data Interface Pins (Continued)

| Signal Name (by mode) | | Pin No. TQFP | Pin Description |
|---|---|---|---|
| **IDL/SCP** | **GCI** | | |
| DGRANT<br>(NT Terminal)<br><br>UDCLK<br>(TSA)<br><br>**Note:** Not used for TDM. | DGRANT<br>(NT Terminal)<br><br>**Note:** Not used for MUX. | 9 | **D-channel Access Granted**—In NT Terminal mode, DGRANT indicates that access to D-Channel has been granted. Refer to **Section 4** for more information.<br>**U-Interface D-channel Clock (gated)**—In Time Slot Assigner Mode (enabled when the following register configuration of the S/T-Interface is enabled : BR12 = $90 and OR6 = $10), this pin is the output for the U-Interface D-channel clock. UDCLK is gated (i.e., available only when the D-channel is available).<br>**Note:** When $\overline{\text{ENO}}$= 1, this output is in High impedance state. |
| DREQUEST/<br>ARU<br>(NT Terminal)<br><br>ARU<br>(TDM, TSA) | DREQUEST/<br>ARU<br>(NT Terminal)<br><br>ARU (MUX) | 10 | **D-Channel Access Request**—In NT Terminal mode, a logic high on this pin allows the MC145576 to attempt to gain D-Channel access for the NT terminal.<br>**U-Interface Activate Request**—When the MC145576 is deactivated, a logic high on ARU causes the U-Interface to transmit a TN/SN1 activation signal to the LT (AR-U Activate Request). The LT then responds to this request and fully activates the MC145576. The ARU operation can be disabled by writing a 1 to S/T-Interface BR12 (b5).<br>**Note:** When $\overline{\text{ENO}}$ = 1, this output is disabled and can be left floating. |

**Table 3-6.** Digital Data Interface Pins (Continued)

| Signal Name (by mode) | | Pin No. TQFP | Pin Description |
|---|---|---|---|
| IDL/SCP | GCI | | |
| CLASS<br>(NT Terminal)<br><br>**Note:** Not used for TDM or TSA. | CLASS<br>(NT Terminal)<br><br>**Note:** Not used for MUX. | 17 | **Message Priority Class**—In NT Terminal mode of operation, the CLASS input allows the selection of the message priority class by logically ORing it internally with S/T Register NR2(b 0). The output of this internal OR gate determines the class of the transceiver for D channel operation. If CLASS is held low, the class selection is determined by the value of NR2(b0). If an application needs to change the class of the MC145576 without a register access, then NR2(b0) should be 0 to allow the class to be selected via the CLASS pin. When the output of the internal OR gate is 0, the priority class for D channel messages sent by the device is set to the signalling or highest priority class (i.e., Class 1 operation). When the output of the internal OR gate is 1, Class 2 operation is selected. The definition and functionality of the class configuration of the MC145576 is fully compliant with CCITT I.430 and ANSI T1.605.<br>**Note:** When $\overline{\text{ENO}}$= 1, this output is disabled and can be left floating. |

**Table 3-7.** CLKOUT Values

| S/T BR8(b6) | S/T BR8(b5) | CLKOUT |
|---|---|---|
| 0 | 0 | 20.48 MHz |
| 0 | 1 | 10.24 MHz |
| 1 | 0 | 5.12 MHz |
| 1 | 1 | 0 MHz |

**Table 3-8.** Test Pulses

| $\overline{\text{PULSE1}}$ | $\overline{\text{PULSE2}}$ | S/T-Interface | U-Interface |
|---|---|---|---|
| 1 | 1 | Normal Mode | Normal Mode |
| 0 | 1 | Single Pulse | Single Pulse |
| 1 | 0 | 96 kHz tone | Force free running SN2 |
| 0 | 0 | Reserved | Force SN0 |

**Table 3-9.** LED Control Combinations

| GCI_LED1 | GCI_LED2 | Indication |
|---|---|---|
| Off | Off | Deactivated |
| Flash (1 Hz) | Off | Activation in progress or U-only activation |
| On | Flash (1 Hz) | U-Interface active, S/T-Interface not active (in progress or there is a problem activating the S/T-Interface) |
| On | Off | Fully Active (S/T and U) |
| Off | On | Error Indication (see note) |
| On | On | Pulse Test Mode |
| Flash (1 Hz) | Flash (1 Hz) | 2B+D Loopback |

**Note:** This state is indicated for 1 s before the MC145576 goes into an automatic reset.

### 3.2.6 Line Interface Pins

These pins form the Line Interface of the MC145576 Transceiver, including the 2B1Q part as well as line interface with the TE/TEs. Refer to **Section 4.2** for additional information on the line interface.

**Table 3-10.** Line Interface Pins

| Pin Name | Pin No. TQFP | Pin Description |
|---|---|---|
| TxP-U, TxN-U | 36, 9 | **Transmit Positive and Transmit Negative Outputs of U-Interface**—These signals are the positive and negative outputs of the differential transmit driver of the U-Transceiver (2B1Q interface). |
| RxP-U, RxN-U | 32, 33 | **Receive Positive and Receive Negative Inputs of U-Interface**—These signals are the positive and negative inputs to the differential receive circuit of the U-Transceiver (2B1Q interface). |
| $V_{ref}P$, $V_{ref}N$ | 35, 34 | **Reference Voltage Positive and Reference Voltage Negative**—These positive and negative signals are used for internal voltage reference. Connect a 0.1 µF ceramic capacitor between $V_{ref}P$ and $V_{ref}N$. |
| TxP-T, TxN-T | 21, 20 | **Transmit Positive and Transmit Negative Outputs of S/T-Interface**—These signals are the differential analog outputs to the S/T transmit line driver. |
| RxP-T, RxN-T | 25, 24 | **Receive Positive and Receive Negative Inputs of S/T-Interface**—These signals are the differential analog inputs to the S/T receiver. |

**Table 3-10.** Line Interface Pins (Continued)

| Pin Name | Pin No. TQFP | Pin Description |
|---|---|---|
| ISET | 23 | **ISET** – This pin performs the ISET function and should have an external resistor connected to ground. A current programming reference resistor of value 30 kΩ accurate to 5% should be connected between ISET and $V_{SS}$ -T. This resistor provides biasing and programs the current limit for the TxP-T and TxN-T driver circuits.<br>**Note:** This resistor is not user programmable and must be 30 kΩ for CCITT I.430 and ANSI T1.605 compatibility. |

# 4

# Modes of Operation

## 4.1 Introduction

Different types of configurations and digital accesses allow the MC145576 to be used in various applications.

## 4.2 Standard NT1 Operation

When configured in GCI mode (IDL/$\overline{\text{GCI}}$ pulled low) and digital access disabled ($\overline{\text{ENO}}$ pulled high), the MC145576 operates as a standalone NT1 (see **Figure 4-1**).

Several pins are still available to provide:

- Indication of the MC145576 state (LED1 and LED2)
- Configuration of the S/T bus (FIX)
- Generation of test pulses ($\overline{\text{PULSE1}}$ and $\overline{\text{PULSE2}}$)
- Indication of the external power supplies status (PS1 and PS2)

To reduce EMC generation, all the other digital pins are disabled.

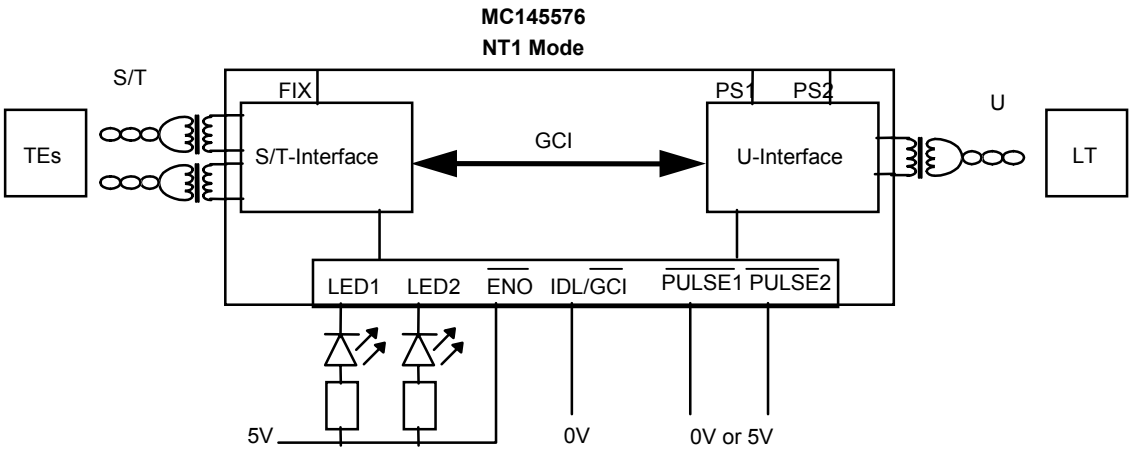



**Figure 4-1.** Standard NT1 Block Diagram

## 4.3 Smart NT1 with POTS Interface (NT1+)

The biggest advantage of the Smart NT architecture is its modularity. Depending on which 68302 microprocessor is used, the Smart NT can address one of the following different specifications:

- **Simple Smart NT based on the 68LC302**—One HDLC controller is used for the D channel and there is an optional RS-232 interface capability. The addition of a simple FPGA provides voice capability from the processor to the POTS.
- **Smart NT with simple TA capability based on 68302 (or 68PM302)**—Two HDLC controllers are used for the D channel and one B channel, and there is an RS-232 interface capability. This allows 64 Kb/s data transfer.
- **Smart NT with full TA capability based on 68QH302**—Three HDLC controllers used for the D channel and the two B channels, and there is an RS-232 interface capability. This allows up to 128 Kb/s data transfer.

Because the MC145576 can be configured for 3 V digital signals, power consumption of the Smart NT can be decreased by using 3 V parts (processor, codecs, etc.).

### 4.3.1 Architecture

Combining the MC145576 with a multiprotocol controller of the MC68302 family, one or two MC145484 PCM codecs and one or two analog line interfaces (SLIC), provides an optimal Smart NT1 architecture. This architecture can use either the IDL/SCP (**Figure 4-2**) or GCI (**Figure 4-3**) digital bus. Motorola recommends the use of the IDL/SCP mode of interconnection between all the parts, because it provides better flexibility for the architecture improvements.

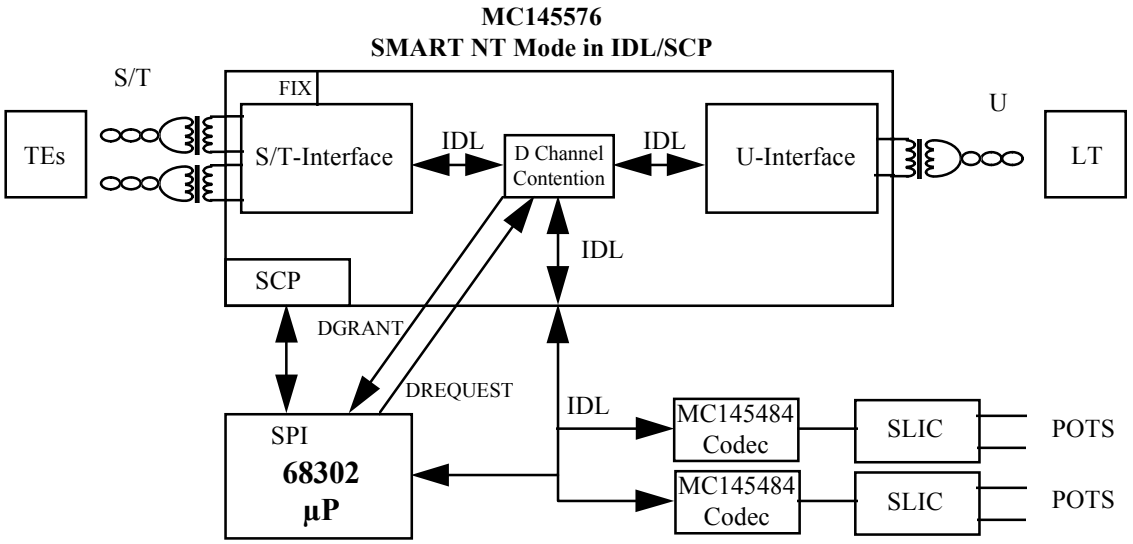



**Figure 4-2.** IDL/SCP based Smart NT Block Diagram

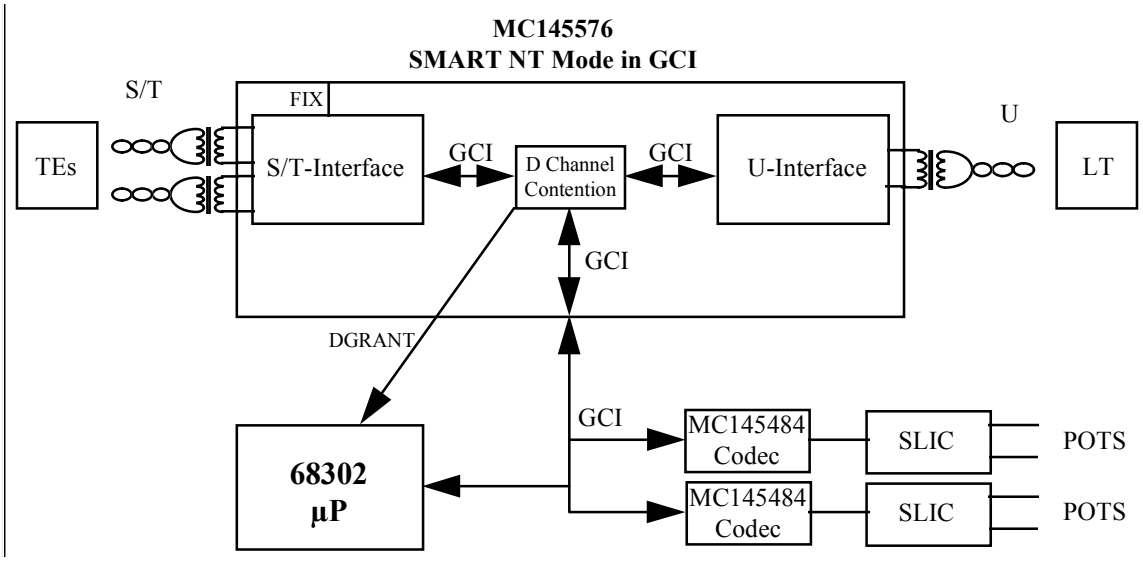



**Figure 4-3.** GCI based Smart NT Block Diagram

## 4.3.2 Configuration

In Smart NT mode of operation, configure the MC145576 in NT Terminal mode. This mode provides the D channel contention capability between the D channel coming from the processor and the D channel coming from the TEs.

For more details on this configuration, refer to **Section 7** (IDL mode) or **Section 8** (GCI mode).

## 4.4 MINI PABX

The Smart NT architecture can be easily adapted to a Mini PABX architecture. This allows internal calls (TE to TE, TE to POTs or POTS to POTS) without going through the Line Card (i.e., there is no need to activate the U loop).

### 4.4.1 Architecture

For this application, the MC145576 provides a digital switch that routes the B and D channels between the POTS, the S/T part, and the U part of the MC145576 (**Figure 4-4**).

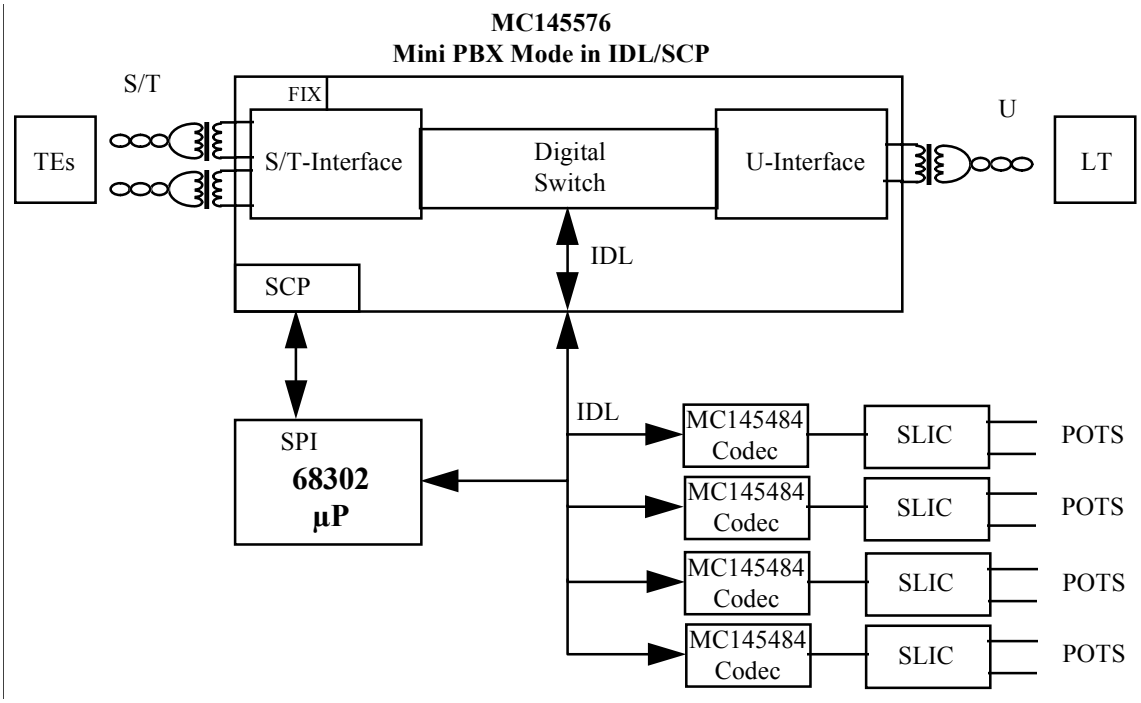



**Figure 4-4.** Mini PABX Block Diagram

Two HDLC controllers are required to process the D channel coming from the TEs and the D channel coming from the Central Office (the D channel contention circuitry is disabled). The Mini PABX can handle up to four simultaneous calls with a maximum of two external calls (i.e., calls through the Central Office).

### 4.4.2 Configuration

In Mini PABX mode of operation, configure the MC145576 in IDL Time Slot Assigner mode. This mode provides the switching capability required for communication between all the connections of the board (i.e., TEs, POTS, and Central Office).

For more details on this configuration, refer to **Section 7** (IDL mode).

## 4.5 U-Interface Terminal Adaptor

For Terminal connection to the U-interface, the S/T part of the MC145576 can be configured in Absolute Power Down mode. This allows the processor direct access to the U-interface.

### 4.5.1 Architecture

This architecture can use the IDL/SCP (**Figure 4-5**) or GCI (**Figure 4-6**) digital bus.

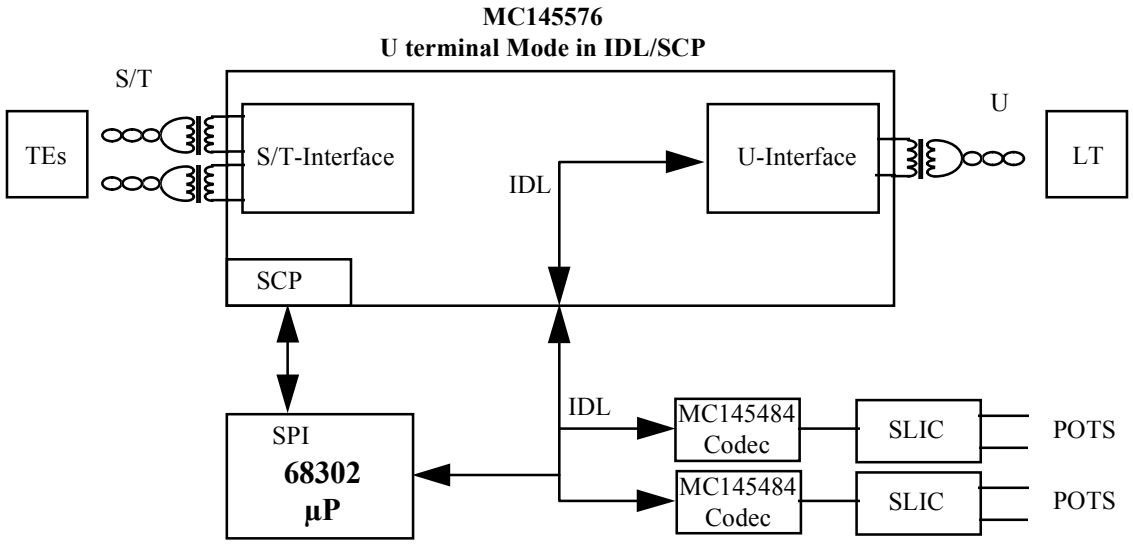



**Figure 4-5.** IDL/SCP-based Terminal U Block Diagram

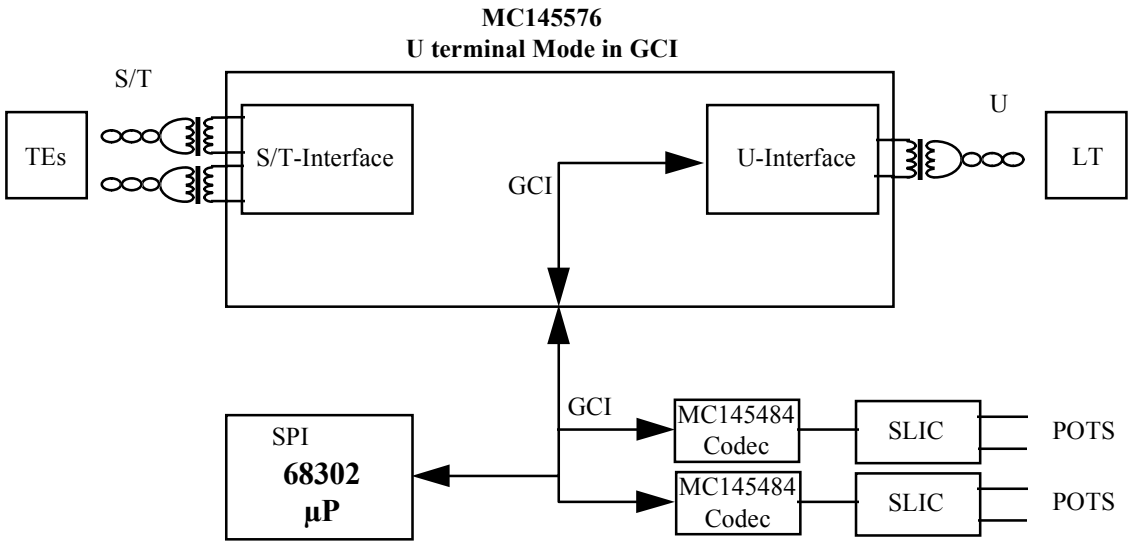



**Figure 4-6.** GCI-based Terminal U Block Diagram

If the S/T-interface is required, then the MC145576 can be reconfigured to operate in Smart NT mode. Connections between the MC145576 and the processor are identical in Smart NT mode and in U Terminal mode.

### 4.5.2 Configuration

In U Terminal mode of operation, configure the MC145576 in TDM mode. In this mode, the S/T and the U part of the MC145576 are completly separated (no direct 2B+D data connection). So, the S/T part can be switched into Absolute Power Down mode without affecting the U part.

For more details on this configuration, refer to **Section 7** (IDL mode) or **Section 8** (GCI mode).

# 5

# Register Description Reference

## 5.1 Introduction

This section describes the MC145576 internal registers.

## 5.2 Registers Description

The MC145576 registers are divided into two basic groups, each of which support their respective interface (U or S/T). The register groups are:

- U Interface Registers:
  - U Nibble Registers
  - U R6 Register
  - U Byte Registers
  - U Overlay Registers
- S/T Interface Registers:
  - S/T Nibble Registers
  - S/T Byte Registers
  - S/T Overlay Registers

The MC145576 registers are accessible externally through the SCP bus in IDL/SCP mode of operation or through the Monitor Channel in GCI mode of operation. Most register functions are available in both modes of operation, but for those which are not, the register function is indicated as follows:

- Register functions available in SCP/IDL mode only are shown in *italic* (e.g., *Software Reset)*
- Register functions available in GCI only are shown in **bold** (e.g., **Stop/Go Disabled**)

Each bit described in the following sections is identified with a read/write indicator, shown in the lower right corner of the each bit name cell in the register layout diagram.

**Table 5-1.** Bit Read/Write Indicator

| Indicator | Type | Description |
|---|---|---|
| rw | Read/Write | The external microcontroller can write to a Read/Write bit and read back the written data. |
| ro | Read Only | The external microcontroller may only read a Read Only bit. Writing to it has no effect unless specified differently in the bit description. Setting or clearing a Read Only bit is an internal operation. |
| ro/wo | Read Only/ Write Only | The external microcontroller may write to a Read Only/Write Only bit, but the value the microcontroller reads back is not necessarily the value it wrote. This type of bit is set and cleared by some internal operations. |

## 5.3 U-Interface Registers

These registers are situated in the U-Interface portion of the MC145576 and are almost exclusively relevant to the operation of the U-Interface.

### 5.3.1 U Nibble Registers

The U Nibble Registers are a set of six 4-bit control and status registers used with the U-Interface. **Figure 5-1** lists the registers along with bit names and default settings after reset.

| Register | b3 | b2 | b1 | b0 | Value after Reset |
|---|---|---|---|---|---|
| NR0 | *Software Reset* | *Power Down enable* | Reserved | *Return to Normal* | $0 |
| NR1 | Linkup | Error Indication (EI) | Superframe Sync | Transparent/ Activation in progress | $0 |
| NR2 | *Activation Request (AR)* | *Deactivation Request (DR)* | Superframe Update Disable | Customer | $0 |
| NR3 | IRQ3 | IRQ2 | IRQ1 | IRQ0 | $0 |
| NR4 | IRQ3 Enable | IRQ2 Enable | IRQ1 Enable | IRQ0 Enable | $0 |
| NR5 | Reserved | Block B1 | Block B2 | Swap B1/B2 | $0 |

**Figure 5-1.** U-Interface Nibble Register Map

#### 5.3.1.1 U-Interface NR0

| b3 | b2 | b1 | b0 |
|---|---|---|---|
| *Software Reset* rw | *Power Down enable* rw | reserved | *Return to Normal* rw |

**Figure 5-2.** U-Interface NR0 Bit Definitions

**Figure 5-2** names the bit fields in NR0. These fields are defined as follows:

- **Software Reset (b3)**—This bit forces the U-Interface transceiver into a reset state. Setting this bit to 1 causes a software reset. To allow the transceiver to resume operation, this bit must be cleared by either writing a 0 to it or asserting hardware reset. Reset must be asserted for at least six 20.48 MHz clock periods. There must be a 20.48 MHz clock at $XTAL_{in}$ for the MC145576 to reset correctly. This bit has no effect on the contents of NR0 and BR10.
- **Power-Down Enable (b2)**—When this bit = 1 and the U-Interface transceiver is searching for a wake-up tone from the far-end tranceiver, the MC145576 enters the Power-Down mode. In Power-Down mode, the MC145576 transmit drivers and the time division multiplex interface circuitry for both IDL/GCI and GCI operation are turned off. This bit must be cleared to 0 before enabling the MC145576 to perform any non-activation related functions other than waiting for a wakeup tone. The MC145576 automatically exits from Power-Down mode on one of three conditions:
  - 1. A wakeup tone is detected on the U-Interface.
  - 2. The external microcontroller sets the Activation Request bit, (NR2(b3)).
  - 3. This bit is reset to 0.

  **NOTE:** When this bit is 0, the U-Interface transceiver is not permitted to enter power-down mode. The U-Interface transceiver has warm start capability regardless of the state of this bit.
- **Return to Normal (b0)**—This bit is used to return maintenance functions to their normal operating state. When set to 1, the CRC Corrupt bit (BR8(b3)) and all of the loopback control bits in BR6 are cleared.

  **NOTE:** Never modify NR0 while the device is in GCI mode. Ensure that reserved bit b1 is 0 at all times to maintain future compatibility.

### 5.3.1.2 U-Interface NR1

| b3 | b2 | b1 | b0 |
|---|---|---|---|
| Linkup<br>ro | Error Ind (EI)<br>ro | Superframe Sync<br>ro | Transparent/ Activation in progress<br>ro |

**Figure 5-3.** U-Interface NR1 Bit Definitions

**Figure 5-3** names the bit fields in NR1. These fields are defined as follows:

- **Linkup (b3)**—This bit is set when the U-Interface transceiver completes an activation up to the point where full-duplex operation of the U-Interface is established. For the ANSI T1.601-1992 defined activation to be completed, the ACT bit in the M4 maintenance bits must still be exchanged. However, from purely a transmit/receive point of view, the U-Interface is operational when Linkup is 1. Linkup remains set until one of three things happens:
  - 1. Receive framing is lost or severely in error, and remains so, for 480 ms.
  - 2. Receive framing is lost after Deactivate Request is set in NR2(b2), or Verified DEA (BR3(b1)) becomes a 1 during M4 Control mode 0,0 (BR9(b5–b4)).
  - 3. A hardware or software reset occurs.
- **Error Indication (b2)**—This bit = 1 when a timer expires. Error Indication is always automatically reset prior to the next IRQ3. This is the result of either setting the Activate Request bit in NR2(b3) or receiving a wakeup tone. Error Indication is not cleared by reading NR1. Time-out sources are:
  - 15-second Activation Timer (BR11(b0)).
  - 480-ms loss of frame/signal.
- **Superframe Sync (b1)**—This bit is a 1 when the received superframe is being reliably detected. It transitions from 0 to 1 coincident with Linkup being set. Subsequently, if the superframe is lost, Superframe Sync returns to 0, and if Superframe Sync remains 0 for 480 ms, the U-Interface transceiver deactivates. While Superframe Sync is 0, the received maintenance bits are unknown. IRQ2, IRQ1, and IRQ0 are not generated while Superframe Sync is 0. The 2B+D data is blocked (forced to all 1s) when Superframe Sync is 0.
- **Transparent/Activation in Progress (b0)**—This bit has a dual purpose. When the transceiver is deactivated, this bit is 0. Whenever an activation begins, this bit is internally set to a 1 and an IRQ3 is generated. When the activation process is completed, Linkup = 1 indicating success, and this bit remains set to 1, indicating that the receiver and Superframe Deframer are ready to pass data transparently from the U-Interface to the IDL/GCI interface. If the activation process fails, this bit is cleared and Error Indication = 1. Whenever Linkup is 1, this bit may be cleared, indicating that the receiver detected a high error on the U-Interface. Under this condition, the receiver blocks received data (forcing the 2B+D data to all 1s) until the error returns to normal. The received data is not transmitted on the IDL/GCI interface until Linkup is 1, Superframe Sync is 1, Transparent/Activation in Progress is 1, and either Customer Enable (see NR2(b0)) or Verified ACT (see BR3(b2)) is 1.

**NOTE:** When access to the D channel via register OR12 is enabled by setting BR10(b1), the operation of the NR1 status bits is modified. NR1 indicates a D channel interrupt by setting all four status bits to 1s. Reading OR12 clears the special code (1111) from NR1 but does not affect any updates in activation status. So, if there has been a change in activation status, an interrupt is still queued up even though the D channel interrupt has been cleared.

#### 5.3.1.3 U-Interface NR2

| *b3* | *b2* | *b1* | *b0* |
|---|---|---|---|
| *Activation Request (AR)* rw | *Deactivation Request (DR)* rw | Superframe Update Disable rw | Customer Enable rw |

**Figure 5-4.** U-Interface NR2 Bit Definitions

**Figure 5-4** names the bit fields in NR2. These fields are defined as follows:

- **Activation Request (b3)**—When this bit = 1 and the U-Interface is in ANSI T1.601-1992 defined Full Reset, the transceiver begins an activation. The external microcontroller never needs to set this bit to 0. The bit is internally set to 0 whenever Transparent/Activation in Progress (NR1(b0)) = 1 or on hardware or software reset. If the activation fails for any reason, the Activation Request bit must be set to 1 once again to initiate another activation attempt. The transceiver self-activates if an incoming tone is detected. Once activation starts, the MC145576 automatically clears this bit. Do not continuously reassert this bit. It only needs to be set once per activation attempt.
- **Deactivation Request (b2)**—The Deactivate Request bit is set to 1 by the external microcontroller in response to a received DEA bit on the M4 channel, which indicates to the U-Interface that this is a normal deactivation attempt. In this case, the MC145576 reactivates in the warm start mode. The MC145576 automatically clears this bit upon deactivation.
- **Superframe Update Disable (b1)**—This bit tells the Superframe Framer whether or not to update the maintenance bits M40–M47, M50, M51, and M60, which are being transmitted with the new bits that have been loaded in the control registers. In normal operation, this bit is always set to 0, allowing the transmitted bits to be updated at the transmit superframe boundary with the maintenance channel data in registers BR0 and BR2(b7–b4). The transceiver can be forced to send exactly three superframes of updated M4 channel data before it deactivates. In that sequence of operations, the Superframe Update Disable bit is first set to 1. The M4 maintenance bits are then written by the external microcontroller to the proper setting for deactivation. The Superframe Update Disable bit = 0 and the Deactivate Request bit in NR2(b2) = 1. This guarantees that the U-Interface sends exactly three superframes of updated M4 data before the activation state controller shuts everything down. Superframe Update Disable does not affect the transmitted EOC, FEBE, or CRC maintenance bits.

- **Customer Enable (b0)**—When this bit = 1, it permits the U-Interface to pass 2B+D data transparently. During the activation procedure, the Customer Enable bit normally = 0. Only after the U-Interface has reached full-duplex operation and the ACT bits of the M4 maintenance channel have been properly exchanged, should the Customer Enable bit be set to a 1. See BR9(b5–b4), M4 Control Bits, for another way to achieve 2B+D data transparency.

**NOTE:** Though NR2 is not normally written to in GCI mode, if an application requires it, ensure that bits b3 and b2 are always written as 0 while the device is in GCI mode.

#### 5.3.1.4 U-Interface NR3

| *b3* | *b2* | *b1* | *b0* |
|---|---|---|---|
| IRQ3<br>ro | IRQ2<br>ro | IRQ1<br>ro | IRQ0<br>ro |

**Figure 5-5.** U-Interface NR3 Bit Definitions

**Figure 5-5** names the bit fields in NR3. These fields are defined as follows:

- **IRQ3 (b3)**—This interrupt is set by a state change in NR1 and is cleared by reading NR1. If this bit is set by the D channel register interrupt, it is cleared once OR12 has been read, unless there has been a change in activation status.
- **IRQ2 (b2)**—This interrupt is dedicated to the EOC. Updating of the EOC buffer R6 by the Superframe Deframer sets this bit. The loading of the EOC buffer depends on its mode of operation. See BR9(b7–b6) for details about when the buffer is loaded. To clear the interrupt, it is necessary to read R6. IRQ2 is asserted at the end of the fourth and eighth basic frame of a superframe.
- **IRQ1 (b1)**—This interrupt is dedicated to the received M4 maintenance bits. This bit is set whenever the M4 buffer (BR1) is updated. Updating of the M4 buffer depends on its mode of operation. See BR9(b5–b4) for details of buffer updating. To clear the interrupt, it is necessary to read BR1. IRQ1 is asserted at the end of every superframe.
- **IRQ0 (b0)**—This interrupt is dedicated to the received M50, M51, and M60 bits from basic frames 1 and 2 buffered in BR3. Whenever these bits in BR3 are updated, this interrupt bit is set. The updating of BR3 is dependent on its mode of operation. See BR9(b3–b2) for details of when the buffer is updated. To clear the interrupt, it is necessary to read BR3. IRQ0 is asserted at the end of the fourth received basic frame of a superframe.

### 5.3.1.5 U-Interface NR4

| *b3* | *b2* | *b1* | *b0* |
|---|---|---|---|
| IRQ3 Enable<br>rw | IRQ2 Enable<br>rw | IRQ1 Enable<br>rw | IRQ0 Enable<br>rw |

**Figure 5-6.** U-Interface NR4 Bit Definitions

**Figure 5-6** names the bit fields in NR4. These fields are defined as follows:

- **IRQ3 Enable (b3)**—A 1 in this field enables IRQ3. A 0 disables the interrupt.
- **IRQ2 Enable (b2)**—A 1 in this field enables IRQ2. A 0 disables the interrupt.
- **IRQ1 Enable (b1)**—A 1 in this field enables IRQ1. A 0 disables the interrupt.
- **IRQ0 Enable (b0)**—A 1 in this field enables IRQ0. A 0 disables the interrupt.

### 5.3.1.6 U-Interface NR5

| *b3* | *b2* | *b1* | *b0* |
|---|---|---|---|
| Reserved | Block B1<br>rw | Block B2<br>rw | Swap B1/B2<br>rw |

**Figure 5-7.** U-Interface NR5 Bit Definitions

**Figure 5-7** names the bit fields in NR5. These fields are defined as follows:

- **Block B1 (b2)**—When this bit is 1 and the IDL/GCI Invert (BR7(b4)) is 0, the B1 channel is forced to transmit 1s on the IDL/GCI interface. When IDL/GCI Invert (BR7(b4)) is 1, 0s are transmitted in the B1 timeslot. Data received on the B1 channel from the IDL/GCI interface is still transmitted normally through the U-Interface. The B1 designator on this bit always refers to the IDL/GCI interface. Therefore, even if bit Swap B1/B2 (NR5(b0)) is 1, data in the first B channel timeslot on the IDL/GCI interface is the data that is blocked.
- **Block B2 (b1)**—When this bit is 1 and the IDL/GCI Invert (BR7(b4)) is 0, the B1 channel is forced to transmit 1s on the IDL/GCI interface. When IDL/GCI Invert (BR7(b4)) is 1, 0s are transmitted in the B2 timeslot. Data received on the B2 channel from the IDL/GCI interface is still transmitted normally out of the U-Interface. The B2 designator on this bit always refers to the IDL/GCI interface. Therefore, even if bit Swap B1/B2 (NR5(b0)) is 1, data in the second B channel timeslot on the IDL/GCI interface is the data that is blocked.
- **Swap B1/B2 (b0)**—When this bit is 1, the IDL/GCI interface performs a swap of the B channels from the U-Interface to the IDL/GCI interface and from the IDL/GCI interface to the U-Interface.

**NOTE:** Ensure that reserved bit b3 is 0 at all times to maintain future compatibility.

## 5.3.2 U-Interface R6 Register

| *b11* | *b10* | *b9* | *b8* | *b7* | *b6* | *b5* | *b4* | *b3* | *b2* | *b1* | *b0* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| EOC a1 ro/wo | EOC a2 ro/wo | EOC a3 ro/wo | EOC dm ro/wo | EOC i1 ro/wo | EOC i2 ro/wo | EOC i3 ro/wo | EOC i4 ro/wo | EOC i5 ro/wo | EOC i6 ro/wo | EOC i7 ro/wo | EOC i8 ro/wo |

**Figure 5-8.** U-Interface R6 Register Bit Definitions

As shown in **Figure 5-8**, this register is 12 bits long to match the length of the EOC message. This register is double buffered for read and write operations. Refer to **Figure 5-9** and **Figure 5-10** to see how the EOC bits in this register map to the superframe. Operation of R6 depends on the setting of the EOC control bits in BR9(b7–b6) and BR14(b6).

- **BR14(b6) = 0 (Default mode)**—R6 performs as a read-only/write-only register. Data read from R6 by the external microcontroller is the EOC message that the Superframe Defframer stores according to the EOC Control register (BR9(b7–b6)). Data written to R6 is stored in a latch contained in the Superframe Framer and is subsequently transmitted beginning on the next transmit EOC frame boundary. The Superframe Framer latches are set to 1s on hardware or software resets. The Superframe Update Disable register, NR2(b1), has no effect on this register.
- **BR14(b6) = 1**—The Superframe Framer register that contains the transmit EOC message bits becomes a read/write register. Therefore, the data that is written to the Superframe Framer may be read back through R6. In this mode, the received EOC message is not available.

| | Framing | 2B+D | Overhead Bits (M1–M6) | | | | | |
|---|---|---|---|---|---|---|---|---|
| QUAT Positions | 1–9 | 10–117 | 118s | 118m | 119s | 119m | 120s | 120m |
| Bit Positions | 1–18 | 19–234 | 235 | 236 | 237 | 238 | 239 | 240 |
| Basic Frame # | Sync Word | 2B+D | M1 | M2 | M3 | M4 | M5 | M6 |
| 1 | ISW | 12 x 2B+D | EOC a1 | EOC a2 | EOC a3 | ACT | 1 | 1 |
| 2 | SW | 12 x 2B+D | EOC dm | EOC i1 | EOC i2 | DEA | 1 | FEBE |
| 3 | SW | 12 x 2B+D | EOC i3 | EOC i4 | EOC i5 | SCO | CRC1 | CRC2 |
| 4 | SW | 12 x 2B+D | EOC i6 | EOC i7 | EOC i8 | 1 | CRC3 | CRC4 |
| 5 | SW | 12 x 2B+D | EOC a1 | EOC a2 | EOC a3 | 1 | CRC5 | CRC6 |
| 6 | SW | 12 x 2B+D | EOC dm | EOC i1 | EOC i2 | 1 | CRC7 | CRC8 |
| 7 | SW | 12 x 2B+D | EOC i3 | EOC i4 | EOC i5 | UOA | CRC9 | CRC10 |
| 8 | SW | 12 x 2B+D | EOC i6 | EOC i7 | EOC i8 | AIB | CRC11 | CRC12 |

ACT = start up bit (0 during start up)
AIB = Alarm Indication Bit (0 indicates interruption)
CRC = Cyclic Redundancy Check: covers 2B?+?D + M4
DEA = turn off bit (0 indicates turn off)
SCO = 0 start on command only
EOC = embedded operations channel
a = address bit
dm = data/message indicator (0 = data, 1 = message)
FEBE = Far-End Block Error
UOA = U-only-activation
1 = reserved bit for future standard

**Figure 5-9.** Register Bit Locations Within the Superframe LT → NT

| | Framing | 2B+D | Overhead Bits (M1–M6) | | | | | |
|---|---|---|---|---|---|---|---|---|
| QUAT Positions | 1–9 | 10–117 | 118s | 118m | 119s | 119m | 120s | 120m |
| Bit Positions | 1–18 | 19–234 | 235 | 236 | 237 | 238 | 239 | 240 |
| Basic Frame # | Sync Word | 2B+D | M1 | M2 | M3 | M4 | M5 | M6 |
| 1 | ISW | 12 x 2B+D | EOC a1 | EOC a2 | EOC a3 | ACT | 1 | 1 |
| 2 | SW | 12 x 2B+D | EOC dm | EOC i1 | EOC i2 | PS1 | 1 | FEBE |
| 3 | SW | 12 x 2B+D | EOC i3 | EOC i4 | EOC i5 | PS2 | CRC1 | CRC2 |
| 4 | SW | 12 x 2B+D | EOC i6 | EOC i7 | EOC i8 | NTM | CRC3 | CRC4 |
| 5 | SW | 12 x 2B+D | EOC a1 | EOC a2 | EOC a3 | CSO | CRC5 | CRC6 |
| 6 | SW | 12 x 2B+D | EOC dm | EOC i1 | EOC i2 | 1 | CRC7 | CRC8 |
| 7 | SW | 12 x 2B+D | EOC i3 | EOC i4 | EOC i5 | SAI | CRC9 | CRC10 |
| 8 | SW | 12 x 2B+D | EOC i6 | EOC i7 | EOC i8 | NIB | CRC11 | CRC12 |

ACT = start up bit (0 during start up)
CRC = cyclic redundancy check: covers 2B+D + M4
CSO = Cold Start Only (1 for cold start only)
EOC = embedded operations channel
a = Address bit
dm = data/message indicator (0 = data, 1 = message)
FEBE = Far-End Block Error
NTM = NT in Test Mode bit (set = 0 to indicate test mode)
PS1, PS2 = power status bits, (set = 0 to indicate power problems)
SAI = S-activation indicator bit (optional, 1 for S/T activity)
NIB = Network Indicator Bit
1 = reserved bit for future standard

**Figure 5-10.** Register Bit Locations Within the Superframe NT → LT

### 5.3.3 U Byte Registers

The U Byte Registers are a set of sixteen 8-bit registers used with the U Interface. **Table 5-11** lists the registers along with bit names and default settings after reset.

| Reg. | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Value after Reset | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | IDL/ SCP | GCI |
| BR0 | M40 | M41 | M42 | M43 | M44 | M45 | M46 | M47 | $FF | $F7 |
| BR1 | M40 | M41 | M42 | M43 | M44 | M45 | M46 | M47 | $3F | $FF |
| BR2 | M50 | M60 | M51 | FEBE input | reserved | reserved | reserved | reserved | $FF | $FF |
| BR3 | M50 | M60 | M51 | received FEBE | computed FEBE | verified ACT | verified DEA | superframe detect | $E0 | $F0 |
| BR4 | FEBE counter 7 | FEBE counter 6 | FEBE counter 5 | FEBE counter 4 | FEBE counter 3 | FEBE counter 2 | FEBE counter 1 | FEBE counter 0 | $FF | $FF |
| BR5 | NEBE counter 7 | NEBE counter 6 | NEBE counter 5 | NEBE counter 4 | NEBE counter 3 | NEBE counter 2 | NEBE counter 1 | NEBE counter 0 | $CD | $3C |
| BR6 | U-loop B1 | U-loop B2 | U-loop 2B+D | U-loop transparent | IDL/GCI Loop B1 | IDL/GCI Loop B2 | IDL/GCI Loop 2B+D | IDL/GCI loop transp | $00 | $00 |
| BR7 | reserved | **GCI_PS1 pin** | **GCI_PS2 pin** | IDL/GCI U invert | *IDL freerun disable* | reserved | reserved | *IDL 8/10* | $00 | $00 |
| BR8 | frame steering | frame control 2 | frame control 1 | frame control 0 | CRC corrupt | match scrambler | reserved | reserved | $01 | $01 |
| | frame state 3 | frame state 2 | frame state 1 | frame state 0 | reserved | reserved | reserved | reserved | $01 | $01 |
| BR9 | EOC control 1 | EOC control 0 | M4 control 1 | M4 control 0 | M5/M6 control 1 | M5/M6 control 0 | FEBE/NEBE control | reserved | $00 | $00 |
| BR10 | reserved | reserved | reserved | reserved | reserved | select Dump access | select D Channel access | select Overlay registers | | |
| BR11 | activation control 6 | activation control 5 | activation control 4 | activation control 3 | activation control 2 | activation control 1 | activation control 0 | activation timer dis | $0C | $0C |
| | activation state 6 | activation state 5 | activation state 4 | activation state 3 | activation state 2 | activation state 1 | activation state 0 | activation timer exp | $0C | $0C |
| BR12 | activation control steer | reserved | load activation state | step activation state | hold activation state | jump select | reserved | force linkup | $00 | $00 |
| | EPI 18 | EPI 17 | EPI 16 | EPI 15 | EPI 14 | EPI 13 | EPI 12 | EPI 11 | $00 | $00 |
| BR13 | enable MEC updates | accum EC output | enable EC updates | fast EC beta | accum DFE output | enable DFE output | fast DFE/ ARC beta | clear all coefficients | $00 | $00 |
| | EPI10 | EPI 9 | EPI 8 | EPI 7 | EPI 6 | EPI 5 | EPI 4 | EPI 3 | $00 | $00 |
| jBR14 | reserved | ro/wo to r/w | reserved | Framer to Deframer loop | ± 1 tone | reserved | reserved | reserved | $00 | $00 |
| BR15 | Mask 7 | Mask 6 | Mask 5 | Mask 4 | Mask 3 | Mask 2 | Mask 1 | Mask 0 | | |

**Figure 5-11.** U-Interface Byte Register Map

### 5.3.3.1 U-Interface BR0

BR0 contains the M4 bits that are framed and sent by the Superframe Framer. Bits written to this register are sent out on the next transmit Superframe boundary if Superframe Update Disable (NR2(b1)) is cleared (0). This register is double buffered. All bits are set (1) following a hardware reset ($\overline{\text{RESET}}$ pulled low) or software reset (NR0(b3) is set). This register is replaced by OR0 when BR10(b0) = 1.

| *b7* | *b6* | *b5* | *b4* | *b3* | *b2* | *b1* | *b0* |
|---|---|---|---|---|---|---|---|
| M40 rw | M41 rw | M42 rw | M43 rw | M44 rw | M45 rw | M46 rw | M47 rw |

**Figure 5-12.** U-Interface BR0 Bit Definitions

**Figure 5-12** names the bit fields in BR0. **Table 5-2** shows the definitions of the M4 bits as defined by ANSI T1.601-1992 for the Network to NT channel and the NT to Network channel.

**Table 5-2.** M4 Bit Definitions

| M4 Bits | Network to NT | NT to Network |
|---|---|---|
| M40 | ACT | ACT |
| M41 | DEA | PS1 |
| M42 | SCO[1] | PS2 |
| M43 | 1[2] | NTM |
| M44 | 1[2] | CSO |
| M45 | 1[2] | 1[2] |
| M46 | [UOA] | [SAI] |
| M47 | [AIB] | NIB[1] |

**Notes:** **1.** These bits are defined in Bellcore document TR-NWT000397, Issue 3. When set to 0, the LT indicates to the NT that the network deactivates the loop between calls.
**2.** These bits are presently reserved by ANSI T1.601-1988 and should be set to 1s.

**NOTE:** BR0 should not be modified while the device is in GCI mode. See OR6(b4).

### 5.3.3.2 U-Interface BR1

By reading this register, the external microcontroller obtains a buffered copy of the M4 bits being parsed from the received superframe by the Superframe Deframer. The values in the register are valid when Superframe Sync (NR1(b1)) is set (1). See **Section 5.3.3.10** for a description of when the "read" information is updated and when to write to this register. This register is double buffered. The receive M4 channel byte can be read at any time during the superframe prior to the next update. It is recommended that the microcontroller read this register as soon as possible after an interrupt. Setting OR7(b) to 1 selects trinal checking on M4 ACT, DEA, UOA, and SAI bits. If trinal checking of all bits is desired, it must be done via software. This register is replaced by OR1 when BR10(b0) = 1. When OR7(b0) is set to 1, the M4 ACT, DEA, UOA, and SAI bits must be the same for the three superframes before they are updated in this register.

**NOTE:** The value of BR14(b6) has no effect on the operation of this register.

| *b7* | *b6* | *b5* | *b4* | *b3* | *b2* | *b1* | *b0* |
|---|---|---|---|---|---|---|---|
| M40<br>ro/wo | M41<br>ro/wo | M42<br>ro/wo | M43<br>ro/wo | M44<br>ro/wo | M45<br>ro/wo | M46<br>ro/wo | M47<br>ro/wo |

**Figure 5-13.** U-Interface BR1 Bit Definitions

**Figure 5-13** names the bit fields in BR1. **Table 5-2** shows the definitions of the M4 bits as defined by ANSI T1.601-1992 for the Network to NT channel and the NT to Network channel.

### 5.3.3.3 U-Interface BR2

This register contains the reserved M5 and M6 bits that are sent by the Superframe Framer. The bits written to the register are sent out on the next transmit Superframe boundary if Superframer Update Disable (NR2(b1) is cleared (0). All bits are set (1) following a hardware reset ($\overline{\text{RESET}}$ pulled low) or software reset (NR0(b3) is set). See **Section 5.3.3.10** for details concerning the use of the FEBE input (b4). Bits b7, b6, and b5 are double buffered. When BR10(b0) = 1, this register is replaced by OR2.

| *b7* | *b6* | *b5* | *b4* | *b3* | *b2* | *b1* | *b0* |
|---|---|---|---|---|---|---|---|
| M50<br>rw | M60<br>rw | M51<br>rw | FEBE Input<br>rw | Reserved | Reserved | Reserved | Reserved |

**Figure 5-14.** U-Interface BR2 Bit Definitions

**Figure 5-14** names the bit fields in BR2.

- **FEBE Input (b4)**—The bit value is enabled and transmitted as FEBE if BR9(b1) = 1.

**NOTE:** ANSI T1.601-1992 presently reserves bits **M50 (b7)**, **M60 (b6)**, and **M51 (b5)**. Therefore, these bits should be set to 1s for ISDN applications.

**NOTE:** Reserved bits b0, b1, b2, and b3 should be set to 0 at all times to maintain future compatibility.

### 5.3.3.4 U-Interface BR3

BR3 contains the ANSI T1.601-1992 reserved M5 and M6 bits occurring in basic frames 1 and 2 of the superframe that are received by the Superframe Deframer and four other Superframe Deframer status bits. The M5 and M6 values in the register are valid when the Superframe Sync bit (NR1(b1)) = 1. M50, M51, and M60 are updated based on the mode defined by BR9(b3) and BR9(b2).

Bits b7, b, and b5 are double buffered. They can be read at any time during the superframe prior to the next update. It is recommended that this register be read as soon as possible after an M5/M6 channel interrupt. Refer to **Section 5.3.3.10** for details concerning the operation of these three bits. When BR10(b0) = 1, this register is replaced by OR3.

| *b7* | *b6* | *b5* | *b4* | *b3* | *b2* | *b1* | *b0* |
|---|---|---|---|---|---|---|---|
| M50<br>ro/wo | M60<br>ro/wo | M51<br>ro/wo | Received FEBE<br>ro | Computed FEBE<br>ro | Verified ACT<br>ro | Verified DEA<br>ro | Superframe Detect<br>ro |

**Figure 5-15.** U-Interface BR3 Bit Definitions

**Figure 5-15** names the bit fields in BR3.

**NOTE:** ANSI T1.601-1992 presently reserves bits **M50 (b7)**, **M60 (b6)**, and **M51 (b5)**. Therefore, these bits should be set to 1s for ISDN applications.

The remaining bits are:

- **Received FEBE (b4)**—This is the state of the received FEBE bit in the last complete received superframe. It is updated at the end of each received superframe when Superframe Sync (NR1(b1)) and Linkup (NR1(b3)) are both 1s.
- **Computed NEBE (b3)**—This is the state of the Cyclic Redundancy Check（CRC）from the last complete received superframe. It is updated at the end of each received superframe. This bit is 0 when a CRC error is detected. Also, when either Superframe Sync (NR1(b1)) or Linkup (NR1(b3)) is 0, this computed near-end block error（NEBE）bit is forced to 0.
- **Verified ACT (b2)**—This is the dual-consecutively checked setting of the ACT bit in the received superframe. Dual-consecutive checking requires that the received bit be in the same state for two consecutive superframes. Whenever the U-Interface transceiver detects a transition from 0 to 1 on Superframe Sync, NR1(b1), Verified ACT = 0. It remains in its current state until both Superframe Sync (NR1(b1)) and Linkup (NR1(b3)) are 1s. Then, if the received ACT bit is 1 for two consecutive superframes, Verified ACT becomes a 1. After Verified ACT becomes a 1, it changes to 0 if the received ACT bit is received as a 0 for two consecutive superframes. This bit is updated at the end of the first frame of each superframe and is provided in this register for status only. See BR9(b5–b4) for more information regarding this bit. When OR7(b0) is set, the M4 ACT and DEA bits must be valid for three superframes before Verified ACT or Verified DEA are updated.

- **Verified DEA (b1)**—This is the dual-consecutively checked, inverted setting of the DEA bit, in the received superframe. Dual-consecutive checking requires that the received bit is in the same state for two consecutive superframes. Whenever the U-Interface transceiver detects a transition from 0 to 1 on Superframe Sync in NR1(b1), Verified DEA = 0. It remains in its current state until both Superframe Sync (NR1(b1)) and Linkup (NR1(b3)) are 1s. Then, if the received DEA bit is 0 for two consecutive superframes, Verified DEA = 1. After Verified DEA = 1, if the received DEA bit = 1 for two consecutive superframes, then Verified DEA = 0. This bit is updated at the end of the second basic frame of each superframe and is provided in this register for status only. See BR9(b5–b4) for more information regarding this bit. When OR7(b0) is set, the M4 DEA bit must be valid for three superframes before Verified DEA is updated.
- **Superframe Detect (b0)**—This is the unmodified output of the Superframe Deframer's detection circuit. It is primarily intended for diagnostic purposes.

### 5.3.3.5 U-Interface BR4

This register contains the current FEBE count. The counter is not cleared by a software or hardware reset. The register can be preset to any value by writing to it. If the FEBE bit is active in a superframe, the counter increments at the end of the received superframe. The counter does not increment unless Superframe Sync (NR1(b1)) and Linkup (NR1(b3)) are both 1s. If OR7(b1) is set, then the FEBE counter rolls over from $FF to $00. User software must account for the possibility that, if OR7(b1) is set, the counter value read from BR4 might be less than the previous value, indicating that the counter has rolled over. This register is replaced by Register OR4 when BR10(b0) = 1. When OR7(b1) is cleared (default after reset), BR4 counts to $FF and does not roll over.

| *b7* | *b6* | *b5* | *b4* | *b3* | *b2* | *b1* | *b0* |
|---|---|---|---|---|---|---|---|
| FEBE Counter 7 rw | FEBE Counter 6 rw | FEBE Counter 5 rw | FEBE Counter 4 rw | FEBE Counter 3 rw | FEBE Counter 2 rw | FEBE Counter 1 rw | FEBE Counter 0 rw |

**Figure 5-16.** U-Interface BR4 Bit Definitions

**Figure 5-16** names the bit fields in BR4. These bits are:

- **FEBE Counter 7–FEBE Counter 0 (b7–b0)**—These bits constitute the FEBE Counter.

### 5.3.3.6 U-Interface BR5

This register contains the current NEBE count. A NEBE occurs whenever the received CRC message does not match the computed CRC or when Linkup (NR1(b3)) is 1 and Superframe Sync (NR1(b1)) is 0. The Superframe Framer maintains the superframe timing to increment the NEBE counter when Superframe Sync is 0. The counter is not cleared by a software or hardware reset. The register can be preset to any value by writing to it.

When the Superframe Deframer detects a CRC error in the received superframe, the counter is incremented at the end of that superframe. When OR7(b1) is set, then the NEBE counter rolls over from $FF to $00. User software must account for the possibility that, if OR7(b1) is set, the counter value read from BR5 might be less than the previous value, indicating that the counter has rolled over. When BR10(b0) = 1, this register is replaced by Register OR5. When OR7(b1) is cleared (default after reset), BR5 counts to $FF and does not roll over.

| *b7* | *b6* | *b5* | *b4* | *b3* | *b2* | *b1* | *b0* |
|---|---|---|---|---|---|---|---|
| NEBE Counter 7<br>rw | NEBE Counter 6<br>rw | NEBE Counter 5<br>rw | NEBE Counter 4<br>rw | NEBE Counter 3<br>rw | NEBE Counter 2<br>rw | NEBE Counter 1<br>rw | NEBE Counter 0<br>rw |

**Figure 5-17.** U-Interface BR5 Bit Definitions

**Figure 5-17** names the bit fields in BR5. These bits are:

- **NEBE Counter 7–NEBE Counter 0 (b7–b0)** — These bits constitute the NEBE Counter.

### 5.3.3.7 U-Interface BR6

This register contains the loopback controls. For normal (no loopback) operation, bits b7–b5 and b3–b1 of BR6 should be 0. BR6 is cleared by a software reset (NR0(b3) = 1), hardware reset ($\overline{\text{RESET}}$ is driven low), or when the Return to Normal bit (NR0(b0)) is set. When a bit is set to 1, the appropriate loopback is enabled. This register is replaced by Register OR6 when BR10(b0) = 1. Bits b7–b4 are not set when the MC145576 is operating in the automatic EOC mode.

| *b7* | *b6* | *b5* | *b4* | *b3* | *b2* | *b1* | *b0* |
|---|---|---|---|---|---|---|---|
| U-Loop B1 rw | U-Loop B2 rw | U-Loop 2B+D rw | U-Loop Transparent rw | IDL/GCI-Loop B1 rw | IDL/GCI-Loop B2 rw | IDL/GCI-Loop 2B+D rw | IDL/GCI-Loop Transparent rw |

**Figure 5-18.** U-Interface BR6 Bit Definitions

**Figure 5-18** names the bit fields in BR6. These bits are:

- **U-Loop B1 (b7)**—This bit selects a loopback on the B1 channel toward the U-Interface.
- **U-Loop B2 (b6)**—This bit selects a loopback on the B2 channel toward the U-Interface.
- **U-Loop 2B+D (b5)**—This bit selects a loopback on the B1, B2, and D channels toward the U-Interface.
- **U-Loop Transparent (b4)**—This bit selects whether the loopback toward the U-Interface should be handled transparently or not. This transparency selection applies to all channels that are selected for loopback to the U-Interface.
- **IDL/GCI-Loop B1 (b3)**—This bit selects a loopback on the B1 channel toward the IDL/GCI interface. This bit operates in all IDL and GCI modes.
- **IDL/GCI-Loop B2 (b2)**—This bit selects a loopback on the B2 channel toward the IDL/GCI interface. This bit operates in all IDL and GCI modes.
- **IDL/GCI-Loop 2B+D (b1)**—This bit selects a loopback on the B1, B2, and D channels toward the IDL/GCI interface. When this bit = 1, the IDL/GCI-loop B1 and IDL/GCI-loop B2 bits are ignored. This bit operates in all IDL and GCI modes.
- **IDL/GCI-Loop Transparent (b0)**—This bit selects whether the loopback toward the IDL/GCI interface is handled transparently or not. This transparency selection applies to all channels that are selected for loopback to the IDL/GCI interface.

**Figure 5-19** and **Figure 5-20** may be used to determine the combined effect of setting more than one loopback control in BR6, as well as the bits in NR5 and BR7. Only details for the B1 channel are shown, but a similar set of logic applies to both the B2 and D channels. DOUT and DIN refer to the two external pins on the device. There are two control signals shown in **Figure 5-20** that do not come from MC145576 registers. Link Active is an internal signal that is asserted when the ANSI T1.601-1992 defined activation sequence reaches SN3/SL3 and Customer Enable (NR2(b0)) is set, or Verified ACT (BR3(b2)) is set. Link Good is asserted whenever the ANSI T1.601-1992 defined activation sequence is completed successfully and the internally monitored receive error rate is adequate for passing data.

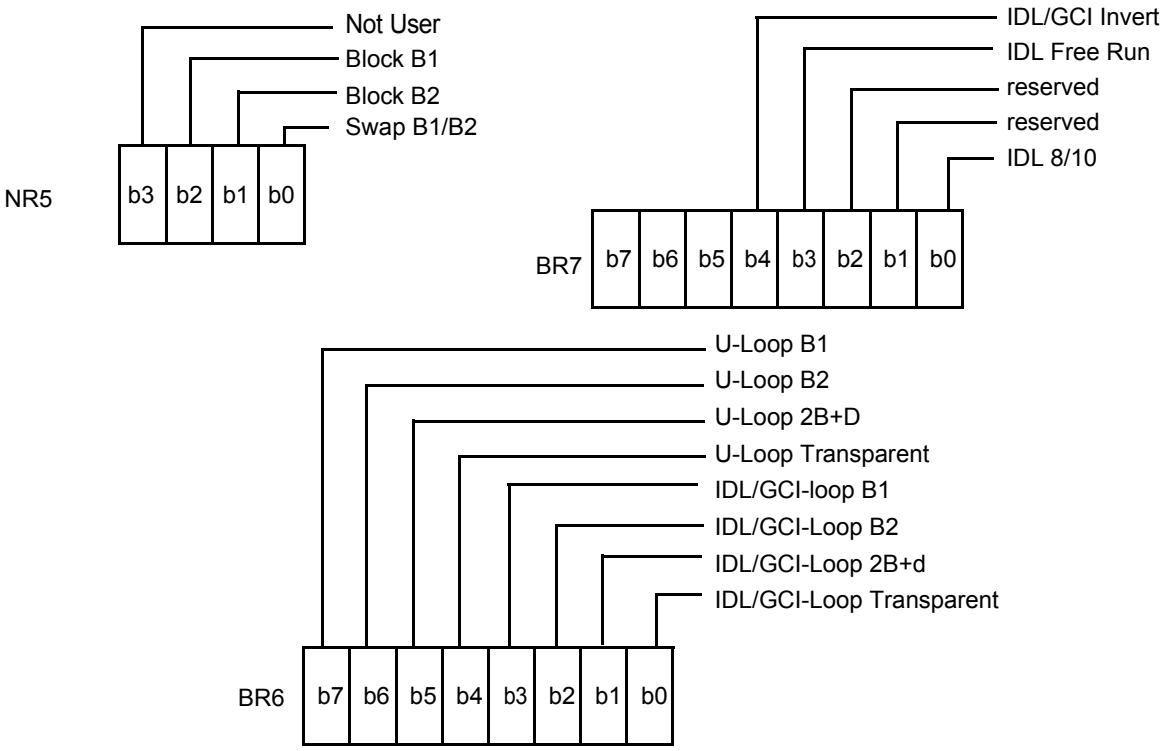



**Figure 5-19.** IDL/GCI Interface Loopback Control Bits (U-Interface)

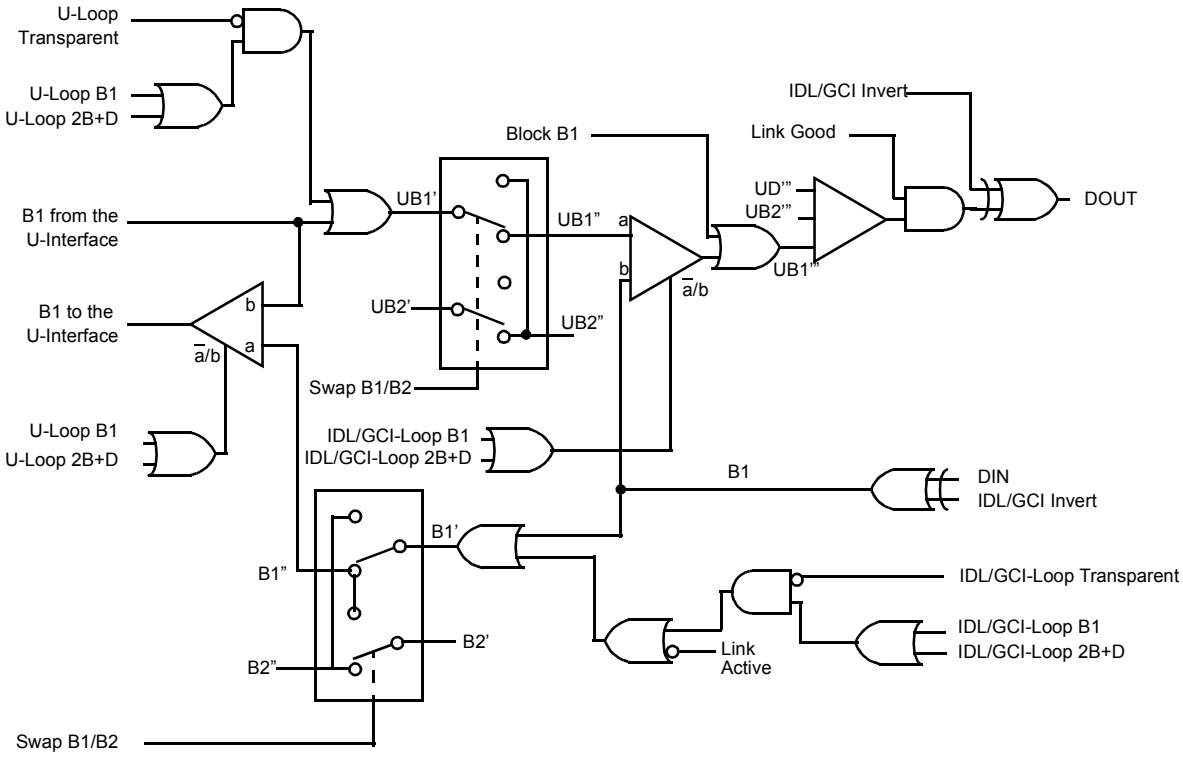



**Figure 5-20.** IDL/GCI Interface Loopback Logic Diagram (U-Interface)

### 5.3.3.8 U-Interface BR7

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| reserved | **GCI IN2** ro | **GCI IN1** ro | IDL/GCI Invert rw | *IDL Free Run* rw | reserved | reserved | *IDL 8/10* rw |

**Figure 5-21.** U-Interface BR7 Bit Definitions

**Figure 5-18** names the bit fields in BR6. The function of the bits depends on the selected IDL or GCI control mode. These bits are:

- **GCI IN2 (b6)**—This is a read-only bit. When read (provided the MC145576 is in full GCI mode), bit IN2 reflects the state of a GCI mode dedicated input pin. These pins may be used for any purpose in a GCI application.
- **GCI IN1 (b5)**—This is a read-only bit. When read (provided the MC145576 is in full GCI mode), bit IN1 reflects the state of a GCI mode dedicated input pin. These pins may be used for any purpose in a GCI application.
- **IDL/GCI Invert (b4)**—When set to 1, this bit forces the IDL/GCI interface to invert every bit just before it is transmitted on the DOUT pin and invert every bit received on DIN.
- **IDL Free Run (b3)**—When set to 0, this bit forces the DCL and FSC output to run continuously when in the IDL/GCI Master mode. When this bit is 1, the DCL and FSC stop when the U-Interface transceiver is deactivated. DCL and FSC start operating when Superframe Sync in NR1(b1) becomes 1 and halt when the U-Interface transceiver enters the ANSI T1.601 defined *Tear Down* state.
- **IDL 8/10 (b0)**—This bit reorders the sequence of 2B+D data presented in the IDL data transfer. The two possible transfer sequences are shown in **Figure 5-22** and **Figure 5-23**. A 1 selects the 8-bit mode and a 0 selects the 10-bit mode. In the 8-bit mode, the two B channels are provided sequentially, followed by the two D channel bits. In the 10-bit mode, one D channel bit follows each B channel byte. The ability to swap the B channels, (NR5(b0)), applies to both of these modes. For further information about the IDL interface, see **Section 5.4.**

**NOTE:** If timeslot assignment mode is enabled via OR6(b7), OR6(b6), or OR6(b5), then the IDL 8/10 control bit is ignored and B channel and D channel data is placed according to OR0–OR5. If GCI electrical mode is selected by setting OR6(b3) to a 1, the IDL interface transfers only 2B+D data in the GCI timeslot locations as programmed in OR5(b2–b0).

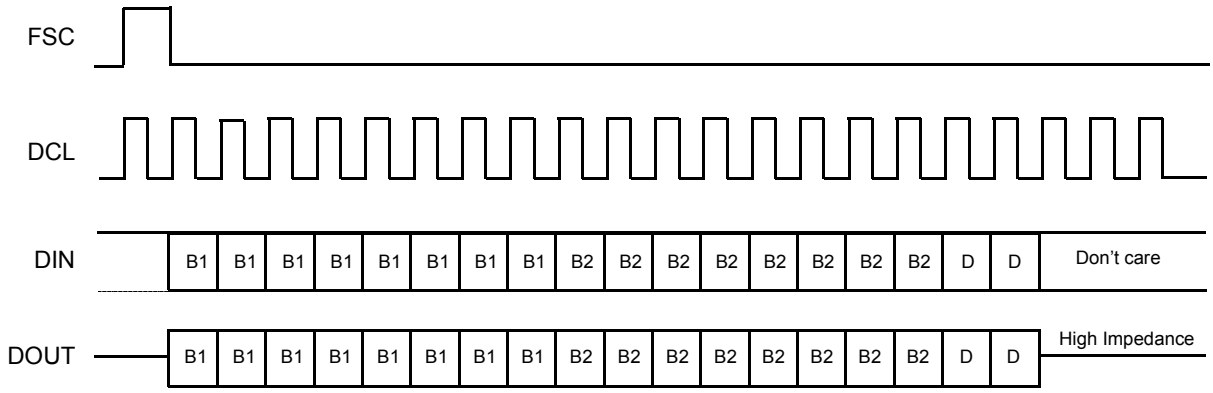



**Figure 5-22.** IDL Interface Timing in 8-Bit Master Mode

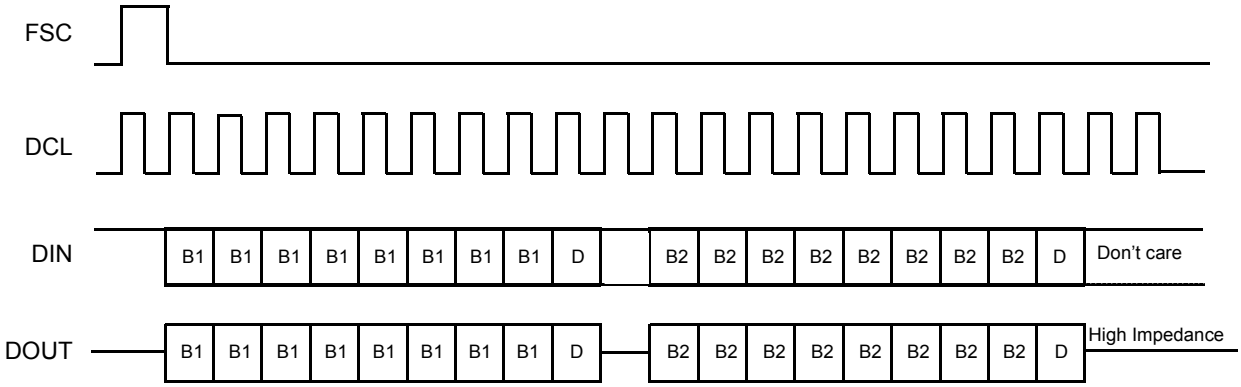



**Figure 5-23.** IDL Interface Timing in 10-Bit Master Mode

### 5.3.3.9 U-Interface BR8

| | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|
| Frame Steering mode (b7=1) | Frame Steering wo | Frame Control 2 wo | Frame Control 1 wo | Frame Control 0 wo | CRC Corrupt rw | Match Scrambler rw | reserved | reserved |
| Frame State mode (b7=0) | Frame State 3 ro | Frame State 2 ro | Frame State 1 ro | Frame State 0 ro | reserved | reserved | reserved | reserved |

**Figure 5-24.** U-Interface BR8 Bit Definitions

**Figure 5-24** names the bit fields in BR8. The configuration of this register depends on the value of b7. If b7 = 1, the Frame Steering mode is selected and the bits are defined as follows:

- **Frame Steering (b7)**—When this bit is a 1, the Frame Control 2–0 bits take over control of the Superframe Framer's mode of operation.
- **Frame Control 2–Frame Control 0 (b6–b4)**—These bits set the mode of operation for the Superframe Framer when the Frame Steering bit is 1. **Table 5-3** shows the mode the Superframe Framer enters, based on the three Frame Control bits and the Frame Steering bit.

**Table 5-3.** Superframe Frame Steering Modes of Operation

| Frame Steering | Frame Control 2:0 | | | Superframe Framer Mode of Operation | |
|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | NT | LT |
| 1 | 0 | 0 | 0 | SN0 | SL0 |
| 1 | 0 | 0 | 1 | Six frames of 10 KHz tone followed by SN1 | SL1 |
| 1 | 0 | 1 | 0 | SN2 | SL2 |
| 1 | 0 | 1 | 1 | SN3 | SL3 |
| 1 | 1 | 0 | 0 | 10 KHz tone | |
| 1 | 1 | 0 | 1 | 40 KHz tone | |
| 1 | 1 | 1 | 0 | Generates a single quat every basic frame which alternates over all four of the 2B1Q symbols. | |
| 1 | 1 | 1 | 1 | Superframe Framer free runs the scrambler with no synchronization words. | |

- **CRC Corrupt (b3)**—When set to 1, this bit forces the transmitted CRC to be inverted. It is used for EOC maintenance procedures and to force an outgoing corrupt CRC in digital loop carrier systems. As the transmit framer transmits the CRC and this bit is set, the transmitted CRC is inverted. This bit can be cleared or setat any time during transmission of a superframe. When OR7(b2) = 1, the operation of this bit is modified so that the outgoing CRC is only corrupted on the current superframe.
- **Match Scrambler (b2)**—When set to 1, this bit forces the descrambler and scrambler polynomials to match. This is used for external analog loopback and framer-to-deframer loopback.

If b7=0, the Superframe Framer output is determined by the state of the Automatic Activation Controller, the .Frame State mode is selected and the bits are defined as follows:

- **Frame State 3–Frame State 0 (b7–b4)**—These bits provide the external microcontroller with the current state of the U-Interface transceiver's Superframe Framer, regardless of whether the Superframe Framer is being controlled by the external microcontroller or internally by the Automatic Activation Controller. The meaning of Frame State 2:0 maps directly onto the meaning of Frame Control 2:0. Frame State 3 is 0 at all times, except during TN of an NT activation sequence. State transitions are always made on frame or superframe boundaries.

### 5.3.3.10 U-Interface BR9

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| EOC Control 1 rw | EOC Control 0 rw | M4 Control 1 rw | M4 Control 0 rw | M5/M6 Control 1 rw | M5/M6 Control 0 rw | FEBE/NEBE Control rw | Reserved |

**Figure 5-25.** U-Interface BR9 Bit Definitions

**Figure 5-25** names the bit fields in BR9. The bits are defined as follows:

- **EOC Control 1–0 (b7–b6)**—These bits control the EOC handling capability of the U-Interface transceiver. Table 4-9 gives a brief description of each mode selected by the EOC Control bits. The EOC Trinal-Check mode (b7,b6 = 1,0) and the Automatic EOC Processor mode (b7,b6 = 0, 0/1) are described in **Table 5-4**. The default mode setting is 0,0; thereby selecting the Automatic EOC Processor. Regardless of the operating mode, every time R6 is loaded by the deframer, IRQ2 (NR3(b2)) = 1. Use the update on every frame mode (b7,b6 = 1,1) for digital loop carrier or proprietary applications.

**Table 5-4.** EOC Control Modes

| EOC Control 1–0 | | Function |
|---|---|---|
| b7 | b6 | |
| 1 | 1 | Update EOC register (R6) on every EOC frame (twice during each superframe). Recommended for Digital Loop Carrier applications. |
| 1 | 0 | **Update EOC register (R6) after passing a trinal- check.** The EOC Trinal-Check operation checks for three identical consecutive EOC messages being received before loading the EOC message into R6. R6 is always updated with the received message when the third identical consecutive message is received.<br><br>When operating as an NT in Trinal-Check mode, received EOC messages are automatically transmitted back by the Superframe Framer if the address is either the NT1 or broadcast address. This continues until three valid consecutive identical messages have been received. If the EOC address in the received EOC message is not 0 or 7, the Hold message is substituted and automatically transmitted back to the LT. Once three valid consecutive identical messages have been received, the deframer updates R6. Once R6 has been updated with the received message, the Superframe Framer's R6 (written to by a SCP interface operation) is transmitted. It is up to the microcontroller firmware to handle the EOC message and place a response into R6 before the U-chip sends the next EOC frame out to the LT (see **Figure 5-20**). R6 is repeated throughout all subsequent EOC frames until it is altered by another CPI interface write to it, or the received EOC message changes. |

**Table 5-4.** EOC Control Modes (Continued)

| EOC Control 1–0 | | Function |
|---|---|---|
| b7 | b6 | |
| 0 | 0 or 1 | **Update EOC register (R6) after passing a trinal-check and also invoke Automatic EOC Processor to operate.** An Automatic EOC Processor is provided. This processor operates the EOC in accordance with ANSI T1.601-1992. The processor recognizes EOC messages addressed to either the NT1 or the broadcast address. The processor decodes the messages in Table 4-10 and then takes the action indicated. If a properly addressed message is received that is not listed in the table, the "Unable to Comply" message is transmitted in response. If an improperly addressed message is received, the "Hold State" message is transmitted with the NT1 address. Whenever operating in this mode, the EOC Trinal-Check operation continues to function and R6 is loaded with the EOC message that the Automatic EOC Processor decodes. Note that because the Automatic EOC Processor is an NT mode only function, selecting mode 0,0 in the LT mode is equivalent to mode 1,0. Regardless of EOC mode, R6 is not altered while Superframe Detect (BR3(b0)) is a 0. When the automatic EOC mode is enabled, bits in BR6 are not set when loopback messages are received. |

**Table 5-5.** Automatic EOC Processor Functions

| EOC Message | Automatic EOC Processor Response |
|---|---|
| Operate 2B+D Loopback | Invokes a loopback to the U-Interface at the IDL interface of the B1, B2, and D channels. Transparency is determined by setting BR6(b4), U-loop transparent |
| Operate B1 Channel Loopback | Invokes a loopback to the U-Interface at the IDL interface of the B1 channel. The loopback is transparent |
| Operate B2 Channel Loopback | Invokes a loopback to the U-Interface at the IDL interface of the B2 channel. The loopback is transparent |
| Request Corrupted CRC | Equivalent to setting BR8(b3) to a 1 |
| Notify of Corrupted CRC | None |
| Return to Normal | Resets all of the previously invoked EOC functions |
| Hold State | Maintains previously invoked EOC functions |

- **M4 Control 1–0 (b5, b4)**—These bits control the M4 handling capability of the U-Interface transceiver. The default mode setting is b5, b4 = 0,0. In all of the modes, BR1 is not loaded and an IRQ1 (NR3(b1)) is not be issued unless both Linkup (NR1(b3)) and Superframe Sync (NR1(b1)) are 1s. When OR7(b0) = 1; UOA, ACT, SAI, and DEA bits in the M4 channel are trinal-checked. See **Table 5-6**.

**Table 5-6.** M4 Control Modes

| OR7 | BR9 M4 Control 1:0 | | Description |
|---|---|---|---|
| | b5 | b4 | |
| 0 | 0 | 0 | M4 Dual Consecutive mode. In addition, the Verified ACT (BR3(b2)) and Verified DEA (BR3(b1)) operations are enabled in this mode only. |
| | 0 | 1 | M4 Dual Consecutive mode. |
| | 1 | 0 | Delta mode. |
| | 1 | 1 | Every mode. |
| 1 | 0/1 | 0/1 | M4 channel bits M40 (ACT), M41 (DEA), and M46 (UOA, SAI) are trinal-checked. Remaining bits operate per BR9(b5,b4) settings. Verified ACT and Verified DEA available on trinal-checked ACT, DEA bits when b5–b4 = 0,0. |

— *M4 Dual Consecutive Modes (b5, b4 = 0,0 or 0,1)*—The M4 Dual Consecutive modes perform a simple algorithm on the received M4 bits, and only interrupt the external microcontroller when an M4 bit has changed state and has remained in the new state for two consecutive superframes. The M4 bit values read from BR1 in this mode are only the most recent values that have been the same for two consecutive superframes. Referring to **Table 5-7**, suppose, for example, that for several superframes the M4 bits have been all 0s, as shown in the column labeled *Received M4 Byte*. If the external microcontroller read BR1, it would read all 0s as shown in the column labeled *BR1 Contents*. Now, notice in the subsequent superframes 2 and 3 that the received M4 bits that do not hold their state for at least two consecutive superframes, do not cause an interrupt, and do not show up in BR1.

At start-up, there is no history of what has been received in the M4 bits. Therefore, the technique for the initial setting for BR1 is as follows: a hardware or software reset sets BR1 to all 0s. However, at the user's discretion, while either Linkup (NR1(b3)) or Superframe Sync (NR1(b1)) is 0, the user may write to BR1 and set the initial value. In this way, the external microcontroller may assume a current state for the M4 bits, and then wait for an IRQ1 to inform it of a change in state. Also, any time that Superframe Sync is lost and then regained, the initial programmed value is reloaded into BR1.

The default M4 Dual Consecutive mode (b5, b4 = 0,0) has the additional feature of performing automatic detection of the ACT and DEA bits. Verified ACT (BR3(b2)) and Verified DEA ((BR3(b1)) are dual consecutive checked values of M40 and M41. Verified ACT is valid for both NT and LT modes. Verified DEA operates in the NT mode only. Whenever there is a 0 to 1 transition on Superframe Sync (NR1(b1)), Verified ACT and Verified DEA are reset. If M40 is received as 1 for two consecutive superframes, Verified ACT = 1. Similarly, if M40 is received as 0 for two consecutive superframes, Verified ACT = 0. When this mode is selected, the logical OR of Verified ACT and the Customer Enable bit in NR2(b0) permits customer data transparency without any action taken by the external microcontroller. In NT mode, if M41 is received for two consecutive superframes as 0, Verified DEA = 1. Similarly, if M41 is received as 1 for two consecutive superframes, Verified DEA returns to 0. When this mode is selected, the logical OR of Verified DEA and the Deactivate Request bit in NR2(b2) allows the U-Interface transceiver to respond to the far-end transceiver's intention to deactivate without requiring any interaction by the external microcontroller. Note that the state of Verified ACT and Verified DEA may be monitored by the external microcontroller through BR3(b2–b1).

**Table 5-7.** M4 Dual Consecutive Modes Example

| Superframe | Received M4 Byte | BR1 Contents | Action |
|---|---|---|---|
| 1 | 0000 0000 | 0000 0000 | – |
| 2 | 1000 0001 | 0000 0000 | – |
| 3 | 0001 0001 | 0000 0001 | IRQ1 is set |

- *M4 Delta Mode (b5, b4 = 1,0)*—The Delta mode compares the M4 data from the previous superframe against the current received superframe M4 data. If there is a difference in at least one bit, BR1 is updated and an IRQ1 interrupt is issued. Note that in this mode, BR1 always contains a copy of the latest received M4 byte from the previous superframe.
- *M4 Every Mode (b5, b4 = 1,1)*—The Every mode stores each received superframe of M4 data in BR1 and issues an interrupt at the end of every received superframe.

**NOTE:** Regardless of the mode of operation, BR1 is not altered while Superframe Sync (NR1(b1)) is 0.

- *M4 Trinal-Check Mode*—The M4 ACT, DEA, SAI, and UOA bits can be configured for trinal-check operation by setting OR7(b0) to a 1. See **Section 4.5.8** for more detail.

- **M5/M6 Control 1–0 (b3, b2)**—These bits control the M5/M6 handling capability of the U-Interface transceiver. The default mode setting is b3, b2 = 0,0, which selects the Dual Consecutive mode. These controls are identical in operation to the M4 mode control functions, except that they apply to M50, M51, and M60. Refer to the M4 Control mode paragraphs above for a description of the M5/M6 Control modes. The M5/M6 interrupt, IRQ0 (NR3(b0)), occurs in the middle of the superframe when basic frame 4 has been completely received.

**Table 5-8.** M5/M6 Control Modes

| M5/M6 Control 1:0 | | Description |
|---|---|---|
| b3 | b2 | |
| 0 | 0/1 | M5/M6 Dual Consecutive mode. |
| 1 | 0 | Delta mode. |
| 1 | 1 | Every mode. |

- **FEBE/NEBE Control**—This bit controls how the transmitted FEBE is computed. If this bit is 0, the transmitted FEBE is set active if either the Computed NEBE (BR3(b3)) is active or the FEBE input (BR2(b4)) is set active. If this control bit = 1, the transmitted FEBE = whatever is set in the FEBE input (BR2(b4)).

**NOTE:** For FEBE and NEBE, *active* means set to 0.

### 5.3.3.11 U-Interface BR10

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | Reserved | Reserved | Select Dump Access rw | Select DCH Access rw | Select Overlay rw |

**Figure 5-26.** U-Interface BR10 Bit Definitions

**Figure 5-26** names the bit fields in BR10. The bits are defined as follows:

- **Select Dump Access (b2)**—This bit hides the normal byte register BR13, and the register becomes a byte-wide access port, OR13, to the dump/restore mechanism of the U-Interface. Two more bits in the overlay registers control the operating mode of the dump/restore mechanism. See **Section 5.3.4.9**. This bit is reset by both hardware and software resets.
- **Select DCH Access (b1)**—This bit hides the normal byte register, BR12, and the register becomes an 8-bit read-only/write-only register, OR12, and provides access to the D channel. When this bit is asserted, D channel input data present on the pin interfaces is ignored and DOUT is high impedance. Instead, the D channel is sourced strictly from this register. D channel data received from the U-Interface maintains correct byte alignment relative to the U-Interface basic frame boundary on the pin interfaces, and is readable through OR12, eight bits at a time. IRQ3 is used to indicate when every new eight bits of data are received, in addition to indicating a change in receive status.
  A special code (1111) is loaded in Nibble register NR1, to indicate that the source of the interrupt is the D channel access register. Both transmit and receive of the D channel data is aligned respective to the transmit and receive superframes. When selected, the D channel access register has the highest priority over other possible routes (e.g., the IDL/GCI interface and the D channel port), for the D channel data. This bit is reset by both hardware and software resets. Software should read and write this register at the time the D channel interrupt occurs.

  Enabling OR12 access, enables the D channel interrupt onto IRQ3. The interrupt must still be enabled via IRQ3 Enable in NR4 for the IRQ pin to become active. Upon receipt of the interrupt, the external controller must read the interrupt status in NR3 to determine that it is an IRQ3. The controller must then read NR1, where it would find the code 1111, indicating the actual source is a D channel interrupt.

  **NOTE:** If DCH Access mode is used in conjunction with timeslot assignment, the D channel timeslot must not be timeslot 0 in order to maintain synchronization with the transmit superframe.
- **Select Overlay (b0)**—This bit hides the normal byte registers BR0–BR9, and the registers become the overlay registers OR0–OR9. In general, the overlay registers contain device information that needs to be set only once following reset, such as the timeslot information or during some test mode. This bit is reset by both hardware and software resets.

### 5.3.3.12 U-Interface BR11

| | *b7* | *b6* | *b5* | *b4* | *b3* | *b2* | *b1* | *b0* |
|---|---|---|---|---|---|---|---|---|
| Control mode (BR12(b7)= 0) | Activation Control 6 wo | Activation Control 5 wo | Activation Control 4 wo | Activation Control 3 wo | Activation Control 2 wo | Activation Control 1 wo | Activation Control 0 wo | Activation Timer Disable wo |
| Interpolate mode (BR12(b7)=1) | Activation State 6 ro | Activation State 5 ro | Activation State 4 ro | Activation State 3 ro | Activation State 2 ro | Activation State 1 ro | Activation State 0 ro | Activation Timer Expire ro |

**Figure 5-27.** U-Interface BR11 Bit Definitions

**Figure 5-27** names the bit fields in BR11. The function of this register depends on the values set in BR12. When the Activation Control Steer bit (BR12(b7)) = 0, the BR11 bits are defined as follows:

- **Activation Control 6–0 (b7–b1)**—These write-only bits allow the external microcontroller to set a new activation state for the U-Interface transceiver to execute. The transition to this state is controlled by BR12. Use of this register is not required for normal operation.
- **Activation Timer Disable (b0)**—When this write-only bit is 0, the activation timer operates normally. During activation, the timer runs for approximately 15 seconds, and then the Activation Timer Expire bit becomes 1, and the activation state machine reacts to the time-out. When this bit = 1, the activation timer is disabled and the Activation Timer Expire always reads back as 0.

When the Activation Control Steer bit (BR12(b7)) = 1, the BR11 bits are defined as follows:

- **Activation State 6–0 (b7–b1)**—These read-only bits contain the current state of the internal activation controller. Activation State 6, BR11(b7) indicates cold start mode when it is 0 and indicates warm start mode when it is 1.
- **Activation Timer Expire (b0)**—This bit shows the status of the activation timer. A 1 indicates that the activation timer has expired.

### 5.3.3.13 U-Interface BR12

| | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|
| Write-only | Activation Control Steer<br>wo | reserved | Load Activation State<br>wo | Step Activation State<br>wo | Hold Activation State<br>wo | Big Jump Select<br>wo | reserved | Force Linkup<br>wo |
| Read-only | EPI 18<br>ro | EPI 17<br>ro | EPI 16<br>ro | EPI 15<br>ro | EPI 14<br>ro | EPI 13<br>ro | EPI 12<br>ro | EPI 11<br>ro |

**Figure 5-28.** U-Interface BR12 Bit Definitions

**Figure 5-28** names the bit fields in BR12. For a write to this register, the bits are defined as follows:

- **Activation Control Steer (b7)**—When this bit is 0, the internal MC145576 CPU has total control of its peripherals, and has them perform a normal activation procedure. However, when this bit = 1, the internal CPU and its peripherals are directed to use the control information provided in BR13, BR15A(b7), and BR15A(b6).
- **Load Activation State (b5)**—When this bit = 1, Activation Control 6–0 is loaded into the activation controller as the new state. The load is performed at a time that does not adversely affect the operation of the CPU, and takes place within 1 baud of setting this bit to 1. To load an activation state, this bit must initially be 0. The desired state is then loaded into BR11 and this bit is set to 1. Loading overrides the setting of the Hold Activation State bit (b3).
- **Step Activation State (b4)**—When this bit = 1, the activation controller advances to its next state based on its current inputs. The step is performed at a time that does not adversely affect the operation of the CPU. This bit must be returned to 0 following the step, to prepare for subsequent steps. Stepping overrides the Hold Activation State bit (b3). The step does not occur unless the CPU has determined that a condition for continuing to the next activation state is satisfied.
- **Hold Activation State (b3)**—When this bit = 1, the activation controller remains in the current state until either a Load Activation State (b5) or a Step Activation State (b4) is performed.
- **Big Jump Select (b2)**—When this bit = 1, timing phase jumps are made in four-unit increments. When this bit = 0, timing phase jumps are in one-unit increments.

**NOTE:** Ensure that reserved bit b1 is always 0 to maintain future compatibility.

- **Force Linkup (b0)**—When this bit = 1, the internal status is forced to be that of full-duplex operation, but the CPU is still operating according to the activation state as read in BR11. However, loopbacks and maintenance operations may be performed at the Superframe Framer/Deframer level with full data transparency.

This register also constitutes part of the read-only EPI register as follows:

- **EPI 18–11 (b7–b0)**—These are the most significant bits of the CPU EPI register. The EPI register in the CPU takes on different meanings, depending on the current activation state. This EPI register is updated once per frame. The EPI bits 10–3 are in BR13. The EPI bits 2–0 are not available to the external microcontroller.

### 5.3.3.14 U-Interface BR13

| | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|
| Write-only | Enable MEC Updates wo | Accumulate EC Output wo | Enable EC Updates wo | Fast EC Beta wo | Accumulate DFE Output wo | Enable DFE Updates wo | Fast DFE/ ARC Beta wo | Clear All Coefficients wo |
| Read-only | EPI 10 ro | EPI 9 ro | EPI 8 ro | EPI 7 ro | EPI 6 ro | EPI 5 ro | EPI 4 ro | EPI 3 ro |

**Figure 5-29.** U-Interface BR13 Bit Definitions

**Figure 5-29** names the bit fields in BR13. For a write to the register, the bits are defined as follows:

- **Enable MEC Updates (b7)**—When set to 0, this bit freezes the current coefficients of the Memory Echo Canceller (MEC).
- **Accumulate EC Output (b6)**—When this bit = 1, the results of all three echo cancellers (MEC, Transversal Echo Canceller (TEC), and Infinite Impulse Response Echo Canceller (IIREC)) are included in the process of recovering the received symbol.
- **Enable EC Updates (b5)**—When set to 0, this bit freezes the current coefficients of the TEC and IIREC echo cancellers.
- **Fast EC Beta (b4)**—This bit controls the echo canceller beta constant. A 1 instructs the echo canceller to adapt at its fastest rate.
- **Accumulate DFE Output (b3)**—When 0, this bit forces the output from the Decision Feedback Equalizer (DFE) convolution to 0 and the symbol storage elements of the DFE alternate ± 1. When this bit is 1, the DFE convolution is included in the process of recovering the received symbol.
- **Enable DFE Updates (b2)**—When set to 0, this bit freezes the DFE coefficients and the Adaptive Reference Control (ARC) tap.
- **Fast DFE/ARC Beta (b1)**—This bit controls the betas for the DFE and ARC. When set to 1, the DFE and ARC adapt at their highest rate.
- **Clear All Coefficients (b0)**—When set to 1, the coefficients in the DFE, ARC, TEC, and MEC are cleared and the elastic buffer is reset. The timing offset between the receive and transmit clocks is not altered by setting this bit.

This register also constitutes part of the read-only EPI register as follows:

- **EPI 10–3 (b7–b0)**—These are the least significant bits of the EPI register within the CPU. The EPI register in the CPU takes on different meanings, depending on the current activation state. This EPI register is updated once per frame. The EPI bits 18–11 are in BR12. EPI bits 2–0 are not available to the external microcontroller.

### 5.3.3.15 U-Interface BR14

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| reserved | RO/WO to R/W<br>rw | reserved | Framer-to-Deframer Loop<br>rw | ± 1 Tones<br>rw | reserved | reserved | reserved |

**Figure 5-30.** U-Interface BR14 Bit Definitions

**Figure 5-30** names the bit fields in BR14. The bits are defined as follows:

- **RO/WO to R/W (b6)**—When this bit = 1, all of the write-only registers, become read/write registers for diagnostic purposes. A normally read-only bit is not available when this b6 = 1.
- **Framer-to-Deframer Loopback (b4)**—This bit enables the Superframe Framer to Superframe Deframer Loopback mode when it is 1. The transmit drivers are off in this mode.
- **±1 Tones (b3)**—When this bit = 1, the Superframe Framer generates its tones (10 KHz and 40 KHz) using ± 1 quats instead of the default of ± 3 quats.

**NOTE:** Ensure that reserved bits b7, b5, b2, b1, and b0 are always 0.

### 5.3.3.16 U-Interface BR15

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| Mask 7<br>ro | Mask 6<br>ro | Mask 5<br>ro | Mask 4<br>ro | Mask 3<br>ro | Mask 2<br>ro | Mask 1<br>ro | Mask 0<br>ro |

**Figure 5-31.** U-Interface BR15 Bit Definitions

**Figure 5-31** names the bit fields in BR15. These bits are:

- **Mask 7–Mask 0 (b7–b0)**—These bits represent the revision number of the MC145576 transceiver manufacturing mask set.

### 5.3.4 U Overlay Registers

The overlap map is enabled by setting any of the bits BR10(b2–b0). Setting the bits replaces BR0-BR9, BR12, and/or BR13 with the the specified overlay registers. Clearing the bits in BR10(b2–b0) restores the Byte Registers.

| Reg. | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|
| OR0 | *DOUT B1 Channel Timeslots Bits (7–0)* | | | | | | | |
| OR1 | *DOUT B2 Channel Timeslots Bits (7–0)* | | | | | | | |
| OR2 | *DOUT D Channel Timeslots Bits (7–0)* | | | | | | | |
| OR3 | *DIN B1 Channel Timeslots Bits (7–0)* | | | | | | | |
| OR4 | *DIN B2 Channel Timeslots Bits (7–0)* | | | | | | | |
| OR5 | *DIN D Channel Timeslots Bits (7–0)* | | | | | | | |
| OR6 | *TSA B1 EN* | *TSA B2 EN* | *TSA D EN* | **GCI Use M4 BR0** | reserved | reserved | reserved | reserved |
| OR7 | reserved | reserved | reserved | reserved | reserved | CRC Mode Corrupt | FEBE/ NEBE Rollover | M4 Trinal Mode |
| OR8 | D/R Mode1 | D/R Mode 0 | reserved | reserved | reserved | reserved | reserved | reserved |
| OR9 | reserved | Open Feedback Switches | Analog Loopback | reserved | reserved | reserved | reserved | reserved |
| D Channel Access Select Overlay | | | | | | | | |
| OR12 | D Channel Transmit Bits (7–0) | | | | | | | |
| | D Channel Receive Bits (7–0) | | | | | | | |
| Dump/Restore Access Select Overlay | | | | | | | | |
| OR13 | Dump Register Write Access (7–0) | | | | | | | |
| | Dump Register Read Access (7–0) | | | | | | | |

**Figure 5-32.** U-Interface Overlay Register Map

**Figure 5-32** shows the U-Interface registers that overlay the standard byte registers. The address for the overlay registers is the same as the address for the standard byte register set. The overlay registers are substituted for the standard registers when at least one of BR10(b2, b1, or b0) = 1.

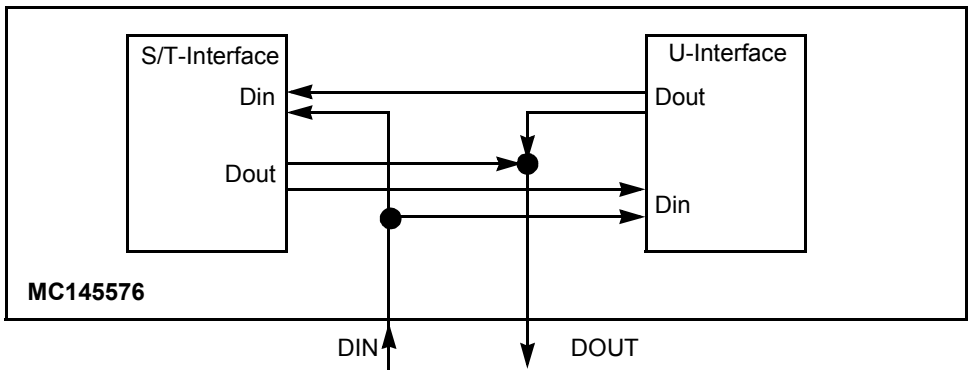



**Figure 5-33.** DIN and DOUT Internal Routing in Timeslot Assigner Mode

### 5.3.4.1 U-Interface OR0

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| DOUT B1 Channel Timeslot Bits (7–0) | | | | | | | |
| rw | | | | | | | |

**Figure 5-34.** U-Interface OR0 Bit Definitions

**Figure 5-34** names the bit fields in OR0. These bits are:

- **DOUT B1 Channel Timeslot Bits (b7–b0)**—This register allows the B1 channel timeslot output from the Dout output of the U-Interface to be allocated one of 256 start points, corresponding to each 2-bit boundary defined by the DCL clock. The default value for OR0 is $00.

### 5.3.4.2 U-Interface OR1

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| DOUT B2 Channel Timeslot Bits (7–0) | | | | | | | |
| rw | | | | | | | |

**Figure 5-35.** U-Interface OR1 Bit Definitions

**Figure 5-35** names the bit fields in OR0. These bits are:

- **DOUT B2 Channel Timeslot Bits (b7–b0)**—This register allows the B2 channel timeslot output from the Dout output of the U-Interface to be allocated one of 256 start points, corresponding to each 2-bit boundary defined by the DCL clock. The default value for OR1 is $00.

### 5.3.4.3 U-Interface OR2

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| DOUT D Channel Timeslot Bits (7–0) | | | | | | | |
| rw | | | | | | | |

**Figure 5-36.** U-Interface OR2 Bit Definitions

**Figure 5-36** names the bit fields in OR2. These bits are:

- **DOUT D Channel Timeslot Bits (b7–b0)**—This register allows the D channel timeslot output from the Dout output of the U-Interface to be allocated one of 256 start points, corresponding to each 2-bit boundary defined by the DCL clock. The default value for OR2 is $00.

**NOTE:** To validate the signal sent by pin UDCLK (pin 9), the D channel timeslot programmed in OR2 should be different from the B1 and B2 channels timeslot programmed in OR0 and OR1 even if B1 or B2 timeslots are not enabled.

### 5.3.4.4 U-Interface OR3

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| DIN B1 Channel Timeslot Bits (7–0) | | | | | | | |
| rw | | | | | | | |

**Figure 5-37.** U-Interface OR3 Bit Definitions

**Figure 5-37** names the bit fields in OR3. These bits are:

- **DIN B1 Channel Timeslot Bits (b7–b0)**—This register allows the B1 channel timeslot input from the Din input of the U-Interface to be allocated one of 256 start points, corresponding to each 2-bit boundary defined by the DCL clock. The default value for OR3 is $00.

### 5.3.4.5 U-Interface OR4

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| DIN B2 Channel Timeslot Bits (7–0) | | | | | | | |
| rw | | | | | | | |

**Figure 5-38.** U-Interface OR4 Bit Definitions

**Figure 5-38** names the bit fields in OR4. These bits are:

- **DIN B2 Channel Timeslot Bits (b7–b0)**—This register allows the B2 channel timeslot input from the Din input of the U-Interface to be allocated one of 256 start points, corresponding to each 2-bit boundary defined by the DCL clock. The default value for OR4 is $00.

### 5.3.4.6 U-Interface OR5

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| DIN B1 Channel Timeslot Bits (7–0) | | | | | | | |
| rw | | | | | | | |

**Figure 5-39.** U-Interface OR5 Bit Definitions

**Figure 5-39** names the bit fields in OR3. These bits are:

- **DIN B1 Channel Timeslot Bits (b7–b0)**—This register allows the D channel timeslot input from the Din input of the U-Interface to be allocated one of 256 start points, corresponding to each 2-bit boundary defined by the DCL clock. The default value for OR5 is $00.

### 5.3.4.7 U-Interface OR6

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| *TSA B1 Enable* rw | *TSA B2 Enable* rw | *TSA D Enable* rw | **GCI Select M4-BR0** rw | reserved | reserved | reserved | reserved |

**Figure 5-40.** U-Interface OR6 Bit Definitions

**Figure 5-40** names the bit fields in OR6. These bits are:

- **TSA B1 Enable (b7)**—This bit is used to enable the B1 channel in IDL Timeslot mode. The B1 timeslot is defined through Overlay registers OR0 and OR3. Whenever any channel (B1, B2, or D) is enabled for Timeslot mode, all channels enter Timeslot mode. If in Timeslot mode and TSA B1 Enable is 0, then the B1 channel is not present on the pin DOUT, and the B1 channel transmit on the U-Interface is actively driven high.
- **TSA B2 Enable (b6)**—This bit is used to enable the B2 channel in IDL Timeslot mode. The B2 timeslot is defined through Overlay registers OR1 and OR4. Whenever any channel (B1, B2, or D) is enabled for Timeslot mode, all channels enter Timeslot mode. If in Timeslot mode and TSA B2 Enable is 0, then the B2 channel is not present on the pin DOUT, and the B1 channel transmit on the U-Interface is actively driven high.
- **TSA D Enable (b5)**—This bit is used to enable the D channel in IDL Timeslot mode. The D timeslot is defined through Overlay registers OR2 and OR5. Whenever any channel (B1, B2, or D) is enabled for Timeslot mode, all channels enter Timeslot mode. If in Timeslot mode and TSA D Enable is a 0, then the D channel is not present on the pin DOUT, and the D channel transmit on the U-Interface is actively driven high.

**NOTE:** Setting b7, b6, or b5 puts the MC145576 in Timeslot Assigner mode. In Timeslot Assigner mode, the IDL 8/10 mode bit in BR7(b0) is ignored and data is placed according to values programmed in OR0–OR5.

- **GCI Select M4-BR0 (b4)**—This bit is useful only in conjunction with full GCI mode. In that mode, when this bit = 0, the GCI C/I channel control automatically sets and resets M4 channel control bits pertaining to the activation state. The bits controlled by the C/I channel are: ACT and SAI. Additionally, the PS1, PS2 bits are transmitted according to the state of PS1 and PS2 pin inputs. When this bit = 1, all M4 bits are transmitted according to the data present in BR0. When operating in full GCI mode, the bit can be set/cleared by using the monitor channel byte register read/write commands. After a hardware or software reset this bit is 0. Normally, GCI operation does not require this bit to be set to a 1.

**NOTE:** After a hardware or software reset, all bits default to 0.

### 5.3.4.8 U-Interface OR7

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| reserved | reserved | reserved | reserved | reserved | CRC Corrupt Mode rw | FEBE/ NEBE Rollover rw | M4 Trinal Mode rw |

**Figure 5-41.** U-Interface OR7 Bit Definitions

**Figure 5-41** names the bit fields in OR7. These bits are:

- **CRC Corrupt Mode (b2)**—This bit changes the operating mode of the input control bit CRC Corrupt (BR8(b3)). When OR7(b2) = 1, the CRC Corrupt input is used to corrupt one, and only one, outgoing superframe CRC. When OR7(b2) = 0, the CRC Corrupt function selected by BR8(b3) operates without restriction. That is, If BR8(b3) is set (1) and OR7(b2) is cleared (0), the CRC of all transmitted superframes is inverted, and this continues until BR8(be) is explicitly reset.
- **FEBE/NEBE Rollover (b1)**—This bit changes the operating mode of the FEBE and NEBE counter registers BR4 and BR5. When FEBE/NEBE rollover = 1, the FEBE and NEBE counter registers do not saturate at all 1s, but instead, rollover from $FF to $00. When FEBE/NEBE rollover = 0, the FEBE and NEBE counter registers saturate at $FF; since neither register is cleared by hardware or software reset, each can only be restarted by writing a new initial value to the register.
- **M4 Trinal Mode (b0)**—This bit changes the operating mode of the persistence checking performed on the ACT, DEA, SAI, and UOA bits in the deframer. When M4 Trinal mode = 1, the checked M4 bits must be valid for three consecutive superframes before asserting Verified ACT, or Verified DEA, etc. When M4 Trinal mode = 0, the M4 bit-checking is controlled by BR9(b5,b4). When operating in full GCI mode, the MC145576 performs trinal checks on the received M4 channel ACT, DEA, SAI, and UOA bits.

**NOTE:** After a hardware or software reset, all bits default to 0.

### 5.3.4.9 U-Interface OR8

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| D/R Mode 1<br>rw | D/R Mode 0<br>rw | reserved | reserved | reserved | reserved | reserved | reserved |

**Figure 5-42.** U-Interface OR8 Bit Definitions

**Figure 5-42** names the bit fields in OR8. These bits are:

- **D/R Mode (1–0) (b7, b6)**—These bits control the operating mode of Dump/Restore Access Overlay register OR12.
  - *00*—Sets the mode for normal dumping and restoring of the internal coefficients via the $EYE_{out}$ interface
  - *01*—Permits write access to the arctap
  - *10*—Permits read access to the arctap
  - *11*—Should be selected to perform dump/restore via the IDL or GCI interface depending on the state of the IDL/GCI pin

**NOTE:** Reserved bits b5–b0 must be set to 0 at all times. After a hardware or software reset, all bits default to 0.

### 5.3.4.10 U-Interface OR9

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| reserved | Open Feedback Switches<br>rw | Analog Loopback<br>rw | reserved | reserved | reserved | reserved | reserved |

**Figure 5-43.** U-Interface OR9 Bit Definitions

**Figure 5-43** names the bit fields in OR9. These bits are:

- **Open Feedback Switches (b6)**—When this bit = 1, it opens the internal feedback path between the transmit (TxP/TxN) and the receive (RxP/RxN) sections. This feature may be used in conjunction with analog loopback.
- **Analog Loopback (b5)**—When this bit = 1, it invokes a receive analog loopback.

**NOTE:** Reserved bits b7 and b4–b0 must be set to 0 at all times. After a hardware or software reset, all bits default to 0.

### 5.3.4.11 U-Interface OR12

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| D Channel Transmit/Receive Bits (7–0) ro/wo | | | | | | | |

**Figure 5-44.** U-Interface OR12 Bit Definitions

**Figure 5-44** names the bit fields in OR2. These bits are:

- **D Channel Transmit/Receive Bits (b7–b0)**—When BR10(b1) = 1, this double buffered register takes the place of Normal Byte register BR12, and the register becomes an 8-bit read-only/write-only register providing access to the D channel. In this mode, D channel input data present on the pin interfaces of MC145576 is ignored. Instead, D channel is sourced strictly from this register. D channel data received from U-Interface is byte aligned to Superframe Sync, and is readable through OR12, eight bits at a time. This register is updated with the received D channel data, when SFS, NR1(b3) is a 1. Data is transferred from OR12 to the U-Interface, when SFS, NR1(b3), is a 1. IRQ3 is used to indicate when each new eight bits of data are received. A special code (1111) is loaded in Nibble register NR1, to indicate that the source of the interrupt is the D channel access register. Reading OR12 clears the special code (1111) from NR1, but does not affect any updates in activation status. So, if there has been a change in activation status, an interrupt is still queued up even though the D channel interrupt has been cleared. Both transmit and receive D channel data are aligned to the transmit and receive superframes. The MC145576 does not perform any HDLC framing/deframing. D channel data is transmitted to and received from the U-Interface most significant bit first.

**NOTE:** If this register is used when the timeslot assignment is enabled, the D channel timeslot must not be 0, in order to maintain synchronization with the transmit superframe.

### 5.3.4.12 U-Interface OR13

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| Dump Register Access Bits (7–0) ro/wo | | | | | | | |

**Figure 5-45.** U-Interface OR13 Bit Definitions

**Figure 5-45** names the bit fields in OR2. These bits are:

- **Dump Register Access Bits (b7–b0)** —This register takes the place of Byte register BR13 when BR10(b2) is set, and then becomes a byte-wide access port to the U-Interface dump/restore mechanism. Two more bits in the overlay registers control the operating mode of the dump/restore mechanism. (See **Section 5.3.4.9**.)

**NOTE:** This bit is reset by both hardware and software resets. After a hardware or software reset, all bits default to 0.

## 5.4 S/T-Interface Registers

These registers are located in the S/T-Interface portion of the MC145576 and are almost exclusively relevant to the operation of the S/T-Interface. Exceptions to this are detailed separately.

### 5.4.1 S/T Nibble Registers

The S/T Nibble Registers are a set of seven control and status registers used with the S/T- Interface. **Figure 5-46** lists the registers along with bit names and default settings after reset.

| Register | b3 | b2 | b1 | b0 | Value after Reset |
|---|---|---|---|---|---|
| NR0 | *Software Reset* | reserved | *Absolute Min Power* | Return to Normal | $0 |
| NR1 | Activation Indication (AI) | Error Indication (EI) | Sleep Indication (SI) | Frame Sync (FS) | $2 |
| NR2 | *Activation Request (AR)* | *Deactivation Request (DR)* | *Activation Timer T1 Expired* | *Terminal Class* | $0 |
| NR3 | IRQ3 | IRQ2 | IRQ6 | IRQ7 | $8 |
| NR4 | IRQ3 Enable | IRQ2 Enable | IRQ6 Enable | IRQ7 Enable | $0 |
| NR5 | Idle B1 Channel TX on S/T-Interface | Idle B2 Channel TX on S/T-Interface | Invert B1 Channel to/from S/T-Interface | Invert B2 Channel to/from S/T-Interface | $0 |
| NR6 | IDL/GCI 2B+D Transparent Loopback at S/T-Interface | Fixed Timing Enable | Sleep Power Down Mode Disable | Exchange B1 and B2 at S/T-Interface | $0 |

**Figure 5-46.** S/T-Interface Nibble Register Map

### 5.4.1.1 S/T-Interface NR0

| b3 | b2 | b1 | b0 |
|---|---|---|---|
| *Software Reset*<br>rw | reserved | *Absolute Min Power*<br>rw | Return to Normal<br>rw |

**Figure 5-47.** S/T-Interface NR0 Bit Definitions

**Figure 5-47** names the bit fields in NR0. These fields are defined as follows:

- **Software Reset (b3)**—When NR0(b3) is 0, the MC145576 functions normally. When this bit = 1, a software reset is applied to the internal circuits of the S/T-Interface. The effect of the software reset is the equivalent of holding the external reset input low (hardware reset), except that NR0(b3–b0) is not reset. Thus, when this bit is set, all internal registers (except NR0) are returned to their initial state. Application of either a hardware or software reset has the effect of re-initializing all the internal registers; it does not prevent access to the SCP.
- **Absolute Minimum Power (b1)**—When this bit is 0, the MC145576 functions normally. When this bit = 1, the S/T-Interface enters a power conservation mode. In this mode a software reset is applied to the chip, all circuits are initialized, all clocking of the device is blocked, and the nonessential bias to the analog functions of the transceiver are removed such that the device consumes the absolute minimum amount of power. The transmit section of the chip is held in the INFO 0 state and IDL Tx is held in the *idle 1s* condition. This bit has no effect on the operation of the SCP. In this mode, only the SCP can operate.
- **Return to Normal (b0)**—When this bit is 0, the MC145576 functions normally. When this bit is 1, the following bits are reset:
  - BR11(b0) 96 KHz Test Signal
  - BR11(b1) External S/T Loopback
  - BR6(b7–b0)
  - BR8(b0) Single Pulse Test Signal

### 5.4.1.2 S/T-Interface NR1

| b3 | b2 | b1 | b0 |
|---|---|---|---|
| Activation Indication (AI)<br>ro | Error Indication (EI)<br>ro | Sleep Indication (SI)<br>ro | Frame Sync (FS)<br>ro |

**Figure 5-48.** S/T-Interface NR1 Bit Definitions

**Figure 5-48** names the bit fields in NR1. These fields are defined as follows:

- **Activation Indication (AI) (b3)**—This bit is set when the loop is fully activated, that is, when it is transmitting INFO 4 and receiving INFO 3.
- **Error Indication (EI) (b2)**—NR1(b2) is set to indicate an error condition has been detected by the activation state machine of the transceiver, as outlined in CCITT I.430, ETSI ETS 300012, and ANSI T1.605. The low-to-high level transition of the EI bit corresponds to the EI1 error indication reporting, while the high-to-low level transition of the EI bit corresponds to the EI2 error indication reporting recovery.

- **Sleep Indication (SI) (b1)—** NR1(b1) is set when the S/T-Interface is in Sleep mode.
- **Frame Sync (FS) (b0)—**NR1(b0) is set when frame synchronization is achieved. NR1(b0) is cleared whenever frame synchronization is lost.

### 5.4.1.3 S/T-Interface NR2

| *b3* | *b2* | *b1* | *b0* |
|---|---|---|---|
| *Activation Request (AR)* rw | *Deactivation Request (DR)* rw | *Activation Timer T1 Expired* rw | *Terminal Class* rw |

**Figure 5-49.** S/T-Interface NR2 Bit Definitions

**Figure 5-49** names the bit fields in NR2. These fields are defined as follows:

- **Activation Request (AR) (b3)—**When this bit = 1, an activation request input is passed to the activate state machine within the S/T transceiver, as outlined in CCITT I.430, ETSI ETS 300012, and ANSI T1.605. If the transceiver is in the idle state (i.e., transmitting and receiving INFO 0), then AR causes INFO 2 to be sent out on the transmit side of the S/T-Interface. This bit is returned low by the S/T-Interface after its active transition (low-to-high) is recognized by the activation/deactivation state machine of the transceiver to indicate recognition of the requested action.
- **Deactivate Request DR (b2)—**When this bit = 1, a deactivate request input is passed to the activation state machine within the S/T-Interface, as outlined in CCITT I.430, ETSI ETS 300012, and ANSI T1.605. The deactivate request input is used to initiate deactivation of the transmission loop. This bit is returned low by the S/T transceiver after its active transition (low-to-high) has been recognized by the activation/deactivation state machine of the transceiver to indicate recognition of requested action and that deactivation is proceeding.
- **Activation Timer Expired Input (b1)—**When this bit = 1, an activation timer expired input is passed to the activation state machine of the S/T-Interface. This bit corresponds to the Timer #1 expire input. These timers correspond to the activation timers outlined in CCITT I.430, ETSI ETS 300012, and ANSI T1.605. The timer expire input informs the activation/deactivation state machine that sufficient time has elapsed since the request to activate the loop and that attempts to do so should be abandoned. This bit is normally set by the controlling device and is automatically cleared when the MC145576 has activated the loop. This bit can be reset by hardware or a software reset.
- **Terminal Class (b0)—**When the MC145576 is configured for NT Terminal mode, this bit sets the class for D channel operation. When this bit is 0, the chip is set for class 1 operation. Alternatively, when this bit is 1, the chip is configured for class 2 operation. Class 1 and class 2 operations are as per CCITT I.430, ETSI ETS 300012, and ANSI T1.605 (i.e., class 1 is the higher class, used for signalling information, and class 2 is the lower class). The class can also be chosen externally by means of the CLASS/ECHO_IN pin. In this case, the class is chosen by the logical OR of the external pin and NR2(b0). NR2(b0) can be reset by a hardware or a software reset.

### 5.4.1.4 S/T-Interface NR3

| b3 | b2 | b1 | b0 |
|---|---|---|---|
| IRQ3 Rx Info changed<br>rw | IRQ2 Multiframe Reception<br>ro | IRQ6 FECV Detection<br>rw | IRQ1 Terminal D Collision<br>rw |

**Figure 5-50.** S/T-Interface NR3 Bit Definitions

**Figure 5-50** names the bit fields in NR3. These fields are defined as follows:

- **IRQ3 Change in Rx INFO State (b3)**—The interrupt request condition IRQ3 is generated whenever a change occurs in the received information state of the transceiver. This corresponds to a change in the receiving INFO 0, INFO 1, INFO 3, or INFO X state. Thus, when a change occurs in one of these states, the MC145576 internally sets this bit. An external interrupt occurs if Enable IRQ3 (NR4(b3)) is set. IRQ3 can be cleared by writing a 0 to NR3(b3).

**NOTE:** The transmission states (INFO 0, INFO 2, and INFO 4) are as defined in Section 3. INFO X is defined as any transmission state other than those states. An example of such a state would be when the MC145576 is programmed to transmit a 96 KHz test tone (BR11(b0) = 1). An INFO X state interrupt is generated only when receive INFO X state has persisted for > 8 ms. This avoids spurious interrupts during transient INFO X changes seen during activation but allows indication of prolonged INFO X conditions. The INFO X interrupt is repeated each 8 ms for as long as INFO X is detected.

- **IRQ2 Multiframe Reception (b2)**—This bit is for multiframe detection indication. Multiframing is initiated by the NT by setting BR7(b5). A multiframe is 20 basic frames or 5 ms in duration. If this interrupt is enabled by setting NR4(b2) and if multiframing is in progress, then an interrupt is generated on multiframe boundaries; i.e., every 5 ms. Alternatively, the MC145576 can be programmed to generate an interrupt only in the event of a new Q channel nibble having been received. A mutiframing interrupt is cleared by reading BR3. Reading BR3 clears the interrupt, regardless of whether the MC145576 is configured to generate an interrupt in the event of a new nibble or every multiframe.
- **IRQ6 FECV Detection (b1)**—The IRQ6 status bit is set when the MC145576 has detected a far-end code violation.
- **IRQ7 Terminal D Collision (b0)**—NR3(b0) is an interrupt bit used to indicate to external devices that a collision has occurred on the D channel. A D channel collision is considered to have occurred when both DREQUEST and DGRANT are high and the transmitted E echo bit to the TE does not match the previously input D bit on the DIN pin. The interrupt condition is cleared by writing a 0 to NR3(b0). This bit is maskable by means of NR4(b0).

### 5.4.1.5 S/T-Interface NR4

| *b3* | *b2* | *b1* | *b0* |
|---|---|---|---|
| IRQ3 Enable<br>rw | IRQ2 Enable<br>rw | IRQ6 Enable<br>rw | IRQ7 Enable<br>rw |

**Figure 5-51.** S/T-Interface NR4 Bit Definitions

**Figure 5-51** names the bit fields in NR4. These fields are defined as follows:

- **IRQ3 Enable (b3)**—NR4(b3) is an interrupt mask bit for IRQ3. When this bit is set high and IRQ3 is pending (i.e., NR3(b3) having been internally set to a 1), an interrupt is given to an external device by holding the IRQ* pin low. The IRQ* pin is held low until the interrupt condition is cleared by writing a 0 to NR3(b3). When the interrupt mask bit NR4(b3) is a 0, NR3(b3) cannot cause an interrupt to the external device.
- **IRQ2 Enable (b2)**—NR4(b2) is an interrupt mask bit for IRQ2. When this bit is set high and IRQ2 is pending (i.e., NR3(b2) having been internally set to a 1), an interrupt is given to an external device by holding the IRQ* pin low. The IRQ* pin is held low until the interrupt condition is cleared by reading BR3. When the interrupt mask bit (NR4(b2)) is a 0, NR3(b2) cannot cause an interrupt to the external device.
- **IRQ6 Enable (b1)**—NR4(b1) is an interrupt mask bit for IRQ6. When this bit is set high and IRQ6 is pending (i.e., NR3(b1) having been internally set to a 1), an interrupt is given to an external device by holding the IRQ* pin low. The IRQ* pin is held low until the interrupt condition is cleared by writing a 0 to NR3(b1). When the interrupt mask bit NR4(b1) is a 0, NR3(b1) cannot cause an interrupt to the external device.
- **IRQ7 Enable (b0)**—NR4(b0) is an interrupt mask bit for IRQ7. When this bit is set high and IRQ7 is pending (i.e., NR3(b0) having been internally set to a 1), an interrupt is given to an external device by holding the IRQ* pin low. The IRQ* pin is held low until the interrupt condition is cleared by writing a 0 to NR3(b0). When the interrupt mask bit NR4(b0) is a 0, NR3(b0) cannot cause an interrupt to the external device.

### 5.4.1.6 S/T-Interface NR5

| b3 | b2 | b1 | b0 |
|---|---|---|---|
| Idle B1 Channel TX at S/T-Interface<br>rw | Idle B2 Channel TX at S/T-Interface<br>rw | Invert B1 Channel to/from S/T-Interface<br>rw | Invert B2 Channel to/from S/T-Interface<br>rw |

**Figure 5-52.** S/T-Interface NR5 Bit Definitions

**Figure 5-52** names the bit fields in NR5. These fields are defined as follows:

- **Idle B1 Channel (b3)**—When NR5(b3) is 0, the MC145576 functions normally where data received in the B1 channel timeslot via the IDL/GCI is modulated onto the S/T-Interface in the B1 channel timeslot. When NR5(b3) is 1, data input on the IDL/GCI Rx pin in the B1 channel timeslot is ignored, and the *idle 1s* condition exists on the B1 channel timeslot on the S/T-Interface. Note that the default condition (i.e., after power-up or after a reset) for NR5(b3) is 0, thereby allowing the data received via the IDL/GCI interface to be modulated onto the transmission loop.
- **Idle B2 Channel (b2)**—When NR5(b2) is 0, the MC145576 functions normally, where data received in the B2 channel timeslot via the IDL/GCI is modulated onto the S/T transmission loop in the B2 channel timeslot. When NR5(b2) is 1, data input on the IDL/GCI Rx pin in the B2 channel timeslot is ignored, and the *idle 1s* condition exists on the B2 channel timeslot on the S/T transmission loop. Note that the default condition (i.e., after power-up or after a reset) for NR5(b2) is 0, thereby allowing the data received via the IDL/GCI interface to be modulated onto the transmission loop.
- **Invert B1 Channel (b1)**—When NR5(b1) is 0, the B1 channel data received via the IDL/GCI interface is transmitted normally on the transmission loop. When NR5(b1) = 1, the B1 channel data received via the IDL/GCI interface is inverted before entering the modulator portion of the S/T-Interface, prior to transmission on the S/T loop in the B1 timeslot. The selected B1 channel data received via the transmission loop is also inverted before being output on the IDL/GCI Tx output of the S/T-Interface when this function is invoked. This feature is useful in applications where it is required to use inverted data.
- **Invert B2 Channel (b0)**—When NR5(b0) is 0, the B2 channel data received via the IDL/GCI interface is transmitted normally on the transmission loop. When NR5(b0) is set, the B2 channel data received via the IDL/GCI interface is inverted before entering the modulator portion of the S/T-Interface prior to transmission on the S/T loop in the B2 timeslot. The selected B2 channel data received via the transmission loop is also inverted before being output on the IDL/GCI Tx output of the S/T-Interface when this function is invoked. This feature is useful in applications where inverted data is required.

### 5.4.1.7 S/T-Interface NR6

| b3 | b2 | b1 | b0 |
|---|---|---|---|
| 2B+D Transparent Loopback at S/T-Interface<br>rw | Fixed Timing Enable<br>rw | Sleep Power Down Mode Disable<br>rw | Swap B1/B2 at S/T-Interface<br>rw |

**Figure 5-53.** S/T-Interface NR6 Bit Definitions

**Figure 5-53** names the bit fields in NR6. These fields are defined as follows:

- **2B+D IDL/GCI Loopback (b3)**—When NR6(b3) is 0, the S/T-Interface functions normally. When NR6(b3) = 1, the B1, B2, and D channel data input on the IDL/GCI Rx input are buffered and returned to the IDL/GCI Tx output on the next IDL/GCI cycle. The output B1, B2, and D channel data is passed unchanged to the modulator portion of the transceiver and transmitted onto the S/T loop (i.e., the loopback is transparent).
- **Fixed Timing Enable (b2)**—When NR6(b2) is 0, the S/T-Interface is in Adaptive Timing mode. When NR6(b2) = 1, the S/T-Interface is in Fixed Timing mode. This register is ORed with the FIX pin.
- **Sleep Power Down Mode Disable (b1)**—When NR6(b1) is 0, the S/T-Interface is in Sleep Power Down mode. The Sleep state is exited either by setting NR6(b1) to 1, setting NR2(b3) to 1, or by the reception of a signal on the S/T loop.
- **Swap B1/B2 (b0)**—When NR6(b0) is 0, the timeslot assigned positions of the B1 and B2 channel data input and output via the IDL/GCI interface functions normally. When NR6(b0) = 1, the timeslot positions of the B1 and B2 channels are reversed (i.e., data entering the device on IDL/GCI Rx in the B1 timeslot is modulated onto the B2 timeslot) on the S/T loop. Data demodulated from the B2 timeslot from the S/T loop is output on IDL/GCI Tx in the B1 timeslot. The situation is analogous for B2 data entering the device on IDL/GCI Rx. This feature is useful in applications where a particular device (such as a codec filter) is hard-wired to a particular IDL/GCI timeslot and needs to gain access to the opposite B channel timeslot. NR6(b0) has no effect during a 2B+D IDL/GCI loopback.

**NOTE:** For example, if data entering the S/T-Interface by the IDL/GCI in the B1 channel is modulated onto the B2 channel on the S/T loop, then NR5(b3) must be set.

## 5.4.2 S/T Byte Registers

| Reg. | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Value after Reset |
|---|---|---|---|---|---|---|---|---|---|
| BR2 | SC1.1 | SC1.2 | SC1.3 | SC1.4 | Reserved | Reserved | Reserved | Reserved | $00 |
| BR3 | Q.1 | Q.2 | Q.3 | Q.4 | Q Qual | MF Int | Reserved | Tx B1/B2 Exchange | $F0 |
| BR4 | FV7 | FV6 | FV5 | FV4 | FV3 | FV2 | FV1 | FV0 | $00 |
| BR5 | BPV7 | BPV6 | BPV5 | BPV4 | BPV3 | BPV2 | BPV1 | BPV0 | $00 |
| BR6 | B1 S/T LB TP | B1 S/T LB NTP | B2 S/T LB TP | B2 S/T LB NTP | IDL B1 LB TP | IDL B1 LB NTP | IDL B2 LB TP | IDL B2 LB NTP | $00 |
| BR7 | ACT PR Disabled | D Ch PR Disabled | Enable MFrame | Invert E Channel | Always Active En | Reserved | LAPD Pol Cont | ACT T2 EXP | $00 |
| BR8 | reserved | CLKOUT (1) | CLKOUT (0) | Mute B1 from S/T | Mute B2 from S/T | Force E to zero | Force Tx INFO 2 | Tx single Pulse En | $00 |
| BR9 | TXSC2.1 | TXSC2.2 | TXSC2.3 | TXSC2.4 | TXSC3.1 | TXSC3.2 | TXSC3.3 | TXSC3.4 | $00 |
| BR10 | TXSC4.1 | TXSC4.2 | TXSC4.3 | TXSC4.4 | TXSC5.1 | TXSC5.2 | TXSC5.3 | TXSC5.4 | $00 |
| BR11 | *Do not react to Info 1* | *Do not react to Info 3* | Rx Info St Bit1 | Rx Info St Bit0 | Tx Info St Bit1 | Tx Info St Bit0 | Ext S/T Loopback | Tx 96K Test Signal | $00 |
| BR12 | NTTerm Disabled | **Stop/Go Disabled** | AR-U Disabled | *Overlay Enable* | En B1 Input | En B2 Input | En B1 Output | En B2 Output | $00 |

**Table 5-9.** S/T Byte Register Map

There are eleven byte registers (BR2 through BR12) in the MC145576.

### 5.4.2.1 S/T-Interface BR2

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| SC1.1 rw | SC1.2 rw | SC1.3 rw | SC1.4 rw | Reserved | Reserved | Reserved | Reserved |

**Figure 5-54.** S/T-Interface BR2 Bit Definitions

**Figure 5-54** names the bit fields in BR2.

- **Subchannel 1 (SC1) to S/T Loop (b7–b4)**—This nibble used for multiframing. These four bits correspond to subchannel 1 for transmission to the TE(s). Multiframing is initiated by the NT by setting BR7(b5). When multiframing is enabled, the NT transmits the bits in BR2(b7–b4) as subchannel 1, in accordance with CCITT I.430, ETSI ETS 300012, and ANSI T1.605. BR2(b7–b4), is internally polled at the start of every multiframe (this occurs every 5 ms and the device can be programmed to give an interrupt at the start of every multiframe), and its contents are interpreted as subchannel 1. If multiframing is enabled and the contents of BR2(b7–b4) have not been updated, then the subchannel is re-transmitted as is. BR2(b7–b4) can be updated any time between the 5 ms interrupts.

**NOTE:** BR2(b7) is the MSB of SC1 and BR2(b4) is the LSB.

### 5.4.2.2 S/T-Interface BR3

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| Q.1 ro | Q.2 ro | Q.3 ro | Q.4 ro | Q Bit Quality ro | Multiframe Interrupt rw | reserved | Tx B1/B2 Exchange rw |

**Figure 5-55.** S/T-Interface BR3 Bit Definitions

**Figure 5-55** names the bit fields in BR3.

- **Q Nibble from S/T Loop (b7–b4)**—These bits are used in the multiframing mode of operation. When multiframing has been enabled, these bits correspond to the received Q channel nibble from the TE(s). These bits are updated once every multiframe. The device can give an interrupt once every multiframe (see BR3(b2) and NR4(b2)) or every time a new Q channel nibble is received. BR3(b7–b4) are read only bits. Reading BR3 clears the multiframe interrupt.

**NOTE:** BR3(b7) is the MSB of the received Q channel nibble; BR3(b4) is the LSB.

- **Q Bit Quality (b3)**—This bit corresponds to the Q Bit Quality indication. When multiframing has been initiated by the NT, the TE(s) responds by sending Q data once every five frames. This Q data is transmitted in the Fa bit position. During the other four frames (i.e., when the TE(s) are not transmitting Q data), the Fa bit should be a 0. BR3(b3) being high indicates that the Fa bits in the frames where multiframing data was not being transmitted were 0s.
- **Multiframe Interrupt (b2)**—Programming of BR3(b2) dictates whether an interrupt is given every multiframe (assuming multiframing has been enabled and IRQ2 enable, NR4(b2), has been set), or only on the receipt of a new Q channel nibble from the TE(s). When BR3(b2) is 1, an interrupt is given every multiframe. When BR3(b2) is 0, an interrupt is given only on the receipt of a new Q channel nibble. Refer to Section 12 for a more detailed description.
- **Tx B1/B2 Exchange (b0)**—When BR3(b0) is 0, the B1 timeslot (and respectively, the B2 timeslot) from the IDL/GCI interface is modulated into the B1 timeslot (and respectively, the B2 timeslot) of the S/T loop. When BR3(b0) = 1, the B1 timeslot (and respectively, the B2 timeslot) from the IDL/GCI interface is modulated into the B2 timeslot (and respectively, the B1 timeslot) of the S/T-interface. The B1 and B2 timeslots from the S/T loop to the IDL/GCI output of the S/T-interface are not affected by this bit.

**NOTE:** BR3(b0) is used in association with BR6(b6) and BR6(b4) to provide and internal communication between two TEs.

### 5.4.2.3 S/T-Interface BR4

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| FV7 rw | FV6 rw | FV5 rw | FV4 rw | FV3 rw | FV2 rw | FV1 rw | FV0 rw |

**Figure 5-56.** S/T-Interface BR4 Bit Definitions

**Figure 5-56** names the bit fields in BR4.

- **Frame Violation Counter (b7–b0)**—This is a read/write register, thereby allowing the user to program the counter to a predetermined value. The counter is initialized to 100 by a hardware/software reset. Note that the counter, upon reaching a value of FF, does not roll over ( i.e., it remains at FF until the user rewrites a starting value). Note that BR4(b7) is the MSB of the counter and BR4(b0) is the LSB.

Recommendation CCITT I.430, ETSI ETS 300012, and ANSI T1.605 specifications state that there must be two AMI violations in every S/T frame. The F bit is the first violation and the succeeding violation must occur within 13 bauds for and NT configuration. BR4(b7–b0) is the output of an 8-bit binary counter. This counter counts the number of frames which do not contain the correct number of AMI violations. Note that in multiframing, it is possible to have a frame which does not contain the correct number of violations (Fa = 1, B1 = 1). The MC145576, when in multiframe mode, does not count these frames. Thus, this counter is a *frame error* counter, counting the number of frames which do not contain the correct number of AMI violations. BR4(b7–b0) only counts frames not containing the correct number of AMI violations after FSYNC has been achieved, and ceases counting whenever FSYNC is lost.

### 5.4.2.4 S/T-Interface BR5

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| BPV7 rw | BPV6 rw | BPV5 rw | BPV4 rw | BPV3 rw | BPV2 rw | BPV1 rw | BPV0 rw |

**Figure 5-57.** S/T-Interface BR5 Bit Definitions

**Figure 5-57** names the bit fields in BR5.

- **BPV Counter (b7–b0)**—This register is the output of an 8-bit binary counter that records the number of unbalanced frames. A frame in which the total number of positive pulses is different from the total number of negative pulses constitutes an unbalanced frame. It is a read/write register, thereby allowing the user to program the counter to a predetermined value. The counter is initialized to 100 by a hardware/software reset. Note that the counter, upon reaching a value of FF, does not roll over (i.e., it remains at FF until the user rewrites a starting value). Note that BR5(b7) is the MSB of the counter and BR5(b0) is the LSB.

### 5.4.2.5 S/T-Interface BR6

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| B1 S/T Loopback Transparent<br>rw | B1 S/T Loopback Non-Transparent<br>rw | B2 S/T Loopback Transparent<br>rw | B2 S/T Loopback Non-Transparent<br>rw | IDL/GCI B1 Loopback Transparent<br>rw | IDL/GCI B1 Loopback Non-Transparent<br>rw | IDL/GCI B2 Loopback Transparent<br>rw | IDL/GCI B2 Loopback Non-Transparent<br>rw |

**Figure 5-58.** S/T-Interface BR6 Bit Definitions

**Figure 5-58** names the bit fields in BR6.

- **B1 S/T Loopback Transparent (b7)**—When this bit is 0, the device functions normally. When this bit is 1, the device enters a *B1 S/T Loopback Transparent Mode*. In this mode, data entering the device from RxP/PxN in the B1 timeslot is demodulated and remodulated back out on TxP/TxN in the B1 timeslot. The demodulated B1 data continues to present itself on IDL/GCI Tx in the B1 timeslot (hence, the term *transparent*). Data entering the part from IDL/GCI Rx in the B1 timeslot is ignored. This bit is reset to 0 by either a software reset, a hardware reset, or in the *return to normal* mode (NR0(b0) = 1).
- **B1 S/T Loopback Non-Transparent (b6)**—When this bit is 0 the device functions normally. When this bit is 1, the device enters a *B1 S/T Loopback Non-Transparent Mode*. In this mode, data entering the device from RxP/RxN in the B1 timeslot is demodulated and remodulated back out on TxP/TxN in the B1 timeslot. Data entering the part from IDL/GCI Rx in the B1 timeslot is ignored. IDL/GCI Tx ignores the demodulated B1 data, presenting in its stead the *idle 1s* condition in the IDL/GCI Rx B1 timeslot (hence, the term *non-transparent*). This bit is reset to 0 by either a software reset, a hardware reset, or in the *return to normal* mode (NR0(b0) = 1).
- **B2 S/T Loopback Transparent (b5)**—When this bit is 0, the device functions normally. When this bit is 1, the device enters a *B2 S/T Loopback Transparent Mode*. In this mode, data entering the device from RxP/RxN in the B2 timeslot is demodulated and remodulated back out on TxP/TxN in the B2 timeslot. The demodulated B2 data continues to present itself on IDL/GCI Tx in the B2 timeslot (hence, the term *transparent*). Data entering the part from IDL/GCI Rx in the B2 timeslot is ignored. This bit is reset to 0 by either a software reset, a hardware reset, or in the *return to normal* mode (NR0(b0) = 1).
- **B2 S/T Loopback Non-Transparent (b4)**—When this bit is 0, the device functions normally. When this bit is 1, the device enters a *B2 S/T Loopback Non-Transparent Mode*. In this mode, data entering the device from RxP/RxN in the B2 timeslot is demodulated and remodulated back out of TxP/TxN in the B2 timeslot. Data entering the part from IDL/GCI Rx in the B2 timeslot is ignored. IDL/GCI Tx ignores the demodulated B2 data, presenting in its stead the *idle 1s* condition in the IDL/GCI Rx B2 timeslot (hence, the term *non-transparent*). This bit is reset to 0 by either a software reset, a hardware reset, or in the *return to normal* mode (NR0(b0) = 1).

- **IDL/GCI B1 Loopback Transparent (b3)**—When this bit is a 0, the MC145576 operates normally. When this bit is a 1, the MC145576 internally loops back the data received during the B1 timeslot at DIN and transmits it onto the DOUT pin during the B1 timeslot. Data entering the DIN pin during the B1 timeslot is also transmitted onto the S/T-Interface. This bit is reset to 0 by either a software reset, a hardware reset, or in the *return to normal* mode (NR0(b0) = 1).
- **IDL/GCI B1 Loopback Non-Transparent (b2)**—When this bit is a 0, the MC145576 operates normally. When this bit is a 1, the MC145576 internally loops back the data received during the B1 channel timeslot at DIN and transmits it onto the DOUT pin during the B1 timeslot. Data entering the DIN pin during the B1 timeslot is not transmitted onto the S/T-Interface. Instead, the MC145576 transmits idle 1s onto the B1 channel bits of the S/T-Interface. This bit is reset to 0 by either a software reset, a hardware reset, or in the *return to normal* mode (NR0(b0) = 1).
- **IDL/GCI B2 Loopback Transparent (b1)**—When this bit is a 0, the MC145576 operates normally. When this bit is a 1, the MC145576 internally loops back the data received during the B2 channel timeslot at DIN and transmits it onto the DOUT pin during the B2 timeslot. Data entering the DIN pin during the B2 timeslot is also transmitted onto the S/T-Interface. This bit is reset to 0 by either a software reset, a hardware reset, or in the *return to normal* mode (NR0(b0) = 1).
- **IDL/GCI B2 Loopback Non-Transparent (b0)**—When this bit is a 0, the MC145576 operates normally. When this bit is a 1, the MC145576 internally loops back the data received during the B2 channel timeslot at DIN and transmits it onto the DOUT pin during the B2 timeslot. Data entering the DIN pin during the B2 timeslot is not transmitted onto the S/T-Interface. Instead, the MC145576 transmits idle 1s onto the B2 channel bits of the S/T-Interface. This bit is reset to 0 by either a software reset, a hardware reset, or in the *return to normal* mode (NR0(b0) = 1).

#### 5.4.2.6 S/T-Interface BR7

| *b7* | *b6* | *b5* | *b4* | *b3* | *b2* | *b1* | *b0* |
|---|---|---|---|---|---|---|---|
| Activation Procedures Disabled<br>rw | D Channel Procedures Disabled<br>rw | Enable Multi-framing<br>rw | Invert E Channel<br>rw | Always Active Enable<br>rw | Reserved | LAPD Polarity Control<br>rw | Activation Timer #2 Expired<br>rw |

**Figure 5-59.** S/T-Interface BR7 Bit Definitions

**Figure 5-59** names the bit fields in BR7.

- **Activation Procedures Disabled (b7)**—When this bit is 0, the MC145576 functions normally. When this bit = 1, the transmit section of the transceiver is forced into the highest information state. Thus, INFO 4 is forced out on the transmit side of the device. INFO 4 is forced out regardless of what is being received on RxP/RxN. In the event that INFO 0 is being received, the transmitted INFO 3 is transmitted asynchronously. If either INFO 2 or INFO 4 are subsequently received, then the TE's INFO 3 aligns itself to the received signal in accordance with CCITT I.430, ETSI ETS 300012, and ANSI T1.605.

**NOTE:** A TE wakes up if it receives either INFO 2 or INFO 4 from the NT. However, an NT transmitting INFO 0 does not wake up to the reception of INFO 3 from the TE. For an NT to be woken up by a TE, it must first receive INFO 1 from the TE and then proceed to go through the subsequent handshaking.

- **D Channel Procedures Disabled (b6)**—This bit is used to enable/disable D channel contention procedures in accordance with the CCITT I.430, ETSI ETS 300012, and ANSI T1.605. When this bit is 0, the D channel procedures are adhered to as per the DREQUEST, DGRANT, and CLASS pin descriptions. When this bit is 1, the D channel procedures are ignored, allowing the data present in the D channel on IDL/GCI Rx to be modulated regardless of the status of DREQUEST and DGRANT. BR7(b6) = 1 causes the NT terminal to disregard the demodulated E echo bits. The NT terminal's D data is processed regardless.
- **Enable Multiframing (b5)**—This bit is used to enable/disable multiframing in accordance with CCITT I.430, ETSI ETS 300012, and ANSI T1.605. When this bit is 0, multiframing is disabled. In this mode the M, Fa, and S bauds transmitted from the NT is 0. When this bit is 1, multiframing is enabled. In this mode, the M, Fa, and S bauds adheres to the multiframing coding rules as outlined in CCITT I.430 and ANSI T1.605.
- **Invert Echo Channel (b4)**—This bit is used to determine the polarity of the transmitted echo channel from the NT to the TE. When this bit is a 0, the transmitted E bit is the same as the previously demodulated D bit from the TE(s). When this bit is 1, the transmitted E bit is the logical inverse of the previously demodulated D bit.
- **Always Active Enable (b3)**—This bit enables the *active only* NT mode. In this mode, the S/T-interface is restricted to the G2 or G3 state (i.e., the device is either activated or attempting to activate). The device is never allowed to fully deactivate.
- **LAPD Polarity Control (b1)**—When the MC145576 is configured in Terminal Mode, this bit performs the *LAPD Polarity Control* function. When this bit is 0, the active state of DREQUEST and DGRANT signals is defined to be the logic 1 or high state. When this bit is 1, the active state of these signals is defined to be the logic 0 or low state.
- **Activation Timer #2 Expired (b0)**—This bit performs the *Activation Timer #2 Expired* function. When this bit is 0, the NT-configured S/T transceiver uses a value of 50 ms for the Timer #2 value outlined in CCITT I.430, ETSI ETS 300012, and ANSI T1.605 (i.e., the device unambiguously detects INFO 1). When this bit is 1, a value of 100 ms is used for the value of Timer #2.

### 5.4.2.7 S/T-Interface BR8

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| reserved | CLKOUT1<br>rw | CLKOUT0<br>rw | Mute B1 from S/T<br>rw | Mute B2 from S/T<br>rw | Force E to Zero<br>rw | Force Transmit INFO2<br>rw | Transmit Single Pulse Enable<br>rw |

**Figure 5-60.** S/T-Interface BR8 Bit Definitions

**Figure 5-60** names the bit fields in BR8.

- **CLKOUT (b6–b5)** — These bits determine the frequency of CLKOUT.
  - 00 = 20.48 MHz (default)
  - 01 = 10.24 MHz
  - 10 = 5.12 MHz
  - 11 = 0 MHz

**NOTE:** CLKOUT is not available during a hardware reset.

- **Mute B1 from S/T-Interface (b4)** — When this bit is 0, the device functions normally. When this bit is 1, the data transmitted on the B1 channel on IDL/GCI Tx is forced to the *idle 1s* condition.
- **Mute B2 from S/T-Interface (b3)** — When this bit is 0, the device functions normally. When this bit is 1, the data transmitted on the B2 channel on IDL/GCI Tx is forced to the *idle 1s* condition.
- **Force Echo Channel to Zero (b2)** — When this bit is 0, the device functions normally. When this bit is 1, the S/T-Interface forces the transmitted E bits to be 0. This feature is used when the NT wishes to communicate to the TEs on the passive bus that they should disengage from the D channel.
- **Force Tx INFO2 (b1)** — This bit is used when the S/T loop is fully activated (INFO 3/INFO 4) and the S/T-Interface want to resynchronize all the TEs. By setting BR8(b1) to 1, the S/T-Interface replaces INFO 4 with INFO 2 to resynchronize the INFO 3 sent by the TEs. At the reception of the new INFO3, the S/T-Interface sends back INFO 4.

**NOTE:** The S/T-Interface returns this bit low after its active transition (low-to-high) is recognized.

- **Transmit Single Pulse Enable (b0)** — When this bit is 0, the MC145576 functions normally. When this bit is 1, the device transmits frames with one positive and one negative single pulse on the TxP-T/TxN-T pins. This signal can be used for test purposes. The single pulse test signal qualifies as a Transmit INFO X state. The bit is reset to 0 by either a software or hardware reset of in the Return to Normal mode (NR0(b0) = 1).

**NOTE:** In GCI mode, this bit is ORed with the $\overline{\text{PULSE2}}$ signal.

### 5.4.2.8 S/T-Interface BR9

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| TXSC2.1 wo | TXSC2.2 wo | TXSC2.3 wo | TXSC2.4 wo | TXSC3.1 wo | TXSC3.2 wo | TXSC3.3 wo | TXSC3.4 wo |

**Figure 5-61.** S/T-Interface BR9 Bit Definitions

**Figure 5-61** names the bit fields in BR9.

- **SC2 to Loop (b7–b4)**—This nibble is used for multiframing. These four bits correspond to subchannel 2 for transmission to the TE(s). Multiframing is initiated by the NT by setting BR7(b5). When multiframing is enabled, the NT transmits the bits in BR9(b7–b4) as subchannel 2, in accordance with CCITT I.430, ETSI ETS 300012, and ANSI T1.605. BR9(b7–b4), are internally polled at the start of every multiframe (this occurs every 5 ms and the device can be programmed to give an interrupt at the start of every multiframe), and the contents are interpreted as subchannel 2. If multiframing is enabled and the contents of BR9(b7–b4) have not been updated, the subchannel is re-transmitted as is. BR9(b7–b4) can be updated any time between the 5 ms interrupts.

**NOTE:** BR9(b7) is the MSB of SC2 and BR9(b4) is the LSB.

- **SC3 to Loop (b3–b0)**—This nibble is used for multiframing. These four bits correspond to subchannel 3 for transmission to the TE(s). When multiframing is enabled, the NT transmits the bits in BR9(b3–b0) as subchannel 3, in accordance with CCITT I.430, ETSI ETS 300012, and ANSI T1.605. BR9(b3–b0) are internally polled at the start of every multiframe (this occurs every 5 ms and the device can be programmed to give an interrupt at the start of every multiframe), and the contents are interpreted as subchannel 3. If multiframing is enabled and the contents of BR9(b3–b0) have not been updated, the subchannel is re-transmitted as is. BR9(b3–b0) can be updated any time between the 5 ms interrupts.

**NOTE:** BR9(b3) is the MSB of SC3 and BR9(b0) is the LSB.

### 5.4.2.9 S/T-Interface BR10

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| TXSC4.1 wo | TXSC4.2 wo | TXSC4.3 wo | TXSC4.4 wo | TXSC5.1 wo | TXSC5.2 wo | TXSC5.3 wo | TXSC5.4 wo |

**Figure 5-62.** S/T-Interface BR10 Bit Definitions

**Figure 5-62** names the bit fields in BR10.

- **SC4 to Loop (b7–b4)**—This nibble is used for multiframing. These four bits correspond to subchannel 4 for transmission to the TE(s). When multiframing is enabled, the NT transmits the bits in BR10(b7–b4) as subchannel 4, in accordance with CCITT I.430, ETSI ETS 300012, and ANSI T1.605. BR10(b7–b4) are internally polled at the start of every multiframe (this occurs every 5 ms and the device can be programmed to give an interrupt at the start of every multiframe), and the contents are interpreted as subchannel 4. If multiframing is enabled and the contents of BR10(b7–b4) have not been updated, the subchannel is re-transmitted as is. BR10(b7–b4) can be updated any time between the 5 ms interrupts.

**NOTE:** BR10(b7) is the MSB of SC4 and BR10(b4) is the LSB.

- **SC5 to Loop (b3–b0)**—This nibble is used for multiframing. These four bits correspond to subchannel 5 for transmission to the TE(s). When multiframing is enabled, the NT transmits the bits in BR10(b3–b0) as subchannel 5, in accordance with CCITT I.430, ETSI ETS 300012, and ANSI T1.605. BR10(b3–b0) is internally polled at the start of every multiframe (this occurs every 5 ms and the device can be programmed via NR4(b2) to give an interrupt at the start of every multiframe), and the contents are interpreted as subchannel 5. If multiframing is enabled and the contents of BR10(b3–b0) have not been updated, the subchannel is re-transmitted as is. BR10(b3–b0) can be updated any time between the 5 ms interrupts.

**NOTE:** BR10(b3) is the MSB of SC5 and BR10(b0) is the LSB.

### 5.4.2.10 S/T-Interface BR11

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| *Do Not React To INFO 1* rw | *Do Not React To INFO 3* rw | Rx INFO State B1 rw | Rx INFO State B0 rw | Tx INFO State B1 rw | Tx INFO State B0 rw | External S/T Loopback rw | Transmit 96 KHz Test Signal rw |

**Figure 5-63.** S/T-Interface BR11 Bit Definitions

**Figure 5-63** names the bit fields in BR11.

- **Do Not React to INFO 1 (b7)**—This bit is only applicable to the IDL mode of operation. When this bit is 0, the part functions normally. When this bit is 1, the NT does not react to INFO 1 from the TE. (Note, however, that the NT gives an interrupt indicating a change in received information state.) Only when the NT clears this bit does it react to INFO 1. This feature is used in the NT in applications where it is necessary to delay activation of the S/T loop until the U link has reached its active state.
- **Do Not React to INFO 3 (b6)**—This bit is only applicable to the IDL mode of operation. When this bit is 0, the part functions normally. When this bit is 1, the NT does not react to INFO 3 from the TE (this INFO 3 from the TE being the response of the TE to INFO 2 from the NT). Only when the NT resets this bit does it react to INFO 3. In the meantime, the NT continues to transmit INFO 2. This feature is used in the NT in applications where it is necessary to delay activation of the S/T loop until the U link has reached its active state.
- **Rx INFO State B1 and B0 (b5, b4)**—The MC145576 internally sets these bits to indicate the status of the received signal (i.e., it is INFO 0, 1, 3, or X, where INFO X is none of the above). An example of INFO X would be when it is receiving the 96 KHz test signal. Another example of INFO X would be where the transceiver is not receiving INFO 0, but it has not yet determined whether it is INFO 1 or 3. The codes corresponding to the different states are shown in **Table 5-10**.

**Table 5-10.** Rx INFO State Codes

| BR11(b5) | BR11(b4) | Receive Information State |
|---|---|---|
| 0 | 0 | INFO 0 |
| 0 | 1 | INFO 1 |
| 1 | 0 | INFO 3 |
| 1 | 1 | INFO X |

- **Tx INFO State B1 and B0 (b3, b2)**—The MC145576 sets these bits internally to indicate the status of the transmitted signal (i.e., it is INFO 0, 1, 3, or X, where INFO X is none of the above). An example of INFO X would be when it is transmitting the 96 KHz test signal. The codes corresponding to the different states is shown in **Table 5-11**.

**Table 5-11.** Tx INFO State Codes

| BR11(b3) | BR11(b2) | Receive Information State |
|---|---|---|
| 0 | 0 | INFO 0 |
| 0 | 1 | INFO 2 |
| 1 | 0 | INFO 4 |
| 1 | 1 | INFO X |

- **External S/T Loopback (b1)**—When this bit is 0, the MC145576 functions normally. If the transmit pair is shorted to the receive pair while this bit is 1, the device performs an external or analog loopback. In an analog loopback, the device demodulates its own transmitted data. The transceiver should have its activation procedures disabled (BR7(b7) = 1) and be configured for the IDL/GCI master mode (BR7(b3) = 1). This feature is useful for test purposes. In external loopback, the B1, B2, and D channels are looped back.
- **Transmit 96 KHz Test Signal (b0)**—When this bit is 0, the MC145576 functions normally. When this bit is 1, the device transmits a 96 KHz square wave test signal on TxP/TxN. This signal can be used for test purposes. This 96 KHz test signal qualifies as a *Transmit INFO X* state. Correspondingly, the MC145576 receiving the 96 KHz test signal is in the *Receive INFO X* state. This bit is cleared by either a software or hardware reset or in the Return to Normal mode (NR0(b0) = 1). Before setting BR11(b1) to 1, the S/T-Interface should be out of Sleep mode (NR6(b1) = 1).

**NOTE:** In GCI mode, this bit is ORed with the $\overline{\text{PULSE1}}$ signal.

### 5.4.2.11 S/T-Interface BR12

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| NT Term Disabled<br>rw | **Stop/Go Disabled**<br>rw | ARU Disabled<br>rw | *Overlay Enable*<br>rw | Enable B1 Input<br>rw | Enable B2 Input<br>rw | Enable B1 Output<br>rw | Enable B2 Output<br>rw |

**Figure 5-64.** S/T-Interface BR12 Bit Definitions

**Figure 5-64** names the bit fields in BR12.

- **NT Terminal Mode Disabled (b7)**—When this bit is 0, the MC145576 operates in NT Terminal mode. When this bit is 1, the MC145576 operates in TDM mode if OR6(b4) = 0 or in TSA mode if OR6(b4) = 1.

**NOTE:** OR6(b4) has no effect if BR12(b7) = 0.

- **Stop/Go Disabled (b6)**—This bit is only used in GCI NT Terminal mode using a 2.068 MHz clock. In this mode, the S/G bit provides the availability of the D channel on the S/T loop. If the bit is 1, the D channel is not available (Stop). If the bit is 0, the D channel is available (Go). When BR12(b6) = 1, the S/G bit is not available on the GCI frame.
- **ARU Disable (b5)**—When this bit is 0, the MC145576 functions normally. When the U-Interface is not active, writing a 1 to this bit disables the Activate Request for the U-Interface input signal (pin 10).
- **Overlay Enable (b4)**—When this bit is 0, the MC145576 functions normally. When this bit is 1, the S/T-Interface substitutes Overlay Registers OR0–OR7 for BR0–BR7. This bit is reset by both hardware and software resets.

**NOTE:** BR0–BR1 are not listed in the descriptions in this section because the Byte Register locations are reserved except when the Overlay Registers are enabled.

- **Enable B1 Input (b3)**—In NT Terminal mode, this bit controls the input of the B1 channel from the DIN pin. When BR12(b3) is 1, the B1 channel coming from the DIN pin into the MC145576 is transferred to the U-Interface.
- **Enable B2 Input (b2)**—In NT Terminal mode, this bit controls the input of the B2 channel from the DIN pin. When BR12(b2) is 1, the B2 channel coming from the DIN pin into the MC145576 is transferred to the U-Interface.
- **Enable B1 Output (b1)**—In NT Terminal mode, this bit controls the output of the B1 channel to the DOUT pin. When BR12(b1) is 0, the DOUT pin outputs 1s on the B1 channel (or is high impedance if S/T-OR6(b0) = 1). When BR12(b1) is 1, the B1 channel coming from the U-Interface is directed to the DOUT pin.
- **Enable B2 Output (b0)**—In NT Terminal mode, this bit controls the output of the B2 channel to the DOUT pin. When BR12(b0) is 0, the DOUT pin outputs 1s on the B2 channel (or is high impedance if S/T-OR6(b0) = 1). When BR12(b0) is 1, the B2 channel coming from the U-Interface is directed to the DOUT pin.

### 5.4.3 S/T Overlay Registers

The overlap map is enabled by setting the enable bit BR12(b4). The Overlay Registers then replace the Byte registers BR0 to BR7 as described below. The reverse action is achieved by clearing the enable bit BR12(b4). These Overlay Registers are available in SCP mode only.

| Reg. | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|
| OR0 | *DIN B1 Channel Timeslot Bits (7–0)* | | | | | | | |
| OR1 | *DIN B2 Channel Timeslot Bits (7–0)* | | | | | | | |
| OR2 | *DIN D Channel Timeslot Bits (7–0)* | | | | | | | |
| OR3 | *DOUT B1 Channel Timeslot Bits( 7–0)* | | | | | | | |
| OR4 | *DOUT B2 Channel Timeslot Bits( 7–0)* | | | | | | | |
| OR5 | *DOUT D Channel Timeslot Bits( 7–0)* | | | | | | | |
| OR6 | *TSA B1 Enable* | *TSA B2 Enable* | *TSA D Enable* | *TSA Mode Enable* | reserved | reserved | reserved | *IDL DOUT Open drain Enable* |
| OR7 | reserved | *B1 U Int* | *B2 U Int* | *D U Int* | reserved | *B1S/T Int* | *B2 S/T Int* | *D S/T Int* |

**Figure 5-65.** S/T Overlay Register Map

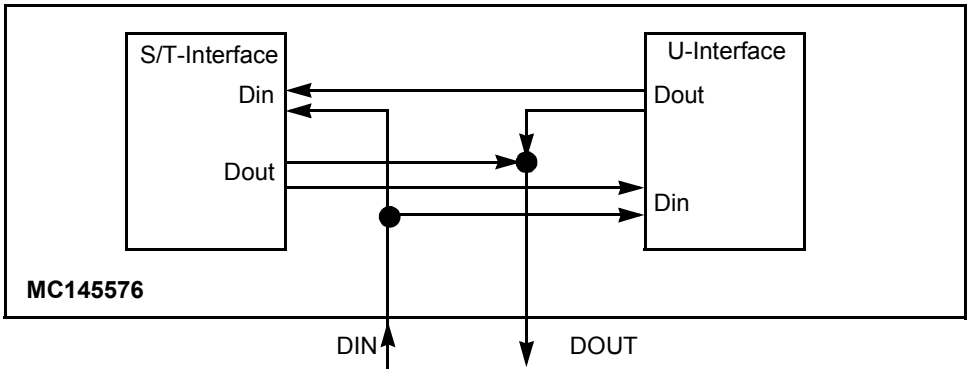



**Figure 5-66.** DIN and DOUT Internal Routing in Timeslot Assigner Mode

### 5.4.3.1 S/T-Interface OR0

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| DIN B1 Channel Timeslot Bits (7–0) | | | | | | | |
| rw | | | | | | | |

**Figure 5-67.** S/T-Interface OR0 Bit Definitions

**Figure 5-67** names the bit fields in OR0. These bits are:

- **DIN B1 Channel Timeslot (b7–b0)**—This register allows the B1 channel timeslot input to the Din input of the S/T-Interface to be allocated 1 of 256 start points, corresponding to each 2-bit boundary defined by the DCL clock. The default value for OR0 is $00.

### 5.4.3.2 S/T-Interface OR1

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| DIN B2 Channel Timeslot Bits (7–0) | | | | | | | |
| rw | | | | | | | |

**Figure 5-68.** S/T-Interface OR1 Bit Definitions

**Figure 5-68** names the bit fields in OR1. These bits are:

- **DIN B2 Channel Timeslot (b7–b0)**—This register allows the B2 channel timeslot input to the Din input of the S/T-Interface to be allocated 1 of 256 start points, corresponding to each 2-bit boundary defined by the DCL clock. The default value for OR1 is $00.

### 5.4.3.3 S/T-Interface OR2

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| DIN D Channel Timeslot Bits (7–0) | | | | | | | |
| rw | | | | | | | |

**Figure 5-69.** S/T-Interface OR2 Bit Definitions

**Figure 5-69** names the bit fields in OR2. These bits are:

- **DIN D Channel Timeslot (b7–b0)**—This register allows the D channel timeslot input to the Din input of the S/T-Interface to be allocated 1 of 256 start points, corresponding to each 2-bit boundary defined by the DCL clock. The default value for OR2 is $00.

### 5.4.3.4 S/T-Interface OR3

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| *DOUT B1 Channel Timeslot Bits (7–0)* | | | | | | | |
| rw | | | | | | | |

**Figure 5-70.** S/T-Interface OR3 Bit Definitions

**Figure 5-70** names the bit fields in OR3. These bits are:

- **DOUT B1 Channel Timeslot (b7–b0)**—This register allows the B1 channel timeslot output from the Dout output of the S/T-Interface to be allocated 1 of 256 start points, corresponding to each 2-bit boundary defined by the DCL clock. The default value for OR3 is $00.

### 5.4.3.5 S/T-Interface OR4

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| *DOUT B1 Channel Timeslot Bits (7–0)* | | | | | | | |
| rw | | | | | | | |

**Figure 5-71.** S/T-Interface OR4 Bit Definitions

**Figure 5-71** names the bit fields in OR4. These bits are:

- **DOUT B2 Channel Timeslot (b7–b0)**—This register allows the B2 channel timeslot output from the Dout output of the S/T-Interface to be allocated 1 of 256 start points, corresponding to each 2-bit boundary defined by the DCL clock. The default value for OR4 is $00.

### 5.4.3.6 S/T-Interface OR5

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| *DOUT D Channel Timeslot Bits (7–0)* | | | | | | | |
| rw | | | | | | | |

**Figure 5-72.** S/T-Interface OR5 Bit Definitions

**Figure 5-72** names the bit fields in OR5. These bits are:

- **DOUT D Channel Timeslot (b7–b0)**—This register allows the D channel timeslot output from the Dout output of the S/T-Interface to be allocated 1 of 256 start points, corresponding to each 2-bit boundary defined by the DCL clock. The default value for OR5 is $00.

**NOTE:** To validate the signal sent by the pin TDCLK (pin 44), the D channel timeslot programmed in OR5 should be different from the B1 and B2 channel timeslots programmed in OR3 and OR4, even if the B1 and B2 timeslots are not enabled.

### 5.4.3.7 S/T-Interface OR6

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| *TSA B1 Enable* rw | *TSA B2 Enable* rw | *TSA D Enable* rw | *TSA Mode Enable* rw | reserved | reserved | reserved | *IDL DOUT Open Drain Enable* rw |

**Figure 5-73.** S/T-Interface OR6 Bit Definitions

**Figure 5-34** names the bit fields in OR6. These bits are:

- **Control Register, TSA B1 Enable (b7)**—This bit is used to enable the B1 channel in IDL timeslot mode. The B1 timeslot is defined through the OR0 and OR3 registers. Whenever TSA is enabled for timeslot mode, all channels enter timeslot mode. If in timeslot mode and TSA B1 enable is a 0, then the B1 channel is not present on DOUT, and the transmit data on the S/T-Interface is forced to all 1s and the DOUT output from the S/T-Interface is high impedance.
- **Control Register, TSA B2 Enable (b6)**—This bit is used to enable the B2 channel in IDL timeslot mode. The B2 timeslot is defined through OR1 and OR4 registers. Whenever TSA is enabled for timeslot mode, all channels enter timeslot mode. If in timeslot mode and TSA B2 enable is a 0, then the B2 channel is not present on DOUT, and the transmit data on the S/T-Interface is forced to all 1s and the DOUT output from the S/T-Interface is high impedance.
- **Control Register, TSA D Enable (b5)**—This bit is used to enable the D channel in IDL timeslot mode. The D timeslot is defined through the OR2 and OR5 registers. Whenever TSA is enabled for timeslot mode, all channels enter timeslot mode. If in timeslot mode and TSA D enable is a 0, then the D channel is not present on DOUT, and the transmit data on the S/T-Interface is forced to all 1s and the DOUT output from the S/T-Interface is high impedance.
- **Control Register, TSA Mode Enable (b4)**—This bit is used to enable the IDL Timeslot Assigned mode of both the U- and S/T-Interfaces. This bit has no effect if BR12(b7) = 0.
- **DOUT Open Drain (b0)**—This bit configures the DOUT pin as an open drain when set to a 1. When this bit = 0, the DOUT pin goes to high impedance between B and D channels.

**NOTE:** Whenever bit b7, b6, or b5 is enabled, the MC145576 enters TSA mode, but to validate the TSA mode for the U-Interface, OR6(b4) should always be set to 1.

### 5.4.3.8 S/T-Interface OR7

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| Reserved | B1 U-Interface rw | B2 U-Interface rw | D U-Interface rw | Reserved | B1 S/T-Interface rw | B2 S/T-Interface rw | D S/T-Interface rw |

**Figure 5-74.** S/T-Interface OR7 Bit Definitions

**Figure 5-34** names the bit fields in OR7. These bits are:

- **B1 U-Interface (b6)**—This bit selects the location of the B1 channel to be transferred to the U loop. If OR7(b6) is 0, the B1 channel from the DIN pin is selected. If OR7(b6) is 1, the B1 channel from the Dout of the S/T-Interface is selected. The default value for OR7(b6) is 0.
- **B2 U-Interface (b5)**—This bit selects the location of the B2 channel to be transferred to the U loop. If OR7(b5) is 0, the B2 channel from the DIN pin is selected. If OR7(b5) is 1, the B2 channel from the Dout of the S/T-Interface is selected. The default value for OR7(b5) is 0.
- **D U-Interface (b4)**—This bit selects the location of the D channel to be transferred to the U loop. If OR7(b4) is 0, the D channel from the DIN pin is selected. If OR7(b4) is 1, the D channel from the Dout of the S/T-Interface is selected. The default value for OR7(b4) is 0.
- **B1 S/T-Interface (b2)**—This bit selects the location of the B1 channel to be transferred to the S/T loop. If OR7(b2) is 0, the B1 channel from the DIN pin is selected. If OR7(b2) is 1, the B1 channel from the Dout of the U-Interface is selected. The default value for OR7(b2) is 0.
- **B2 S/T-Interface (b1)**—This bit selects the location of the B2 channel to be transferred to the S/T loop. If OR7(b1) is 0, the B2 channel from the DIN pin is selected. If OR7(b1) is 1, the B2 channel from the Dout of the U-Interface is selected. The default value for OR7(b1) is 0.
- **D S/T-Interface (b0)**—This bit selects the location of the D channel to be transferred to the S/T loop. If OR7(b0) is 0, the D channel from the DIN pin is selected. If OR7(b0) is 1, the D channel from the Dout of the U-Interface is selected. The default value for OR7(b0) is 0.

# 6

# SCP Mode Device Functionality

## 6.1 Introduction

The MC145576 is equipped with an industry standard Serial Control Port Interface (SCP). The serial control is used by an external controller, such as an MC68HC05 family microcontroller, or MC68302 Integrated Multiprotocol Processor, to communicate with the MC145576. The SCP is a full duplex four-wire interface with control and status information passed to and from the MC145576. The serial control port consists of a transmit output (SCP_TX), a receive input (SCP_RX), a data clock (SCP_CLK), and two enable signals (SCP_EN-U and SCP_EN-T). The two separate enables allow simplified access to the U-Interface or the S/T-Interface portions of the MC145576 and they govern when this access occurs and with which part of the circuit, U-interface or S/T interface. The signal clock SCPCLK, determines the rate of exchange of data in both the transmit and receive directions. The four wire SCP interface is supplemented with one interrupt request line, SCP_IRQ, for external microcontroller notification of an event requiring service. The operation and configuration of the MC145576 is controlled by setting the state of its internal control registers and monitoring its status registers. A complete register map and detailed register descriptions are provided in **Section 5**.

## 6.2 Serial Control Port Mode

In SCP mode, access to the U and S/T registers is enabled separately by $\overline{\text{SCPEN-U}}$ for the U-interface and $\overline{\text{SCPEN-T}}$ for the S/T-interface. Data transfer uses the SCPCLK, SCPTX, and SCPRX signal lines. In general, each SCP operation begins with assertion of the appropriate enable signal. The first received bit is the Read/Write (R/$\overline{\text{W}}$) bit that determines whether the operation is a read (pulled high = 1) or a write (pulled low = 0). The next three bits in sequence define whether the selected register is a specific Nibble Register (U-NR0–5 or S/T-NR0–6), the U-Interface R6, or a byte register operation (the bits are all high = 111). Specific operations are defined in the following sections.
There are three types of SCP register access operations:

- Nibble Register (U-Interface and S/T-Interface)
- R6 Register (U-Interface only)
- Byte Register (U-Interface and S/T-Interface)

**NOTE:** The Overlay Registers replaced the Byte Registers and are accessed through the Byte Register locations when they are overlayed.

### 6.2.1 Nibble Register Operation

The 4-bit Nibble Registers are accessed via an 8-bit SCP interface operation, as shown in **Figure 6-1** (write) and **Figure 6-2** (read). The first bit on SCPRX after assertion of the enable signal is the Read/Write (R/$\overline{\text{W}}$) bit. This is followed by a 3-bit register field (A2–A0) that selects a specific Nibble Register or indicates a Byte Register operation. For a write operation, the 4-bit data word (D3–D0) follows. For a read operation, the 4-bit data word (D3–D0) follows on the SCPTX pin. **Table 6-1** and **Table 6-2** summarize Nibble Register operation bit values.

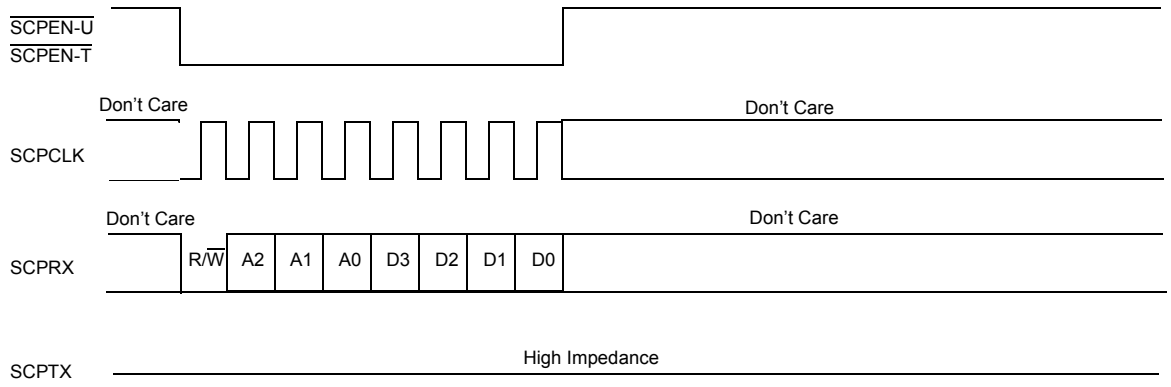



**Figure 6-1.** SCP U-NR0–5 or S/T-NR0–6—Write Operation

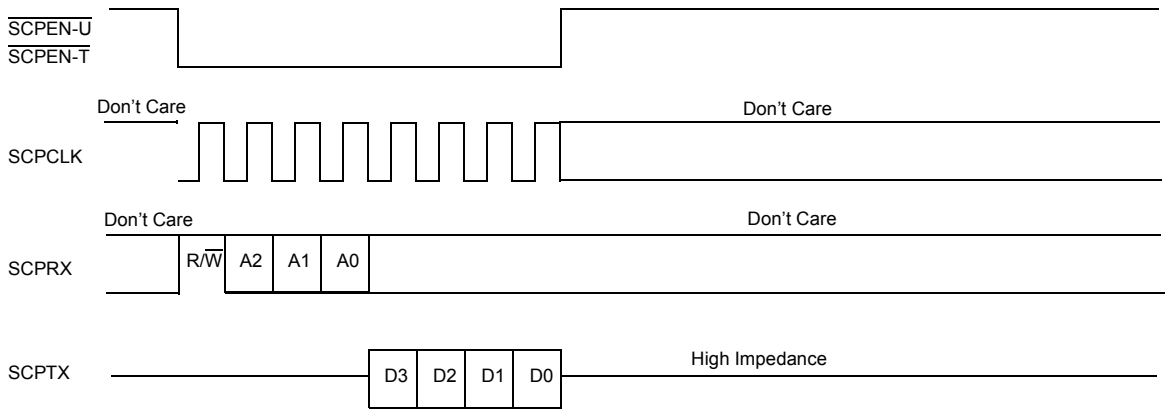



**Figure 6-2.** SCP U-NR0–5 or S/T-NR0–6—Read Operation

**Table 6-1.** U-Interface SCP Nibble Operations

| R/W | A2 | A1 | A0 | Data Bits | | | | Comment |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | d3 | d2 | d1 | d0 | U-NR0 Write |
| 0 | 0 | 0 | 1 | d3 | d2 | d1 | d0 | U-NR1 Write |
| 0 | 0 | 1 | 0 | d3 | d2 | d1 | d0 | U-NR2 Write |
| 0 | 0 | 1 | 1 | d3 | d2 | d1 | d0 | U-NR3 Write |
| 0 | 1 | 0 | 0 | d3 | d2 | d1 | d0 | U-NR4 Write |
| 0 | 1 | 0 | 1 | d3 | d2 | d1 | d0 | U-NR5 Write |
| 1 | 0 | 0 | 0 | x | x | x | x | U-NR0 Read |
| 1 | 0 | 0 | 1 | x | x | x | x | U-NR1 Read |
| 1 | 0 | 1 | 0 | x | x | x | x | U-NR2 Read |
| 1 | 0 | 1 | 1 | x | x | x | x | U-NR3 Read |
| 1 | 1 | 0 | 0 | x | x | x | x | U-NR4 Read |
| 1 | 1 | 0 | 1 | x | x | x | x | U-NR5 Read |

**Table 6-2.** S/T-Interface SCP Nibble Operations

| R/W | A2 | A1 | A0 | Data Bits | | | | Comment |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | d3 | d2 | d1 | d0 | S/T-NR0 Write |
| 0 | 0 | 0 | 1 | d3 | d2 | d1 | d0 | S/T-NR1 Write |
| 0 | 0 | 1 | 0 | d3 | d2 | d1 | d0 | S/T-NR2 Write |
| 0 | 0 | 1 | 1 | d3 | d2 | d1 | d0 | S/T-NR3 Write |
| 0 | 1 | 0 | 0 | d3 | d2 | d1 | d0 | S/T-NR4 Write |
| 0 | 1 | 0 | 1 | d3 | d2 | d1 | d0 | S/T-NR5 Write |
| 0 | 1 | 1 | 0 | d3 | d2 | d1 | d0 | S/T-NR6 Write |
| 1 | 0 | 0 | 0 | x | x | x | x | S/T-NR0 Read |
| 1 | 0 | 0 | 1 | x | x | x | x | S/T-NR1 Read |
| 1 | 0 | 1 | 0 | x | x | x | x | S/T-NR2 Read |

**Table 6-2.** S/T-Interface SCP Nibble Operations (Continued)

| R/W | A2 | A1 | A0 | Data Bits | | | | Comment |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | x | x | x | x | S/T-NR3 Read |
| 1 | 1 | 0 | 0 | x | x | x | x | S/T-NR4 Read |
| 1 | 1 | 0 | 1 | x | x | x | x | S/T-NR5 Read |
| 1 | 1 | 0 | 1 | x | x | x | x | S/T-NR6 Write |

## 6.2.2 R6 Register Operation

The 12-bit R6 register can be accessed with two sequential 8-bit SCP interface operations or a single 16-bit operation. In the first case, shown in **Figure 6-3** and **Figure 6-4**, the second 8-bit operation accesses the last 8 data bits (D7–D0) as shown. A single 16-bit operation is shown in **Figure 6-5** and **Figure 6-6**. See the R6 description in **Section 5.3.2** for correspondence between the ANSI defined *EOC* bits and the data bits transferred over the SCP interface. **Table 6-3** summarizes the R6 operation bit values.

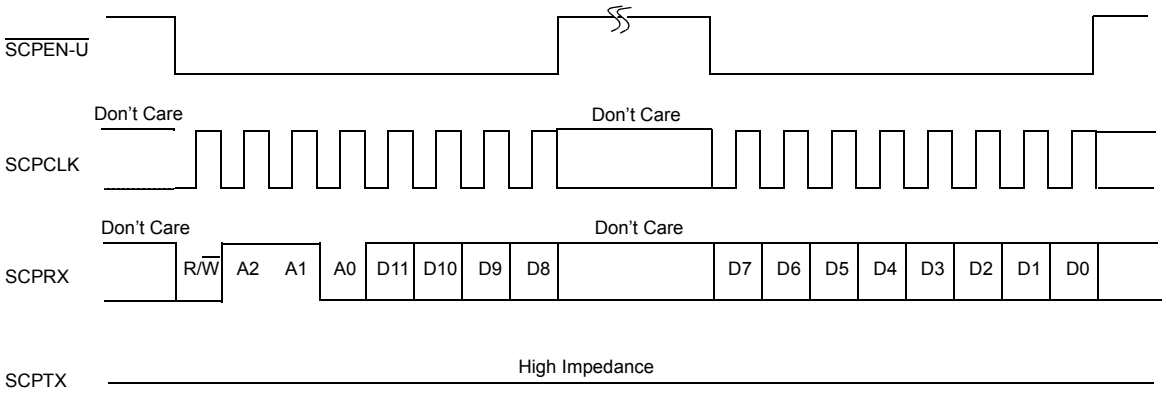



**Figure 6-3.** SCP EOC Register R6 Write Operation Using Double 8-Bit Transfer

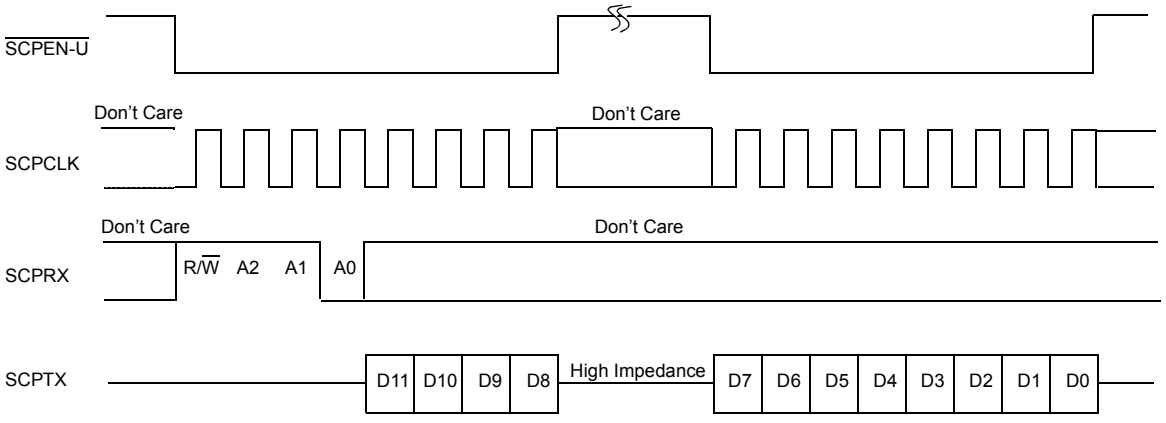



**Figure 6-4.** SCP EOC Register R6 Read Operation Using Double 8-Bit Transfer

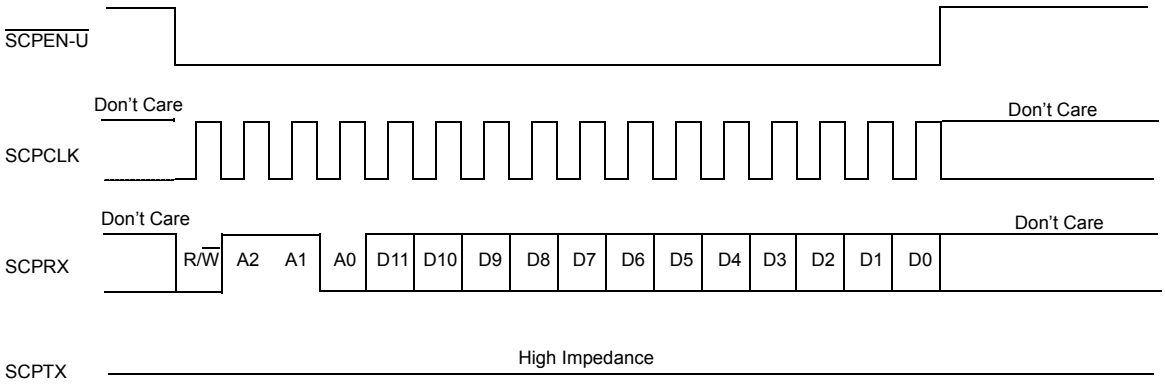



**Figure 6-5.** SCP EOC Register R6 Write Operation Using Single 16-Bit Transfer

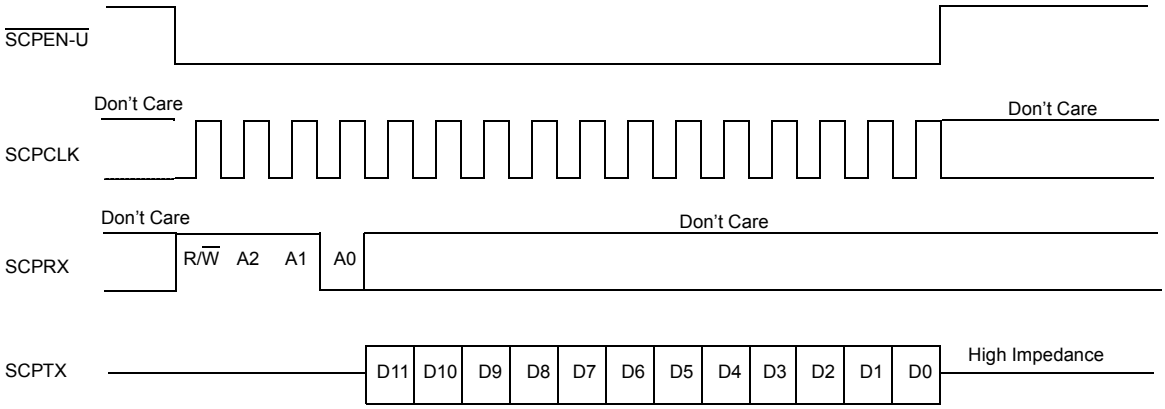



**Figure 6-6.** SCP EOC Register R6 Read Operation Using Single 16-Bit Transfer

**Table 6-3.** U-Interface SCP R6 Operations

| R/W | A2 | A1 | A0 | Data Bits | | | | | | | | | | | | Comment |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 0 | d11 | d10 | d9 | d8 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | U-R6 Write |
| 1 | 1 | 1 | 0 | x | x | x | x | x | x | x | x | x | x | x | x | U-R6 Read |

### 6.2.3 Byte Register Operation

After the appropriate SCPEN signal is asserted low (for U-Interface or S/T-Interface), if the SCPRX signal is held high for 3 clocks after the R/W bit, the chip begins a Byte Register operation. The next four bits select the specified Byte Register. As shown in **Figure 6-7** and **Figure 6-8**, this can be a 2-byte operation in which the second 8-bit operation transfers the data word (D7–D0). Alternately, a Byte Register can be accessed using a single 16-bit operation, as shown in **Figure 6-9** and **Figure 6-10**.

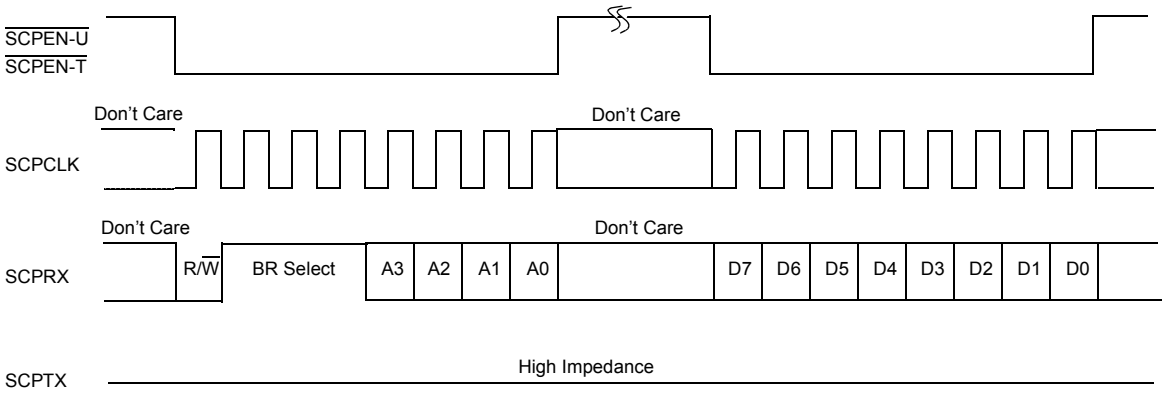



**Figure 6-7.** SCP Byte Register Write Operation Using Double 8-Bit Transfer

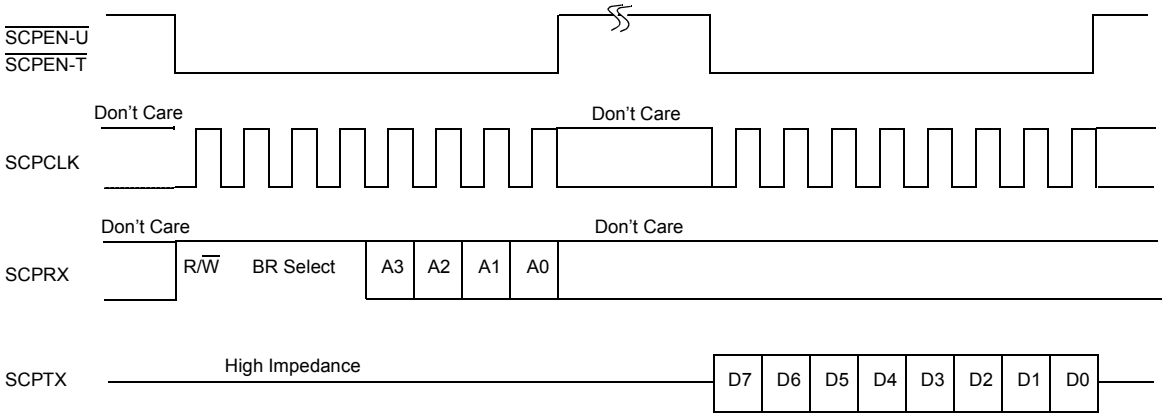



**Figure 6-8.** SCP Byte Register Read Operation Using Double 8-Bit Transfer

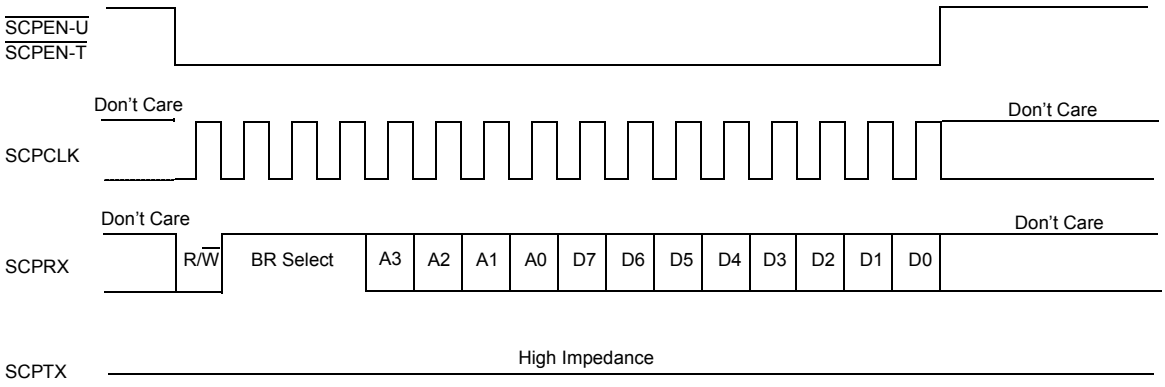



**Figure 6-9.** SCP Byte Register Write Operation Using Single 16-Bit Transfer

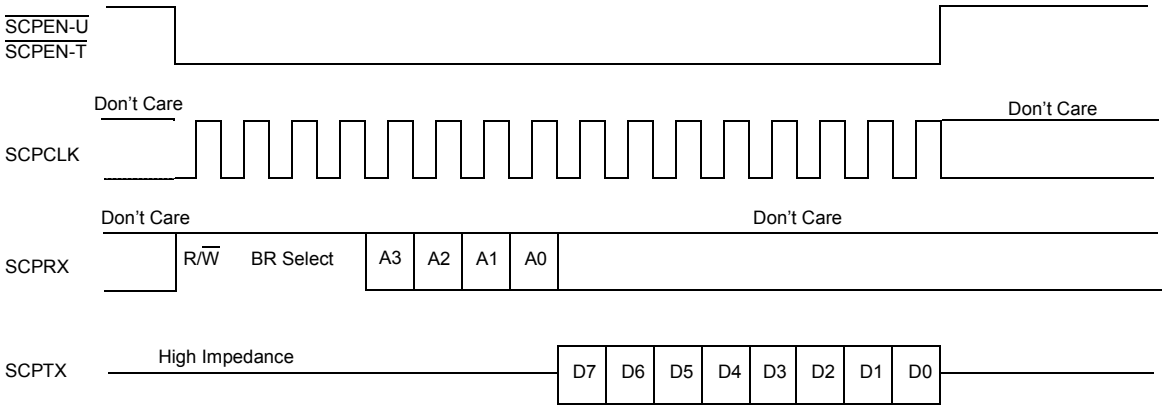



**Figure 6-10.** SCP Byte Register Read Operation Using Single 16-Bit Transfer

**Table 6-4.** SCP U-Interface Byte Operations

| BYTE 1 | | | | | | | | BYTE 2 | | | | | | | | Comment |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R/W | BR Select | | | A3 | A2 | A1 | A0 | Data | | | | | | | | |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | U-BR0 Write |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | U-BR1 Write |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | U-BR2 Write |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | U-BR3 Write |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | U-BR4 Write |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | U-BR5 Write |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | U-BR6 Write |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | U-BR7 Write |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | U-BR8 Write |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | U-BR9 Write |

**Table 6-4.** SCP U-Interface Byte Operations (Continued)

| BYTE 1 | | | | | | | | BYTE 2 | | | | | | | | Comment |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R/$\overline{W}$ | BR Select | | | A3 | A2 | A1 | A0 | Data | | | | | | | | |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | U-BR10 Write |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | U-BR11 Write |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | U-BR12 Write |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | U-BR13 Write |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | U-BR14 Write |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | U-BR15 Write |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | x | x | x | x | x | x | x | x | U-BR0 Read |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | x | x | x | x | x | x | x | x | U-BR1 Read |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | x | x | x | x | x | x | x | x | U-BR2 Read |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | x | x | x | x | x | x | x | x | U-BR3 Read |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | x | x | x | x | x | x | x | x | U-BR4 Read |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | x | x | x | x | x | x | x | x | U-BR5 Read |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | x | x | x | x | x | x | x | x | U-BR6 Read |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | x | x | x | x | x | x | x | x | U-BR7 Read |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | x | x | x | x | x | x | x | x | U-BR8 Read |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | x | x | x | x | x | x | x | x | U-BR9 Read |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | x | x | x | x | x | x | x | x | U-BR10 Read |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | x | x | x | x | x | x | x | x | U-BR11 Read |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | x | x | x | x | x | x | x | x | U-BR12 Read |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | x | x | x | x | x | x | x | x | U-BR13 Read |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | x | x | x | x | x | x | x | x | U-BR14 Read |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | x | x | x | x | x | x | x | x | U-BR15 Read |

**Table 6-5.** SCP S/T-Interface Byte Operations

| BYTE 1 | | | | | | | | BYTE 2 | | | | | | | | Comment |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R/$\overline{W}$ | BR Select | | | A3 | A2 | A1 | A0 | Data | | | | | | | | |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | S/T-BR0 Write |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | S/T-BR1 Write |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | S/T-BR2 Write |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | S/T-BR3 Write |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | S/T-BR4 Write |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | S/T-BR5 Write |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | S/T-BR6 Write |

**Table 6-5.** SCP S/T-Interface Byte Operations (Continued)

| BYTE 1 | | | | | | | | BYTE 2 | | | | | | | | Comment |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R/$\overline{W}$ | BR Select | | | A3 | A2 | A1 | A0 | Data | | | | | | | | |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | S/T-BR7 Write |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | S/T-BR8 Write |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | S/T-BR9 Write |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | S/T-BR10 Write |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | S/T-BR11 Write |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | S/T-BR12 Write |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | x | x | x | x | x | x | x | x | S/T-BR0 Read |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | x | x | x | x | x | x | x | x | S/T-BR1 Read |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | x | x | x | x | x | x | x | x | S/T-BR2 Read |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | x | x | x | x | x | x | x | x | S/T-BR3 Read |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | x | x | x | x | x | x | x | x | S/T-BR4 Read |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | x | x | x | x | x | x | x | x | S/T-BR5 Read |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | x | x | x | x | x | x | x | x | S/T-BR6 Read |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | x | x | x | x | x | x | x | x | S/T-BR7 Read |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | x | x | x | x | x | x | x | x | S/T-BR8 Read |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | x | x | x | x | x | x | x | x | S/T-BR9 Read |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | x | x | x | x | x | x | x | x | S/T-BR10 Read |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | x | x | x | x | x | x | x | x | S/T-BR11 Read |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | x | x | x | x | x | x | x | x | S/T-BR12 Read |

## 6.3 Signal Descriptions

There are six signals that constitute the SCP bus:

- SCP Tx
- SCP Rx
- SCPCLK
- $\overline{\text{SCPEN-U}}$
- $\overline{\text{SCPEN-T}}$
- $\overline{\text{IRQ}}$

A description of each signal follows.

### 6.3.1 SCP Tx

SCP Tx is used to output control, status, and data information from the MC145576 S/T-interface or U-interface, depending on which is enabled. The data is output in either 4-bit nibble (during a Nibble Register read) or 8-bit byte groupings (during a Byte Register read). Data is shifted out on SCP Tx on the falling edges of SCPCLK, Most Significant Bit first.

In a Nibble Register read transaction, the fourth rising edge of SCPCLK after the enable signal ($\overline{\text{SCPEN-U}}$ or $\overline{\text{SCPEN-T}}$) goes low shifts the Least Significant Bit of the 3-bit nibble address into the MC145576. The following falling edge of SCPCLK shifts out the Most Signifcant Bit of the selected Nibble Register and takes SCP Tx out of the high-impedance state. The next three falling edges of SCPCLK shift out the other three bits of the selected Nibble Register. When the Least Significant Bit has been shifted out, the enable signal ($\overline{\text{SCPEN-U}}$ or $\overline{\text{SCPEN-T}}$) should be returned high. This action returns SCP Tx to a high-impedance state.

In a Byte Register read transaction, the eighth rising edge of SCPCLK after the enable signal ($\overline{\text{SCPEN-U}}$ or $\overline{\text{SCPEN-T}}$) goes low shifts in the Least Significant Bit of the 4-bit byte address. The following falling edge of SCPCLK (provided $\overline{\text{SCPEN-U}}$ or $\overline{\text{SCPEN-T}}$ is still low) shifts out the Most Significant Bit of the selected Byte Register and takes SCP Tx out of high impedance. The next seven falling edges of SCPCLK shift out the remaining seven bits of the selected Byte Register. When the Least Significant Bit has been shifted out, the enable signal ($\overline{\text{SCPEN-U}}$ or $\overline{\text{SCPEN-T}}$) should be returned high. This action returns SCP Tx to a high-impedance state.

### 6.3.2 SCP Rx

SCP Rx is used to input control, status, and data information to the S/T-interface or U-interface, depending on which is enabled. Data is shifted into the device on rising edges of SCPCLK. The format for the input of data is as follows: the first bit is the R/W bit (1 = read, 0 = write). This bit selects the operation to be performed on the selected registers within the enabed interface. The next three bits address one of eight specific nibble registers within the enabled interface on which the read or write operation is to be performed. The address bits are shifted in Most Significant Bit first. The last four bits are either the data bits (Most Significant Bit first) written to the selected Nibble Register (NR0–NR6 for the S/T-interface or NR0–NR5 or R6 for the U-interface), or, are the four additional address bits used when addressing Byte Registers. These address bits select one of the sixteen byte-wide registers (which are accessed during the next eight cycles of the SCPCLK or a second 8-bit access). SCP Rx is ignored when data is being shifted out on SCP Tx, or when the enable signals $\overline{\text{SCPEN-U}}$ and $\overline{\text{SCPEN-T}}$ are high.

### 6.3.3 SCPCLK

This is an input to the device used for controlling the rate of transfer of data into and out of the SCP. Data is shifted into the part from SCP Rx on rising edges of SCPCLK. Data is shifted out of the part on SCP Tx on falling edges of SCPCLK. SCPCLK can be any frequency up to 4.096 MHz. An SCP transaction occurs when $\overline{\text{SCPEN-U}}$ or $\overline{\text{SCPEN-T}}$ is brought low.

**NOTE:** SCPCLK is ignored when $\overline{\text{SCPEN-U}}$ and $\overline{\text{SCPEN-T}}$ are both high.

### 6.3.4 $\overline{\text{SCPEN-U}}$

This signal, when held low, selects the SCP for the transfer of control, status, and data information into and out of the MC145576 U-interface. $\overline{\text{SCPEN-U}}$ should be held low for 8 or 16 periods of the SCPCLK signal, in order for information to be transferred into or out of the U-interface. The phase relationship of $\overline{\text{SCPEN-U}}$, with respect to SCPCLK, is as shown in **Figure 6-1** through **Figure 6-10** inclusive.

The transition of $\overline{\text{SCPEN-U}}$ going high aborts any SCP operation in progress, and forces the SCP Tx pin into the high-impedance state.

### 6.3.5 $\overline{\text{SCPEN-T}}$

This signal, when held low, selects the SCP for the transfer of control, status, and data information into and out of the MC145576 S/T-interface. $\overline{\text{SCPEN-T}}$ should be held low for 8 or 16 periods of the SCPCLK signal, in order for information to be transferred into or out of the S/T-interface. The phase relationship of $\overline{\text{SCPEN-T}}$, with respect to SCPCLK, is as shown in **Figure 6-1** through **Figure 6-10** inclusive.

The transition of $\overline{\text{SCPEN-T}}$ going high aborts any SCP operation in progress, and forces the SCP Tx pin into the high-impedance state.

### 6.3.6 $\overline{\text{IRQ}}$

$\overline{\text{IRQ}}$ is an open drain output to the device used for indicating that an interrupt condition exists. This pin is normally pulled high by an external resistor. When this pin goes low, it indicates a read operation of the interrupt status registers (U NR3 and S/T NR3) is required.

## 6.4 SCP Independence from Crystal

The MC145576 operates with a 20.48 MHz crystal frequency. Details of the crystal circuit can be found in **Appendix B**. The SCP operates independently of the 20.48 MHz crystal (i.e., the SCP can be accessed in the presence or absence of the 20.48 MHz input).

## 6.5 SCP Slave Mode

The SCP in the MC145576 always operates in SCP Slave Mode. The SCP Slave Mode is defined as having SCPCLK, $\overline{\text{SCPEN-U}}$, and $\overline{\text{SCPEN-T}}$ as inputs to the device. Thus, any device that communicates with the MC145576 via the SCP must be able to operate in SCP Master Mode in which SCPCLK, $\overline{\text{SCPEN-U}}$, and $\overline{\text{SCPEN-T}}$ are outputs.

# 7

# IDL Interface Mode Device Functionality

## 7.1 Introduction

The Interchip Digital Link (IDL) is a four-wire interface used for full-duplex communication on the board level between ICs. The interface consists of a transmit path (DOUT), a receive path (DIN), and associated clock (DCL), and a synchronizing (sync) signal (FSC). The clock determines the rate at which data is exchanged in both the transmit and receive directions. The sync signal controls when the exchange takes place. Three channels of date are exchanged every 8 KHz: two 64 Kbps B channels and one 16 Kbps D channel used for full duplex communication between the LT and the TE.

## 7.2 Signal Descriptions

As noted in the introduction, there are four signals (with corresponding IC pins) used by the IDL interface:

- **DOUT**—This is the serial data output signal. The data format is mode dependent.
- **DIN**—This is the serial data input signal. The data format is mode dependent.
- **DCL**—This is the bit clock output to the serial interface. The clock is continuous and the edges are synchronous to the frame sync signal. The clock rate can be selected (via the CLK_SEL pin) to be 2.048 MHz (CLK_SEL pulled high) or 512 KHz (CLK_SEL pulled low). The recovered timing is conveyed over DCL by adjusting the width of the clock. The adjustment is made by the internal PLL and occurs during two consecutive 8 KHz frames once per U-interface basic frame. The adjustment consists of adding or subtracting a single 20.48 MHz clock period during the high time of DCL. Since this occurs during two consecutive 8 KHz frames, the total adjustment is ± 97 ns once every basic frame.
- **FSC**—This output signal is used to synchronize all serial interface events. The signal is periodic at 8 KHz and is either phase locked to the signal received from the U frame when the U-interface is activated or from the crystal when the U-interface is deactivated. FSC is high for one cycle of the DCL clock with its rising edge aligned with the rising edge of the DCL clock.

**NOTE:** The IDL interface is always the master (i.e., the FSC and DCL signals are outputs from the device).

## CAUTION

For all IDL modes of operation described in **Section 7.3** through **Section 7.5**, the U Interface must be configured in Power Down Mode (i.e., U-NR0(b2) = 1) after the MC145576 is initialized. If SCP access to the U interface is required later when it is in Power Down Mode (i.e., U loop is not activated), it is necessary to wake up the interface (i.e., make U-NR0(b2) = 0). Then, when the interface is awake, all the U interface registers are accessible. After register operations are completed, put the interface back into Power Down Mode (i.e., make U-NR0(b2) = 1).

## 7.3 IDL Terminal Mode

In this mode the IDL Interface operates as a Terminal connection to the MC145576. The 2B+D data is passed transparently between the U-interface and S/T-interface portions of the MC145576 in both the upstream (towards the LT) and downstream (towards the TE). The IDL interface allows 2B+D data to be transmitted/received into/from this data flow connection:

- The 2B+D data that is output from the DOUT pin is simply the 2B+D data that is being sent downstream from the LT to the TE.
- The 2B+D data that is input to the DIN pin is combined with the 2B+D data that is being sent upstream from the TE to the LT.
- The combination of the two 2B+D data streams is achieved as follows (see **Figure 7-1**):
  - The B-channel data input on DIN is ANDed with the B-channel being passed upstream towards the LT. There is no circuitry in the MC145576 that detects if there is a data collision occurring, this the domain of the layer 2/3 software to ensure that a TE and the NT Terminal, do not attempt to access the same B-channel at the same time (passive bus configuration at S/T-Interface).
  - Likewise the D-channel data input on DIN is ANDed with the D-channel data being passed upstream, however, in this case there is a collision detection function that will ensure that the two D-channels will not collide and corrupt each others. This is accomplished by providing three pins that are used to monitor and enable the D-channel access by the Terminal Interface. These pins are DREQUEST, DGRANT and CLASS.

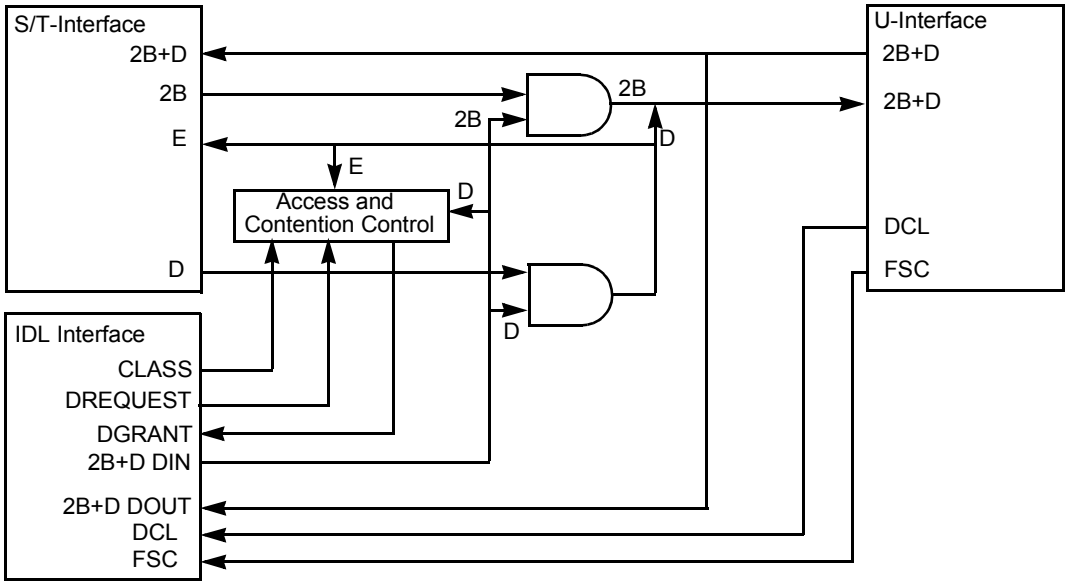



**Figure 7-1.** Conceptual Diagram of Terminal Data Flow

### 7.3.1 Accessing the Channels in Terminal Mode

This section describes the procedure for gaining access in Terminal Mode. When the terminal is inactive, the DREQUEST pin is held low. If the Terminal requires access to the D-channel, it must first pull the DREQUEST pin high. If another TE is already using the D-channel, the Terminal D-channel will be blocked. This is signified by the DGRANT output pin being held low. When the other TE completes its access, the DGRANT pin goes high, signalling to the Terminal that it can use the D-channel. D-channel data is then accepted on the DIN pin and passed upstream to the LT.

When the access is in progress, the data is continually monitored to ensure that a data collision with a TE does not occur. This is achieved by comparing the D-channel data input to the DIN pin with the ANDed combination of that data and the D-Channel being sent upstream from a TE. If they are not the same, then either the TE or the Terminal stops transmitting, but never both.

**NOTE:** The terminal that stops its transmission is the terminal with corrupted data.

This ANDed D-channel data is also sent downstream to the TEs on the E-Channel allowing them to be aware that another TE or terminal is using the D-Channel. The CLASS input is used to set the message priority. To terminate the D-channel access, the DREQUEST must be driven low.

This operation is in accordance with the method of TE D-channel access defined in the ETSI/ANSI specification (I.430) . The data input to the DIN D-channel pin must be in LAPD format to ensure the correct operation of the access/collision circuitry.

### 7.3.2 S/T-Interface and Terminal Mode

The D channel access mechanism (DGRANT and DREQUEST) is not available when the S/T-interface is in Absolute Min Power mode. Moreover, to transfer D data from the DIN pin to the U loop, the S/T-interface can not be in Sleep mode (to ensure this, set the Activation Request bit S/T-NR2(b3) to a 1 or set the Sleep Power Down Mode Disable bit S/T-NR6(b1) to a 1—see **Section 5.4.1.7** for additional information).

During communication on the D channel between the IDL bus and the LT, the S/T-interface should be in one of the following states:

- Transmit INFO2 (i.e., no TE connected)
- Fully activated (i.e., at least one TE is connected)
- Transmit INFO0 and out of Sleep mode (i.e., Idle during which no TE connection is allowed)

### 7.3.3 Terminal Mode IDL Interface Timing

When the MC145576 is configured in IDL mode (i.e., the IDL/GCI pin is pulled high), the default configuration after a hardware or software reset is NT Terminal 10-bit mode. In this mode, the IDL frame uses the format shown in **Figure 7-2**.

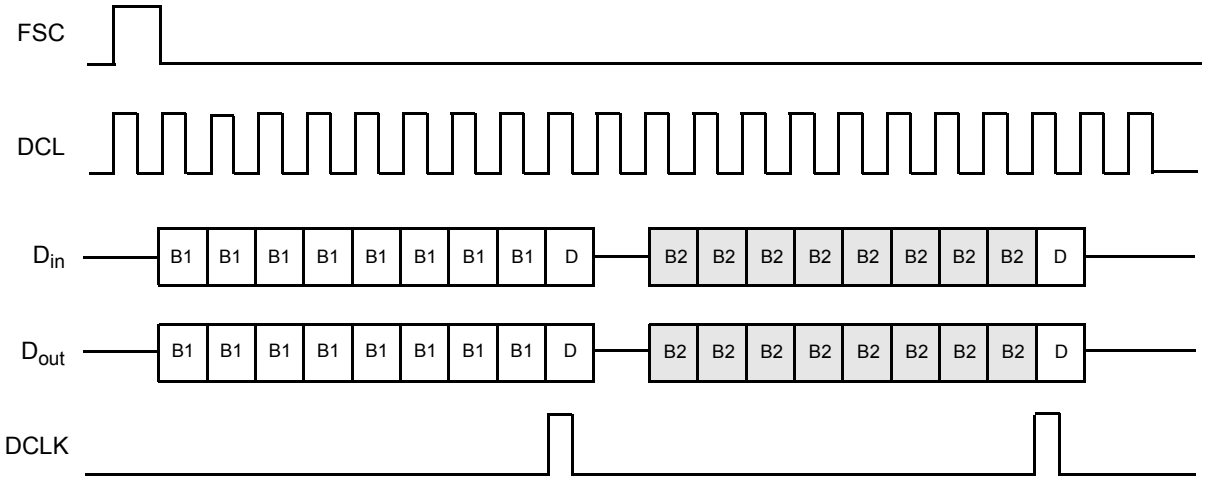



**Figure 7-2.** NT Terminal IDL 10-Bit Mode

When U-BR7(b0) is set to 1, the MC145576 is configured in NT Terminal 8-bit mode—see **Section 5.3.3.8**. In this mode, the IDL frame uses the format shown in **Figure 7-3**.

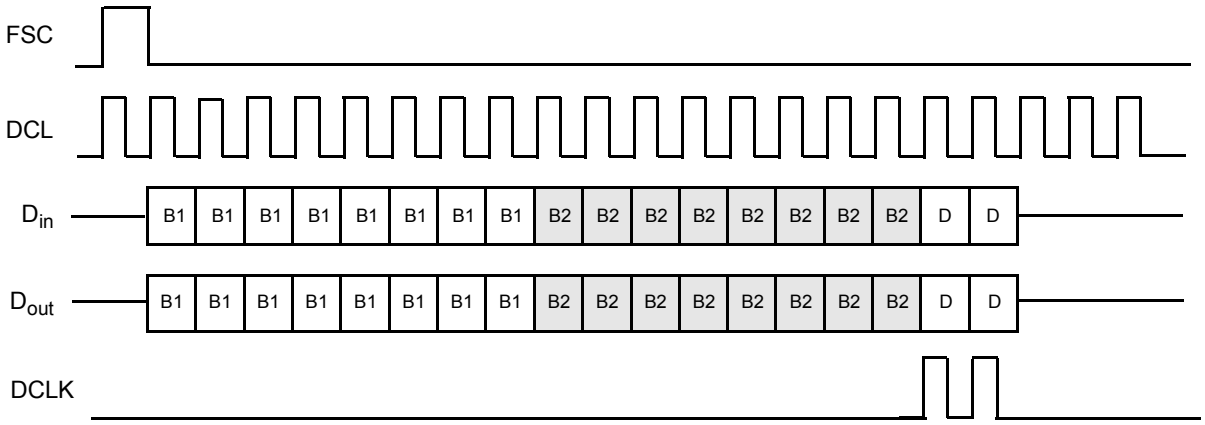



**Figure 7-3.** NT Terminal IDL 8-Bit Mode

By default, the B channels are disabled, both on DIN and DOUT. The can be enabled individually on both DIN and DOUT by writing to S/T-BR12(b3–b0)—see **Section 5.4.2.11** for more information. When the B1 or B2 channel is not enabled on DOUT, the pin outputs 1s during the appropriate timeslot, or is high impedance if S/T-OR6(b0) = 1. The D channel is always available on both DIN and DOUT.

## 7.4 TDM Mode

TDM mode has no direct 2B+D data connection between the U and S/T portions of the MC145576. Instead, the 2B+D data channels are directed to the IDL Interface. There is no Terminal interface DREQUEST, DGRANT, or CLASS signal and no D-channel contention in operation with the downstream TEs. When connected to a *Smart Terminal*, the interface allows very flexible control of the individual data channels, enabling complex control configurations. **Figure 7-4** shows a conceptual diagram of TDM data flow.

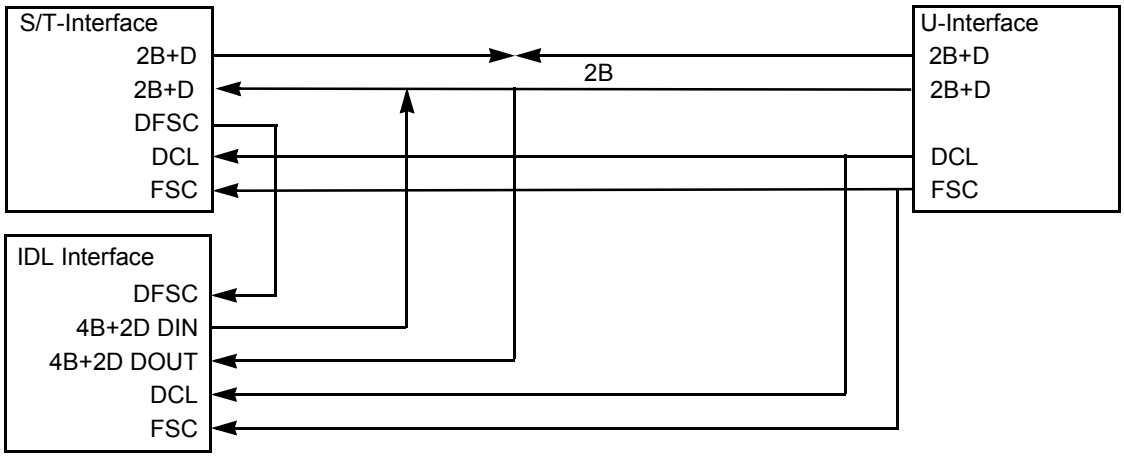



**Figure 7-4.** TDM Data Flow Conceptual Diagram

When the MC145576 is configured in the IDL mode (i.e., the IDL/GCI pin is pulled high) and ST-BR12(b7) is set to 1, the configuration is TDM 10-bit mode. In this mode, the IDL frame uses the format shown in **Figure 7-5**.

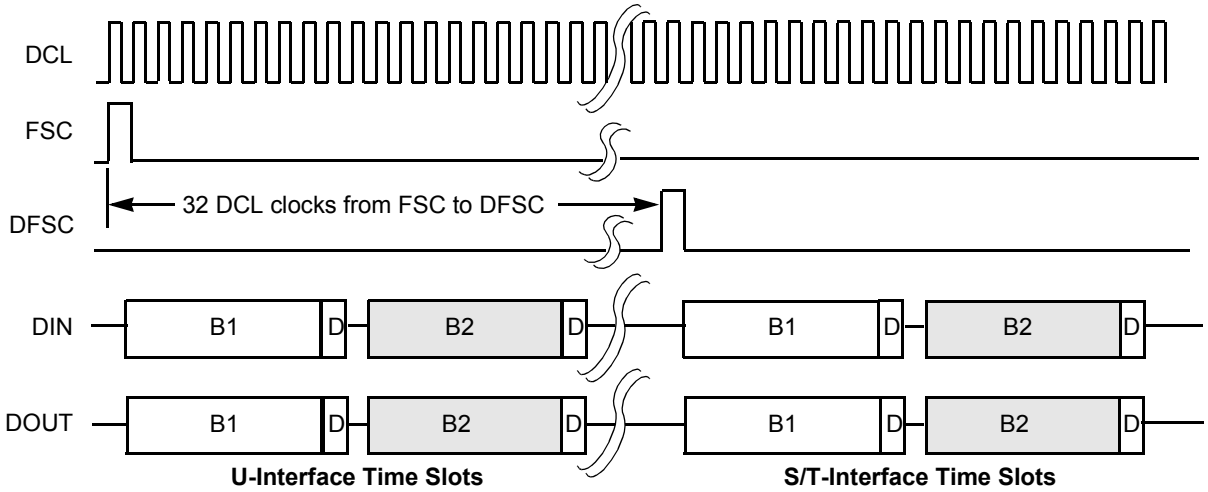



**Figure 7-5.** TDM IDL 10-Bit Mode

When U-BR7(b0) is set to 1 and S/T-BR12(b7) is set to 1, the MC145576 is configured in the TDM 8-bit mode. In this mode, the IDL frame uses the format shown in **Figure 7-6**.

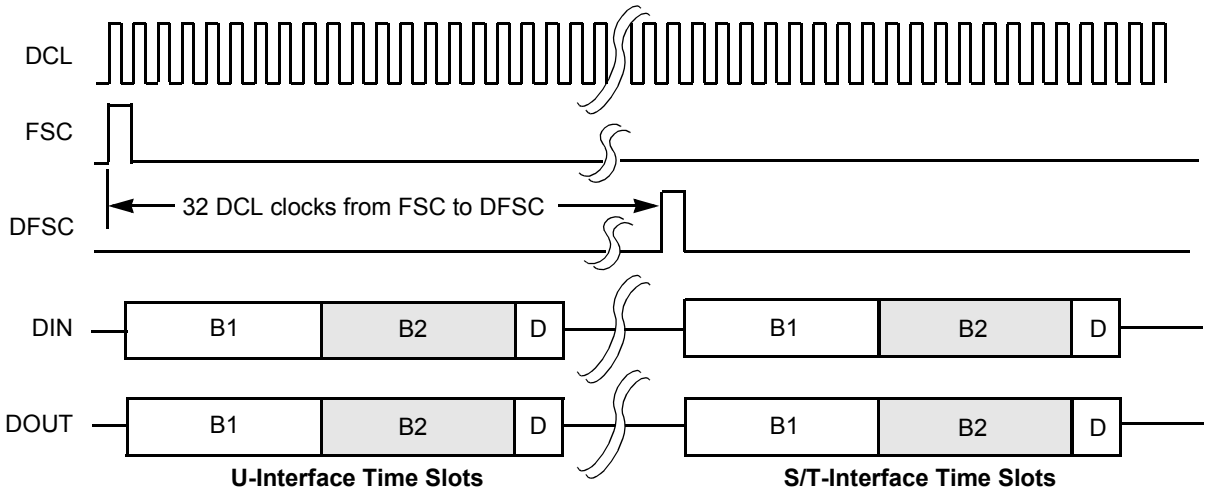



**Figure 7-6.** TDM IDL 8-Bit Mode

## 7.5 TSA Mode

In TSA mode, the full flexibility of the built-in Time Slot Assigners of the S/T and U Interfaces is available. In this mode, the individual data channels of the S/T interface can be enabled onto the IDL interface or be directed to take its data from the U-Interface. This mode is primarily intended for PABX applications where extremely flexible control of the data channels is required.

With a DCL rate of 2.048 MHz, it is possible to allocate to each B and D channel one of the 128 timeslot start times corresponding to each 2-bit boundary. With a DCL rate of 512 KHz, as many as 32 timeslots are available. Timeslot 0 start time corresponds to the falling edge of the FSC signal.

### CAUTION

To protect transmitted data, never program overlapping timeslots even if a timeslot is not enabled. The transmit and receive timeslot for a given B1, B2, or D channel can, however, be the same.

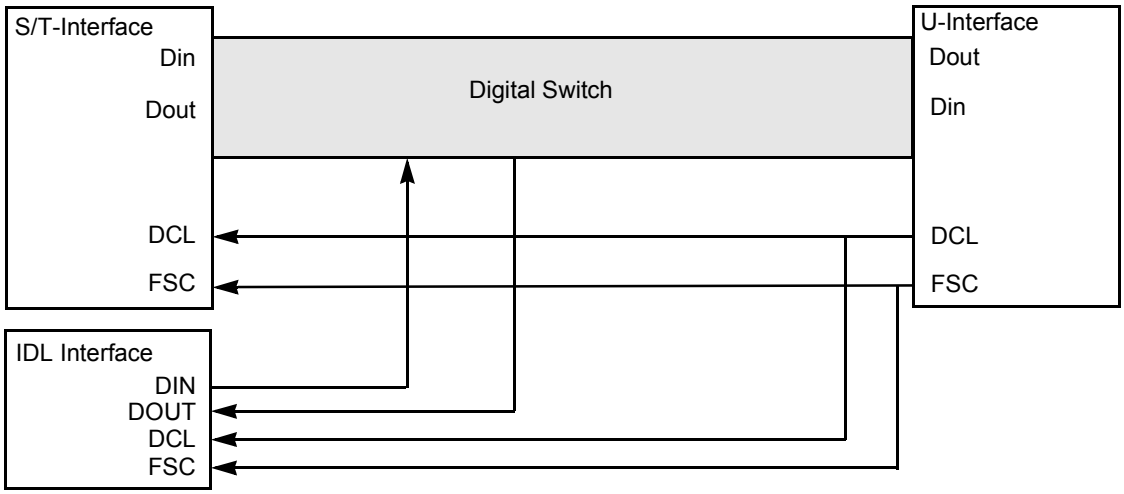



**Figure 7-7.** TSA Data Flow Conceptual Diagram

### 7.5.1 TSA Mode IDL Interface Timing and Programming

When the MC145576 is configured in IDL mode (i.e., the IDL/GCI pin is pulled high), S/T-BR12(b7) is set to 1, and S/T-OR(b4) is set to 1, the configuration is TSA mode. In this mode, the individual B and D channels for the transmit and received directions can be selected using OR0–5 of both the U and S/T registers. The data channels are enabled to the external IDL interface by setting the appropriate TSA enable bits in OR6 of both the U and S/T registers. Internal/External Data flow control is enabled for the individual data channels by OR7 of the S/T registers.

### 7.5.2 TSA Mode Example

Operation of this mode is best described by aid of an example. Consider a Smart NT-Mini-PABX system where the card contains four codecs, as shown in **Figure 7-8**.

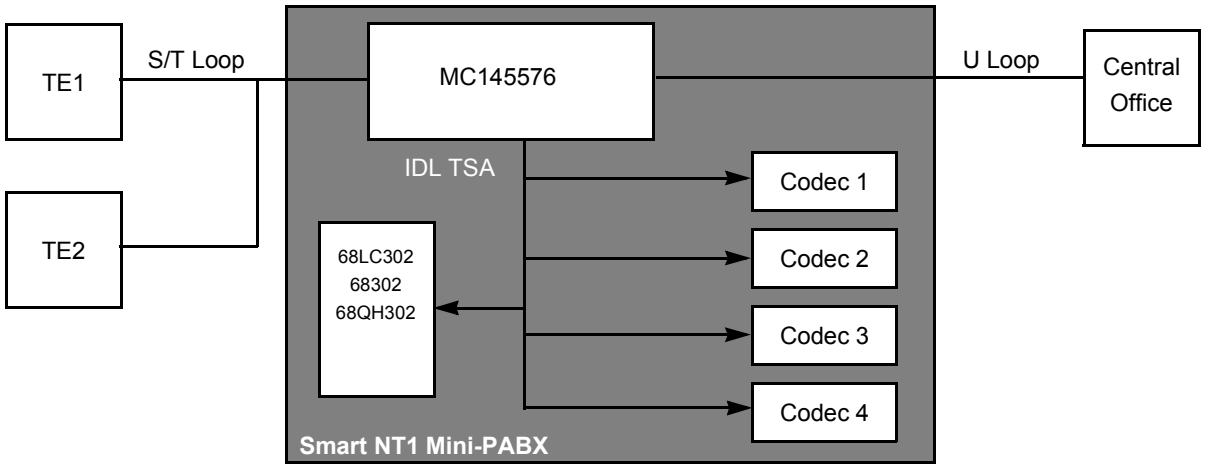



**Figure 7-8.** Mini-PABX Block Diagram

The codecs and the TEs are programmed for the timeslots shown in **Figure 7-9**.

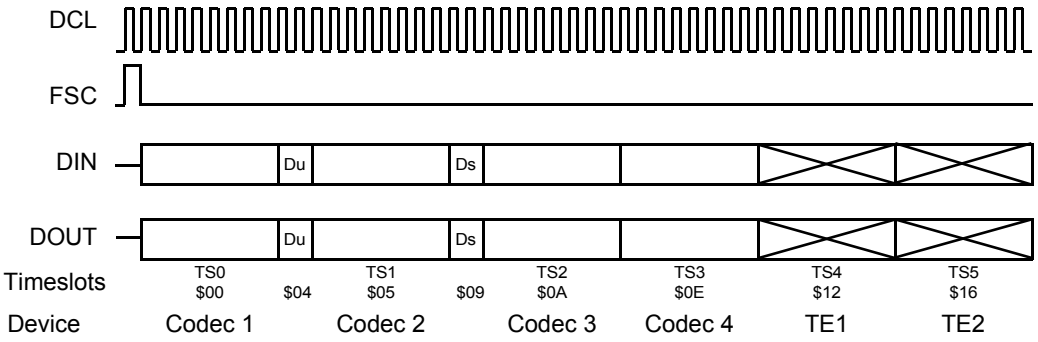



**Figure 7-9.** Timeslots Configuration

The D channels from the LT (Du) and from the TEs (Ds) are routed on the IDL bus to be processed by the microprocessor (one HDLC controller is required per D channel). To facilitate access to the D channels, the MC145576 provides two gated clocks: DCLK-T for the D channel coming from the TEs and DCLK-U for the D channel coming from the LT. The B channel interconnections between the codecs, the TEs, and the LT are controlled by the microprocessor through the Overlay Registers of both the U and S/T registers.

The following registers/bits remain unchanged regardless of the B channel interconnections:

- **U-Interface**—U-OR2 = $04; U-OR5 = $04; U-OR6(b5) = 1
- **S/T-Interface**—S/T-OR2 = $09; S/T-OR5 = $09; S/T-OR6(b5) = 1; S/T-OR6(b4) = 1

**Table 7-1** lists the registers/bits that change depending on the communications configuration.

**Table 7-1. Changed Registers/Bits in TSA Mode by Configuration**

| Configuration | U Registers | S/T Registers |
|---|---|---|
| TE1 to LT and TE2 to LT | OR6 = $E0; OR0 = OR3 = $12; OR1 = OR4 = $16 | OR6 = $F0; OR0 = OR3 = $12; OR1 = OR4 = $16; OR7 = $66 |
| Codec 1 to LT and Codec 2 to LT | OR6 = $E0; OR0 = OR3 = $00; OR1 = OR4 = $05 | OR6 = $30; OR0 = OR3 = $12; OR1 = OR4 = $16; OR7 = $00 |
| TE2 to LT and Codec 1 to LT | OR6 = $E0; OR0 = OR3 = $00; OR1 = OR4 = $16 | OR6 = $70; OR0 = OR3 = $12; OR1 = OR4 = $16; OR7 = $22 |
| TE1 to Codec 1 and TE2 to Codec 3[1] | OR6 = $20 | OR6 = $F0; OR0 = OR3 = $00; OR1 = OR4 = $0A; OR7 = $00 |
| Codec 2 to TE1, Codec 4 to TE2, Codec 1 to LT, and Codec 3 to LT | OR6 = $E0; OR0 = OR3 = $00; OR1 = OR4 = $0A | OR6 = $F0; OR0 = OR3 = $05; OR1 = OR4 = $0E; OR7 = $00 |
| TE1 to TE2[1] | OR6 = $20 | OR6 = $30; BR3 = $01; BR6 = $50 |
| Codec 1 to Codec 2[1] | OR6 = $20 | OR6 = $F0; BR6 = $05; OR0 = OR4 = $00; OR1 = OR3 = $05; OR7 = $00 |
| Codec 1 to Codec 2, Codec 3 to LT, and TE1 to LT | OR6 = $60; OR0 = $00; OR3 = $05; OR1 = OR4 = $0A | OR6 = $F0; BR6 = $05; OR0 = OR4 = $00; OR1 = OR3 = $05; OR7 = $44 |
| Codec 1 to Codec 2, Codec 3 to LT, and TE1 to TE2 | OR6 = $E0; OR0 = OR3 = $0E; OR1 = OR4 = $0A | OR6 = $F0; BR3 = $01; BR6 = $55; OR0 = OR4 = $00; OR1 = OR3 = $05; OR7 = $06[2] |

**Notes:** **1.** When only internal calls are required (i.e., codec to codec, TE to TE, or TE to codec), it is not necessary to activate the U line.

**2.** When both S/T B1/B2 loopback and IDL B1/B2 loopback are used (i.e., S/T-BR6 = $55), it is necessary to set S/T-OR7(b2, b1) bits to 1.

## 7.6 NT Transmit Signal/FSC Phase Relationship

The S/T-interface on the MC145576 behaves as an IDL slave with FSC and DCL provided by the U-interface. The S/T-interface uses FSC to position its outbound waveform correctly. Thus, FSC and the transmitted signal on the S/T loop INFO2 and INFO4 are synchronous. The phase relationship of these signals is shown in **Figure 7-10** with a enlarged inset.

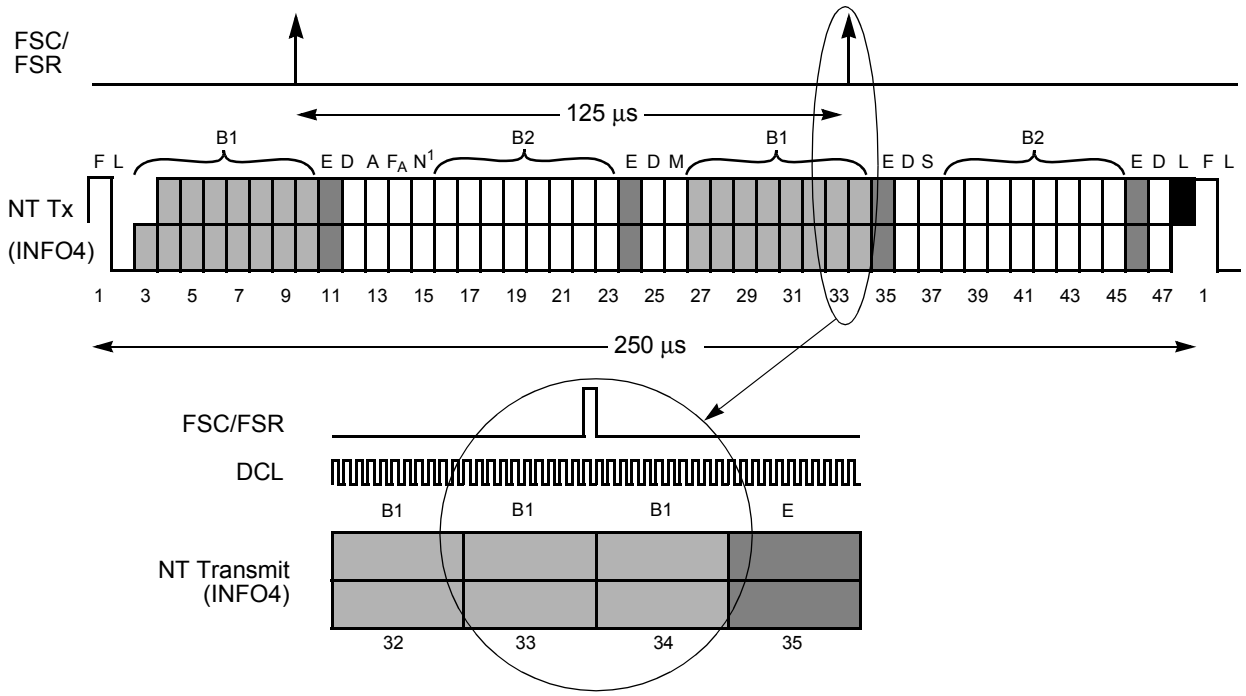



**Figure 7-10.** Phase Relationship of the NT Transmit Signal

# 8

# GCI Mode Device Functionality

## 8.1 Introduction

The General Circuit Interface (GCI) is a four-wire interface used for full-duplex communication between ICs at the board level. The interface consists of a transmit path (DOUT), a receive path (DIN), an associated clock (DCL), and a synchronizing (sync) signal (FSC). The clock determines the rate of exchange of data in both the transmit and receive directions, and the sync signal controls when this exchange is to take place. Three channels of data are exchanged every 8 KHz. These channels consist of two 64 kbps B channels and one 16 kbps D channel used for full duplex communication between the LT and TE. Two other channels are used to configure (Monitor channel) and control (C/I channel) the MC145576.

**NOTE:** The GCI is always master (i.e., the FSC and DCL signals are outputs).

## 8.2 Signal Descriptions

There are four signals (with corresponding IC pins) used by the GCI:

- **DOUT**—This is the serial data output for the GCI. This is an open drain output and must be pulled to $V_{DD}$ I/O through a resistor. The data format is mode dependent.
- **DIN**—This is the serial data input signal for the GCI. The data format is mode dependent.
- **DCL**—This is the double bit clock output to the serial interface (i.e., two clocks per data bit). The recovered timing is conveyed over DCL by adjusting the width of the clock. The adjustment is made by the internal PLL and occurs during two consecutive 8 KHz frames once per U-interface basic frame. The adjustment consists of adding or subtracting a single 20.48 MHz clock period during the high time of DCL. Since this occurs during two consecutive 8 KHz frames, the total adjustment is ± 97 ns once every basic frame.
- **FSC**—This output signal is used to synchronize all serial interface events. The signal is periodic at 8 KHz and is either phase locked to the signal received from the U frame when the U-interface is activated or from the crystal when the U-interface is deactivated. FSC is high for two cycles of the DCL clock with its rising edge aligned with the rising edge of the DCL clock.

## 8.3 GCI Frame Structure

The GCI interface supports two types of frame formats: the single GCI channel and the multiplexed GCI channel formats. A single GCI channel has the following subchannels: two B channels, Monitor channel, ISDN D channel, Command/Indicate channel, and A and E bits, as shown in **Figure 8-1**. This section discusses the single channel format. The multiplexed GCI channel operation is discusses in **Section 8.5**.

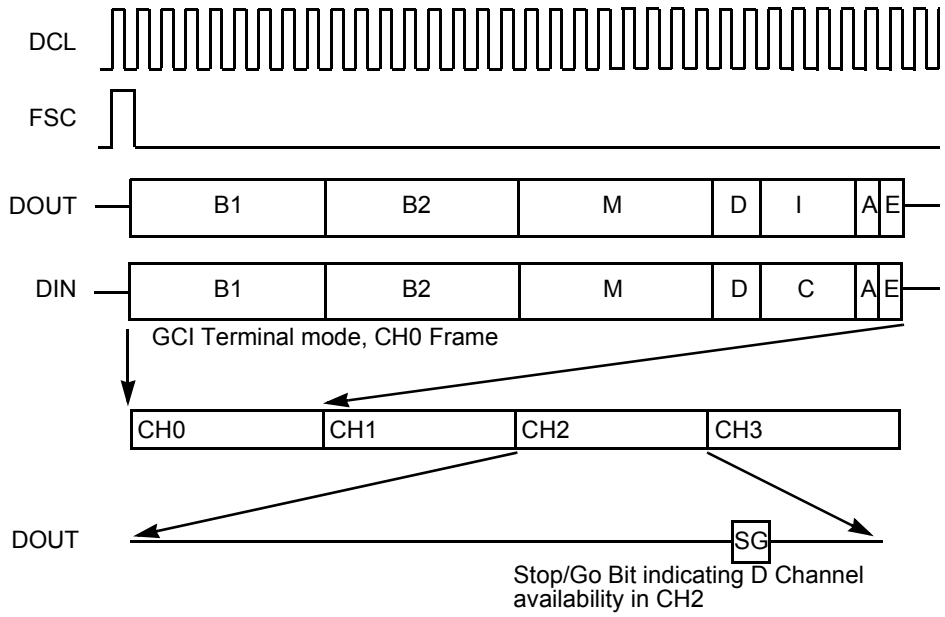



**Figure 8-1.** GCI Frame Structure

The two B channels are used to convey customer data between the MC145576 and other GCI devices. The Monitor channel bits are used to convey register and maintenance information between the MC145576 and other GCI devices. The D bits carry the ISDN basic access D channel. The Command/Indicate bits are used for activation and deactivation of the MC145576 and for control functions. The A and E bits are used as handshake signals during the transfer of monitor channel messages. A multiplexed GCI frame contains four GCI frames in each 125 µs period. **Table 8-1** summarizes the number of GCI frames that can be multiplexed into a 125 µs period.

**Table 8-1.** Multiplexed GCI Frame Configuration

| Clock | Maximum GCI Frames in Multiplex |
|---|---|
| 512 kHz | 1 |
| 2.048 MHz | 4 |

### 8.3.1 Monitor Channel Operation

The monitor channel has access to the entire internal register set of the MC145576. All monitor channel messages are two bytes in length. Each byte is sent twice to permit the receiving device to verify data integrity. The A and E bits in the GCI channel are used to control and acknowledge monitor channel transfers between the MC145576 and the terminal GCI device. When the monitor channel is inactive, the A, E, and M channels in the DOUT GCI frame are high impedance.

The A and E bits in the GCI channel are used to control and acknowledge Monitor. The A and E bits are active when they are driven to $V_{SS}$ during their respective bit times. Pull-up resistors are required on DIN and DOUT. The E bit indicates the transmission of a new Monitor channel byte. The A bit from the opposite direction is used to acknowledge the Monitor channel byte transfer. An idle Monitor channel is indicated by both A and E bits being inactive for two GCI frames. The A and E bits are high impedance when inactive. The Monitor channel data is $FF.

The originating GCI device transmits a byte onto the Monitor channel after receiving the A and E bits equal to 1 for at least two consecutive GCI frames. The originating GCI device also sets its outgoing E bit to 0 in the same GCI frame as the byte that is transmitted. The transmitted byte is repeated for at least two GCI frames, or is repeated in subsequent GCI frames, until the MC145576 acknowledges receiving two consecutive GCI frames containing the same byte. Once the MC145576 acknowledges the first byte, the sending device sets E to high impedance and transmits the first frame of the second byte. Then, the second byte is repeated with the E bit low until it is acknowledged. The destination GCI device verifies that it has received the first byte by setting the A bit to 0 towards the originating GCI device for at least two GCI frames. Successive bytes are acknowledged by the receiving device setting A to high impedance on the first instance of the next byte, followed by A being cleared to 0 when the second instance of the byte is received.

See **Figure 8-2** through **Figure 8-6** for details of Monitor channel operations.

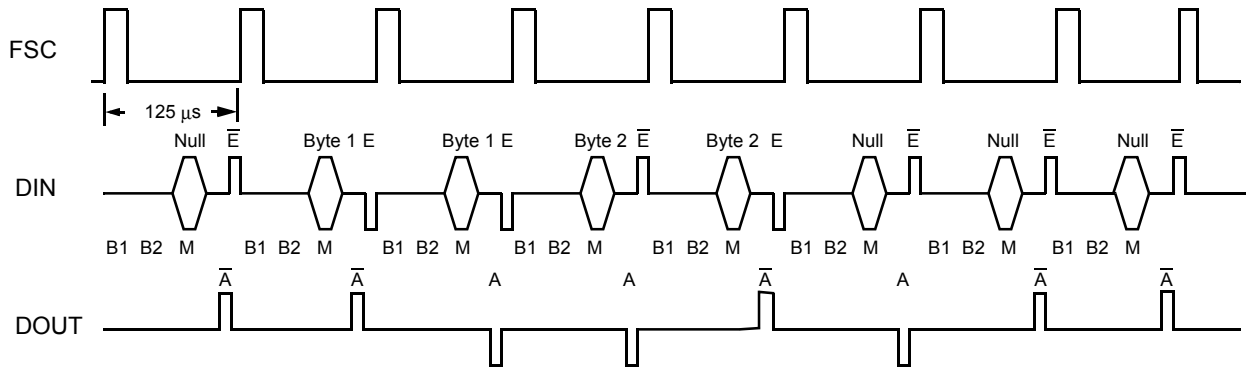



**Figure 8-2.** Monitor Channel Access Protocol

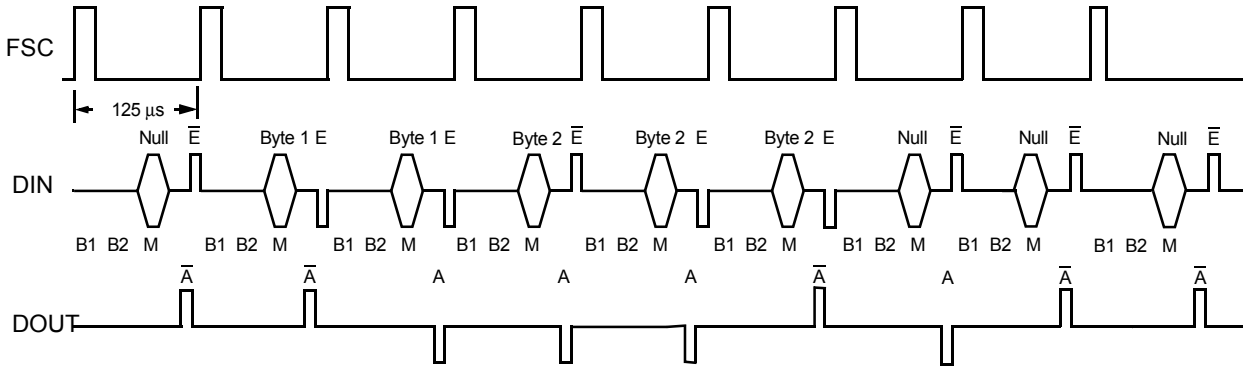



**Figure 8-3.** Monitor Channel Protocol with Delay

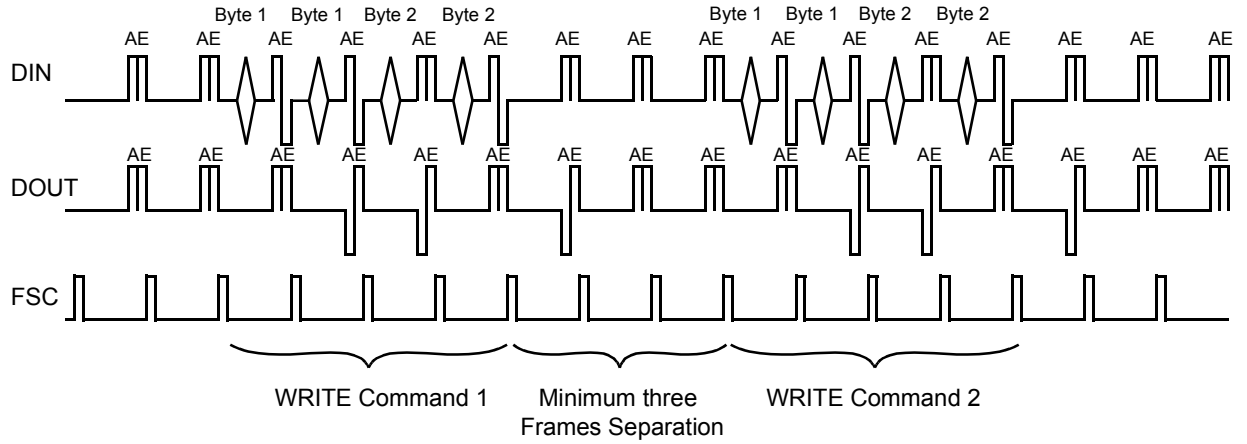



**Figure 8-4.** Monitor Channel Register Write Sequence

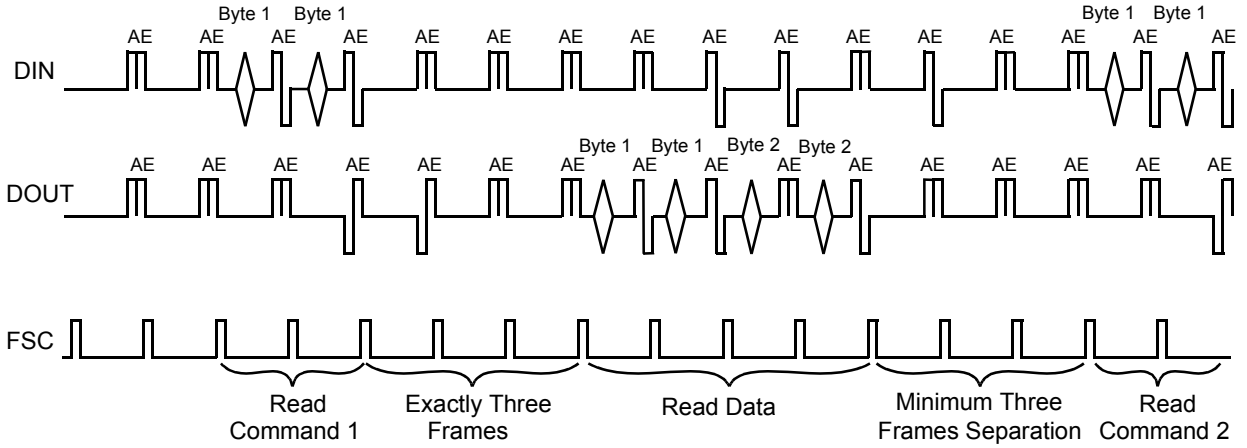



**Figure 8-5.** Monitor Channel Register Read Sequence

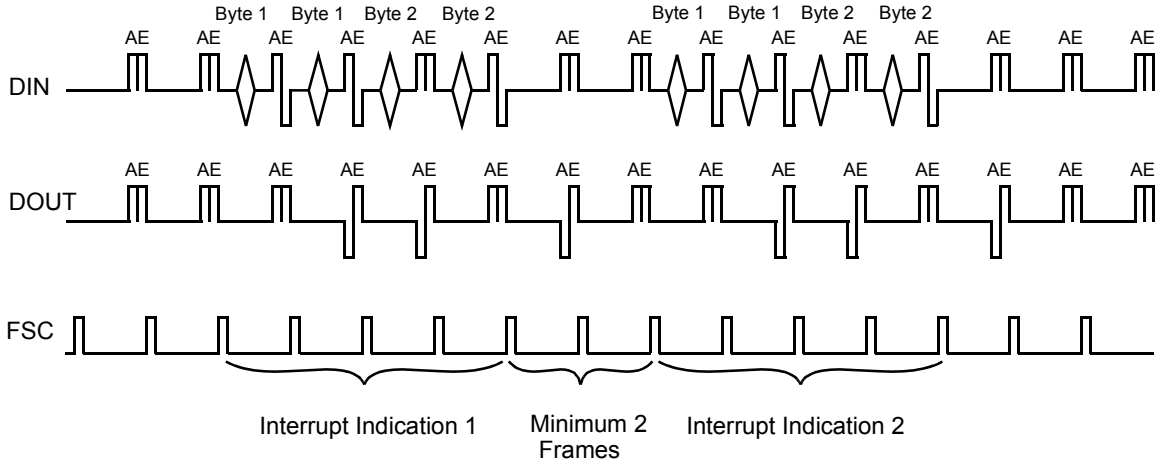



**Figure 8-6.** Monitor Channel Multiple Interrupt Indications Sequence

All M4 channel activity is automatically handled by the MC145576 when configured for GCI mode. The MC145576 issues Monitor channel messages whenever the received EOC, M4, or M5/M6 messages received from the U-interface change, and appropriate dual-checking or trinal-checking of bits has been done. In normal GCI operation, it is not necessary to read or write the internal registers of the MC145576.

If the receiving GCI device does not receive the same Monitor channel byte in two consecutive GCI frames, it indicates this by leaving A = 0 until two consecutive identical bytes are received. The last byte of the sequence is indicated by the originating GCI device setting its E bit to a 1 for two successive GCI frames. **Figure 8-3** shows an example of a delayed GCI Monitor channel message.

### 8.3.2 Monitor Channel Messages and Commands

The MC145576 supports three basic types of Monitor channel messages. The first group of messages are commands that read or write the internal register set of the MC145576. See **Section 5** for a complete description of the MC145576 register set. The second group of messages are responses that are transmitted by the MC145576 after it receives a register read or write command over the Monitor channel. The third group of Monitor channel messages are interrupt indication messages that are transmitted by the MC145576 whenever a change is detected in the Maintenance Channel Receive registers BR1, BR3, or R6 of the U-interface or in the interrupt register NR3 of the S/T-interface.

### 8.3.2.1 Monitor Channel Commands

A GCI device transmits Monitor channel commands to a receiving MC145576 to gain access to its internal register set. The receiving MC145576 then transmits a Monitor channel response message onto the Monitor channel for commands that request data to be read from an internal register. Commands that write data to an internal MC145576 register are accepted and acted upon, but the MC145576 does not issue a response message. Monitor channel commands are listed in **Table 8-2**.

**Table 8-2. Monitor Channel Commands**

| Byte 1 | | | | | | | | Byte 2 | | | | | | | | Command |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSB | | | | | | | LSB | MSB | | | | | | | LSB | |
| b17 | b16 | b15 | b14 | b13 | b12 | b11 | b10 | b27 | b26 | b25 | b24 | b23 | b22 | b21 | b20 | |
| 0 | 0 | 0 | 0 | ba3 | ba2 | ba1 | ba0 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | U-BR Write |
| 0 | 0 | 0 | 1 | ba3 | ba2 | ba1 | ba0 | | | | | | | | | U-BR Read |
| 0 | 0 | 1 | 0 | na3 | na2 | na1 | na0 | d3 | d2 | d1 | d0 | x | x | x | x | U-NR Write |
| 0 | 0 | 1 | 1 | na3 | na2 | na1 | na0 | | | | | | | | | U-NR Read |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | | | | | | | | | U-EOC Read |
| 0 | 1 | 1 | 0 | a1 | a2 | a3 | dm | i1 | i2 | i3 | i4 | i5 | i6 | i7 | i8 | U-EOC Write |
| 1 | 0 | 0 | 0 | ba3 | ba2 | ba1 | ba0 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | T-BR Write |
| 1 | 0 | 0 | 1 | ba3 | ba2 | ba1 | ba0 | | | | | | | | | T-BR Read |
| 1 | 0 | 1 | 0 | 0 | na2 | na1 | na0 | d3 | d2 | d1 | d0 | x | x | x | x | T-NR Write |
| 1 | 0 | 1 | 1 | 0 | na2 | na1 | na0 | | | | | | | | | T-NR Read |

**Notes:** 1. For BR accesses, the address range for ba3–ba0 is $0–$F. The bits d7–d0 are data written to the selected BR.
2. For NR accesses, the address range for na2–na0 is $0-$6. The bits d3–d0 are data written to the selected NR.\
3. The bits a1–a3, dm, and i1–i8 are data written to the EOC register (i.e., R6).
4. The MC145576 does not issue a response to a register write command

The MC145576 acknowledges all messages it receives over the Monitor channel. If an invalid message is received, the MC145576 acknowledges it, but does not take any action.

### 8.3.2.2 Monitor Channel Response Messages

The monitor channel response messages are transmitted onto the GCI monitor channel by the MC145576 in response to a register read command. The monitor channel response messages are given in **Table 8-3**.

**Table 8-3. Monitor Channel Response Messages**

| Byte 1 | | | | | | | | Byte 2 | | | | | | | | Comment |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSB | | | | | | | LSB | MSB | | | | | | | LSB | |
| b17 | b16 | b15 | b14 | b13 | b12 | b11 | b10 | b27 | b26 | b25 | b24 | b23 | b22 | b21 | b20 | |
| 0 | 0 | 0 | 1 | ba3 | ba2 | ba1 | ba0 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | U-Byte Read |
| 0 | 0 | 1 | 1 | 0 | na2 | na1 | na0 | d3 | d2 | d1 | d0 | X | X | X | X | U-Nibble Read |
| 0 | 1 | 0 | 1 | a1 | a2 | a3 | dm | i1 | i2 | i3 | i4 | i5 | i6 | i7 | i8 | U-EOC Read |
| 1 | 0 | 0 | 1 | ba3 | ba2 | ba1 | ba0 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | T-Byte Read |
| 1 | 0 | 1 | 1 | 0 | na2 | na1 | na0 | d3 | d2 | d1 | d0 | X | X | X | X | T-Nibble Read |

**Notes:** **1.** If monitor channel interrupt indication message is transmitted at the same time that a monitor channel read command is received then the indication message takes priority over the read request. All queued interrupt indication messages are issued before the response to the register read message. It is important for software to always check the message code in byte 1 of any received message.

**2.** The bits a1 through a3, dm and i1 through i8 are data that is read from the eoc register R6.

### 8.3.2.3 Monitor Channel Interrupt Indication Messages

The monitor channel interrupt indication messages are automatically transmitted onto the GCI monitor channel by the MC145576 when its receiver deframer updates one of the maintenance channel registers : there are BR1, BR3, EOC register R6 of the U-Interface and the interrupt register NR3 of the S/T-Interface is updated. All outstanding interrupt indication messages are transmitted prior to any response messages being transmitted. **Table 8-4** lists the monitor channel interrupt indication messages.

**Table 8-4. Monitor Channel Interrupt Indication Messages**

| Byte 1 | | | | | | | | Byte 2 | | | | | | | | Comment |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSB | | | | | | | LSB | MSB | | | | | | | LSB | |
| b17 | b16 | b15 | b14 | b13 | b12 | b11 | b10 | b27 | b26 | b25 | b24 | b23 | b22 | b21 | b20 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | M50 | M60 | M51 | Rxd FEBE | C'd FEBE | Ve'd ACT | Ve'd DEA | S Fr Det | M5/M6 INT |
| 0 | 0 | 1 | 0 | S/T IRQ3 | S/T IRQ2 | S/T IRQ1 | S/T IRQ0 | M40 | M41 | M42 | M43 | M44 | M45 | M46 | M47 | M4/T INT |
| 0 | 1 | 0 | 1 | a1 | a2 | a3 | DM | i1 | i2 | i3 | i4 | i5 | i6 | i7 | i8 | EOC INT |

**Notes:** **1.** The bits a1 through a3, dm and i1 through i8 are data that is read from the EOC register R6.

**2.** The data byte returned by the M5/M6 interrupt corresponds to the byte as read from the Byte register BR3 in the U SCP Interface register map.

**3.** The data byte returned by the M4/T interrupt corresponds to the byte as read from Byte register BR1 in the U SCP interface register map and the Nibble Register NR3 in the S/T SCP interface register map.

**4.** The S/T interrupts must first be enabled by writing to NR4 in the S/T Interface register map, before the interrupt indication message is generated by the NT1. The M5/M6, M4 and eoc interrupt messages are enabled by default.

## 8.4 Terminal Mode

The GCI mode of the MC145576 provides a fully operational GCI. The Interface operates as a master (i.e., the MC145576 is the source of the FSC and DCL), which is synchronized to the receive frames of the U-Interface. In this mode the GCI operates as a Terminal connection to the MC145576 where 2B+D data is passed transparently between the U-Interface and S/T-Interface portions of the MC145576 in both the upstream (towards the LT) and downstream (towards the TE). The GCI in this mode allows 2B+D data to be transmitted/received into/from this data flow connection.

The DCL clock frequency is 2.048 MHz thus providing a four-channel GCI frame. The MC145576 only operates in CH0 for B, D, C/I, and monitor channels and in bit 5 of the C/I channel in CH2 (SCIT Terminal mode) which is used to indicate the status of the Terminal D channel availability (stop/go status). The 2B+D data that is output from the DOUT pin is simply the 2B+D data that is being sent downstream from the LT to the TE. The 2B+D data that is input to the DIN pin is combined with the 2B+D data that is being sent upstream from the TE to the LT. The combination of the two 2B+D data streams is achieved as described in the next sections.

### 8.4.1 B Channels

The B channel data input on DIN is ANDed with the B channel being passed upstream towards the LT. There is no circuitry in the MC145576 that detects if there is a data collision occurring, this the domain of the layer 2/3 software to ensure that a TE and the NT Terminal, do not attempt to access the same B channel at the same time (passive bus configuration at S/T-Interface). It is possible to block the B channels independently from any interface (i.e., U, S/T, or GCI via monitor channel control).

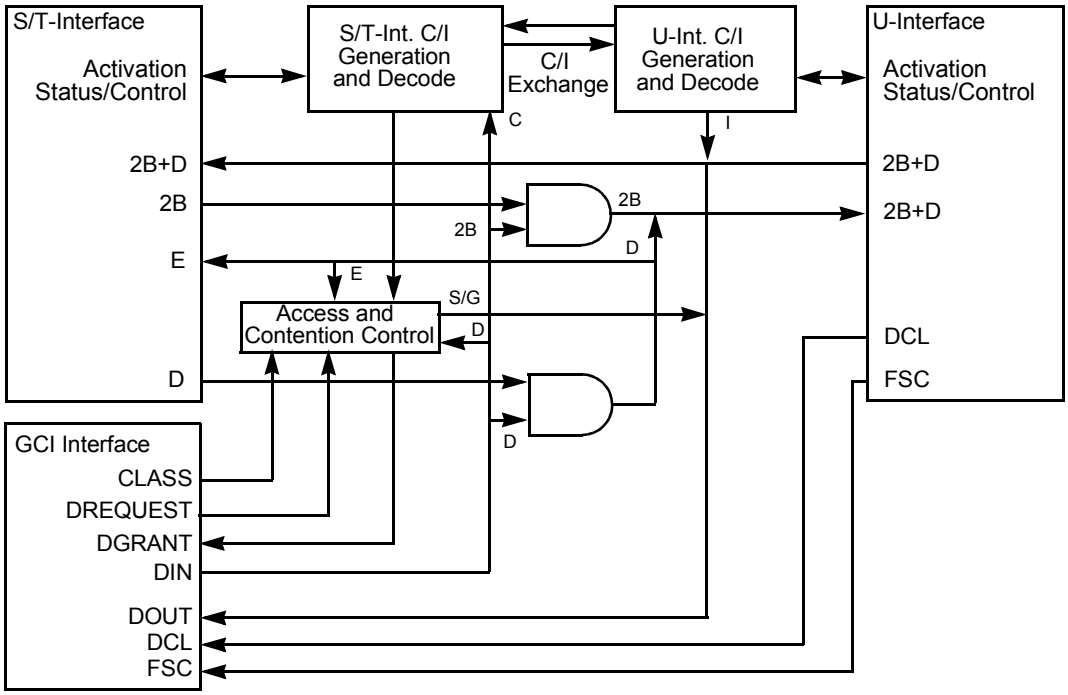
### 8.4.2 D Channel

The D channel data input on DIN is ANDed with the D channel data being passed upstream, however, in this case the collision detection function ensures that the two D channels do not collide and corrupt each others data. Before the D channel is available for use, the NT1 terminal must request access by using a C/I channel command, AI8 or AI10, or by using the DREQUEST input pin. The D channel access circuitry then checks whether the D channel is currently being used by a downstream TE. If so, then terminal access to the D channel is blocked. If the D channel becomes available, (i.e., no TE is transmitting data on the D channel), then access is granted, as indicated by the Stop/Go indication bit, Bit 5 of the C/I Channel in CH2 of the output GCI frame on DOUT, and the DGRANT output pin.

The collision detection circuitry detects when a data collision between the NT1 terminal and a downstream TE occurs. If there is a data collision, then the terminal (NT1 or TE) whose data is corrupted stops transmitting. This ANDed D channel data is also sent downstream to the TEs on the E-Channel in the transmitted S/T-Interface frames allowing them to be aware that another TE or terminal is using the D channel. The CLASS input pin or the C/I commands , AI8/10, can be used to set the message priority. To terminate the D channel access the C/I command AIEOM or DREQUEST should be

used. In the case of DREQUEST it must be taken low.

Control of the D channel is accomplished either by the C/I channel or the DREQUEST/DGRANT/CLASS pins but not a mixture of both. If the C/I channel is controlling D channel access, then hold the CLASS and DREQUEST pins low. Likewise, if the DREQUEST/DGRANT/CLASS pins are used, then use the AIEOM C/I command to control AI8/10. This operation is in accordance with the method of TE D channel access defined in the ETSI/ANSI specification (I.430). The DIN D channel input data must be in LAPD format to ensure the correct operation of the access/collision circuitry.




**Note:** For clarity, the monitor is not shown.

**Figure 8-7.** GCI Data Flow Conceptual Diagram

### 8.4.3 C/I Channel

The C/I channel is used to allow activation of the MC145576 by the NT terminal. The C/I channel is always directed towards the upstream direction. The C/I command input to DIN is combined with the activation status of the S/T-Interface before being passed in the upstream direction to the U-Interface. **Table 8-5** defines the C/I channel command and indication codes available for the GCI terminal mode.

**Table 8-5. GCI Terminal Mode C/I Channel Command and Indication Codes**

| C/I CODE | COMMAND | INDICATION |
|---|---|---|
| 0000 | TIM | DR |
| 0001 | – | – |
| 0010 | – | – |
| 0011 | – | – |
| 0100 | – | RSY |
| 0101 | – | EI2 |
| 0110 | – | – |
| 0111 | – | – |
| 1000 | AR8 | AR |
| 1001 | AR10 | – |
| 1010 | – | ARL |
| 1011 | AIEOM | – |
| 1100 | AI8 | AI |
| 1101 | AI10 | – |
| 1110 | – | AIL |
| 1111 | DI | DC |

**Notes:**
1. TIM = Timing Request for the GCI
2. DR = Deactivation Request from U-Interface
3. RSY = Loss of Sync at U-Interface
4. EI2 = Error Indication at U-Interface
5. AR = Activation Request Indication from U-Interface, Activation request command to MC145576
6. ARL = Indication from NT1 that 2B+D loopback at S/T Interface towards the upstream direction has been activated by LT
7. AIEOM = Activation indication to U-Interface with End Of Message Tag to close the D channel access
8. AI8/10 = Activation indication Command with D channel access command to MC145576 with message class of 8 or 10
9. AI = Activation Indication from U-Interface
10. AIL = Indication from NT1 that 2B+D loopback at S/T Interface towards the upstream direction has been activated by LT
11. DI = Deactivation Indication Command to the MC145576
12. DC = Deactivation confirmation Indication from U-Interface

The Indication code generated on DOUT is the command being passed downstream from the U-Interface to the S/T-Interface. It provides the current status of the MC145576 to the NT terminal. If more precise status information is required, then the NT terminal can access the appropriate activation and maintenance registers of the U and S/T portions of the MC145576.

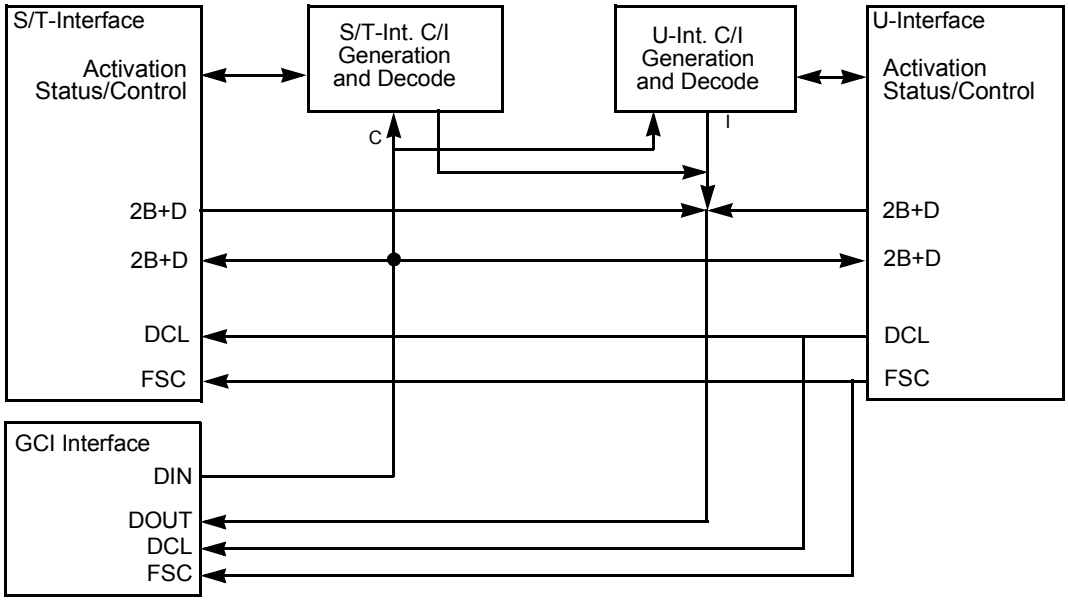
The Command code input to the MC145576 on DIN is combined with the current status of the S/T-Interface before being passed to the U-Interface, thus ensuring that:

- the interface is activated correctly,
- access to the D channel is enabled, and
- the message class is controlled.

## 8.5 Multiplex Mode

**NOTE:** In multiplex mode, only select the clock rate DCL = 2.048 MHz (i.e., pin CLK_SEL = 1).

The Multiplex mode for the GCI operates in a fashion similar to the IDL TDM mode. In this mode, there is no direct 2B+D data connection between the U and S/T portions of the MC145576. Instead the 2B+D data channels are directed to the GCI. Likewise the C/I channels for the individual U and S/T portions are directed towards the GCI. The U-Interface occupies the CH0 channel and the S/T-Interface occupies the CH1 channel. There is no Terminal interface DREQUEST/DGRANT/CLASS and no D channel contention/access in operation with the downstream TEs. The interface allows very flexible control of the individual data channels enabling complex control configurations when connected to a Smart Terminal. One possible example is creating a small, low cost PABX. The CH0 channel also contains the monitor channel used to access the registers of both the U and the S/T interfaces. There is no monitor channel available in CH1. **Figure 8-8** and **Figure 8-9** illustrate the multiplex configuration.




**Note:** For clarity, the monitor is not shown.

**Figure 8-8.** GCI Data Flow Conceptual Diagram

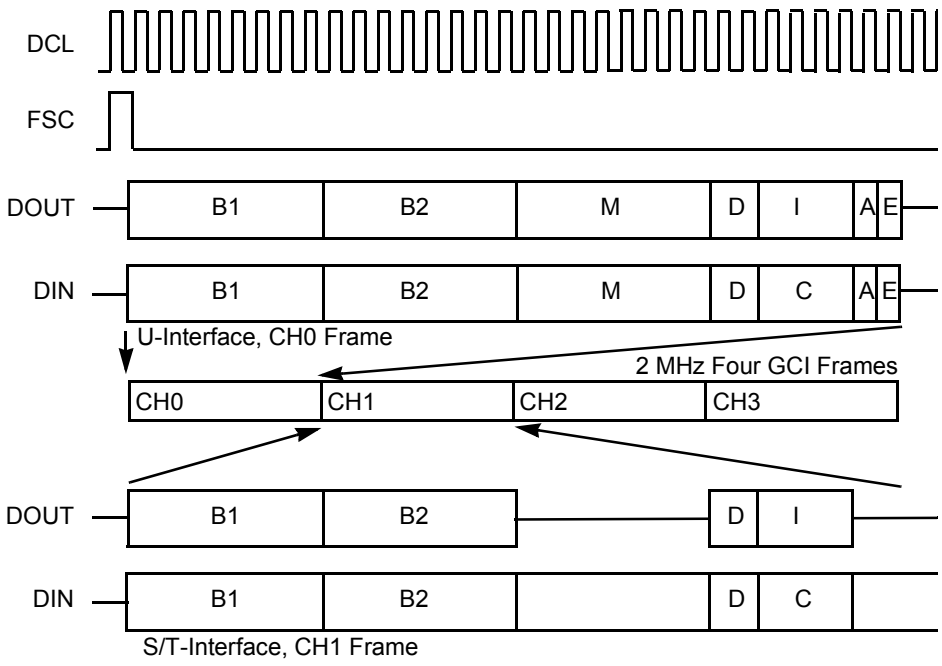



**Figure 8-9.** Multiplex GCI Timing

**Table 8-6** defines the C/I channel command and indication codes available for the GCI Multiplex Mode. As can be seen separate control of the U and S/T Interfaces is accomplished through the use of the C/I channels in CH0 and CH1.

**Table 8-6. Multiplex Mode C/I Channel Code Definitions**

| C/I CODE | Indication CH0 U-Interface | Command CH0 U-Interface | Indication CH1 S/T-Interface | Command CH1 S/T-Interface |
|---|---|---|---|---|
| 0000 | DR | TIM | – | DR |
| 0001 | – | RES | – | RES |
| 0010 | – | – | – | – |
| 0011 | – | – | – | – |
| 0100 | RSY | – | RSY | – |
| 0101 | EI2 | – | – | – |
| 0110 | – | – | – | T1/T3EXP |
| 0111 | – | – | – | – |
| 1000 | AR | AR | AR | AR |
| 1001 | – | – | – | – |
| 1010 | ARL | – | – | ARL |
| 1011 | – | – | – | – |
| 1100 | AI | AI | AI | AI |
| 1101 | – | – | – | – |
| 1110 | AIL | – | – | AIL |
| 1111 | DC | DI | DI | DC |

# 9

# Activation and Deactivation

## 9.1 Introduction

This section describes the activation and deactivation procedures for the MC145576 in IDL/SCP mode and GCI mode.

## 9.2 IDL/SCP Mode

The following sections describe U-interface operations and S/T-interface operations when the MC145576 is in IDL/SCP mode.

### 9.2.1 U-Interface Operations

This section assumes that that MC145576 is configured for the IDL mode of operation. U-interface activation or start-up is the process by which the U-interface initiates a robust full-duplex communications channel. This process is a well-defined sequence of procedures during which the training of the equalizers and echo cancellers at each end of the transmission line takes place. Two types of activation, cold start or warm start, may occur. The MC145576 is capable of supporting both types automatically. Deactivation is the process used to gracefully end communication between the U-interface transceivers at each end of the transmission line. Only a U-interface transceiver in LT mode may initiate a deactivation procedure.

ANSI T1.601-1992 defines ten activation signals, described in **Table 9-1** and **Table 9-2** for the U-interface transceivers to use during the activation procedure. For instance, six basic frames of signal TN are transmitted by the NT when it wants to wake up the LT or in response to the LT transmitting TL. Two basic frames of signal TL are transmitted by the LT when it wants to wake up the NT. When the NT is in the fully operational mode, it transmits the signal known as SN3 and receives SL3 from the LT end. Conversely, when the LT is in fully operational mode, it transmits SL3 and receives SN3. Only when the U-interface is fully activated, with the NT transmitting signal SN3 and the LT transmitting SL3, are the 2B+D channels of data capable of being transmitted over the U-interface.

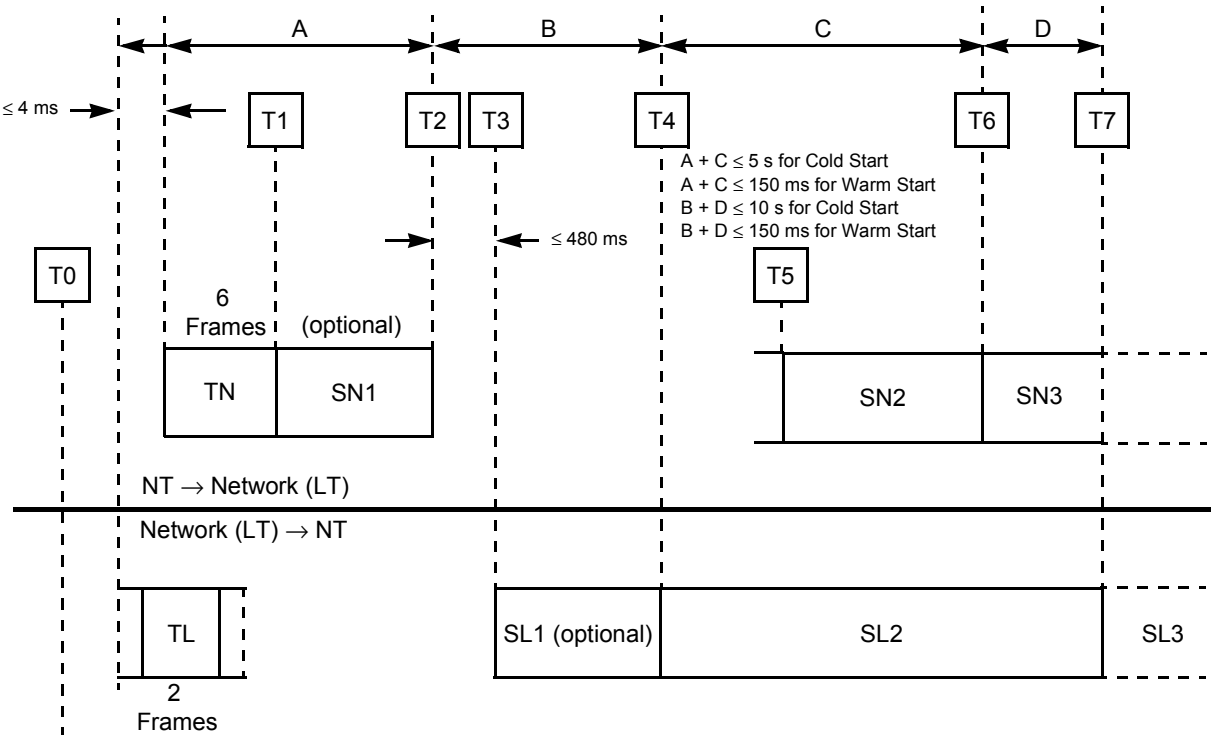
**Table 9-1. NT Mode Activation Signals**

| Information Station | Description |
|---|---|
| TN | A 10 kHz tone consisting of alternating 4 + 3 quats followed by 4 – 3 quats for a time period of six frames |
| SN0 | No signal transmitted |
| SN1 | Synchronization word present, no Superframe Synchronization word (ISW), and 2B+D+M = 1 |
| SN2 | Synchronization word present, no Superframe Synchronization word (ISW), and 2B+D+M = 1 |
| SN3 | Synchronization word present, Superframe Synchronization word (ISW) present, M channel bits active—transmitted 2B+D data is operational when the M4 ACT bit = 1. When M4 ACT = 0, the transmitted 2B+D data = 1. |

**Table 9-2. LT Mode Activation Signals**

| Information Station | Description |
|---|---|
| TL | A 10 kHz tone consisting of alternating 4 + 3 quats followed by 4 – 3 quats for a time period of two frames |
| SL0 | No signal transmitted |
| SL1 | Synchronization word present, no Superframe Synchronization word (ISW), and 2B+D+M = 1 |
| SL2 | Synchronization word present, Superframe Synchronization word (ISW), 2B+D = 0, and M = Normal |
| SL3 | Synchronization word present, Superframe Synchronization word (ISW) present, M channel bits active—transmitted 2B+D data is operational when the M4 ACT bit = 1. When M4 ACT = 0, the transmitted 2B+D data = 0. |

ANSI T1.601-1992 defines the M4 channel ACT bit (see U-BR0(b7) and U-BR1(b7)), which signals the far-end U-interface transceiver that the near-end is capable of transparently passing 2B+D data. **Figure 9-1** shows the activation diagram from the ANSI T1.601 specification. This figure can be used in conjunction with this text to understand the activation sequence.




| Time | Description of Event or State |
|---|---|
| T0 | Reset state |
| T1 | Network and NT are awake |
| T2 | NT discontinues transmission, indicating that NT is ready to receive signal |
| T3 | Network responds to termination of signal and begins transmitting signal toward the NT |
| T4 | Network begins transmitting SL2 toward the NT, indicating that the network is ready to receive SN2. |
| T5 | NT begins transmitting SN2 toward the network, indicating that the NT has acquire SW frame and detected SL2. |
| T6 | NT has acquired superframe marker, and is fully operational. |
| T7 | Network has acquired superframe marker, and is fully operational. |

**Figure 9-1.** MC145576 U-Interface Activation State Diagram

#### 9.2.1.1 Activation Signals for NT mode

The MC145576 U-interface can transmit any of the signals shown in **Table 9-1**. The actual procedure undertaken by the device using these five signals is described later in this section. **Section 5.3.3.9** describes how to control the transmit framer when it is desired to generate signals for test purposes.

### 9.2.1.2 Activation Initiation

The MC145576 U-interface transceiver can be activated in either of two ways. The external microcontroller can explicitly issue Activation Request (U-NR2(b3) = 1) or the transceiver detects an incoming 10 kHz wake-up tone. An LT configured U-interface transceiver searches for an NT sending the TN wake-up tone. An NT configured U-interface transceiver searches for an LT sending the TL wake-up tone. In IDL mode, the Activation in Progress status bit (U-NR1(b0)) is set to a 1 when an incoming 10 kHz wake-up tone is detected. In either case, Activation Request being set or a wake-up tone being detected, the U-interface proceeds with activation automatically and signals the result of the activation to the external microcontroller by setting status bits in NR1 to $B. An NT configured U-interface transceiver always initiates activation by sending a TN tone to the LT. This is done in response to the LT sending a TL or when the Activation Request bit (U-NR2(b3)) is set to a 1.

When configured for SCP mode, all appropriate maintenance channel registers should be initialized prior to setting Activation Request (U-NR2(b3)) or immediately after detecting Activation in Progress (U-NR1(b0)) = 1. In GCI mode, the MC145576 automatically initializes the maintenance channel registers.

**NOTE:** Some applications, such as U-repeaters, may require longer than 15 seconds of activation time. The 15-second activation timer can be disabled by setting Activation Timer Disable (U-BR11(b0)) to a 1.

### 9.2.1.3 Activation Indication

The Linkup status bit (U-NR1(b3)) is used to signify that the loop is active. With MC145576 configured as an NT, this corresponds to NT transmitting SN3 and receiving SL3. When the U-interface is fully active, Superframe Sync (U-NR1(b1)) and Linkup (U-NR1(b3)) are set to a 1.

Whenever the MC145576 detects loss of Superframe Synchronization, U-NR1 becomes $8 and an interrupt is generated if enabled. This indicates that loss of Superframe Synchronization has been detected. When Superframe Synchronization is lost for more than 480 ms, MC145576 always deactivates and sets U-NR1 = $4 error indication, and issues an interrupt if enabled. When the error condition causing loss of Superframe Synchronization goes away before 480 ms has elapsed, U-NR1 returns to $B and an interrupt is generated if enabled. It is not necessary to set Customer Enable (U-NR2(b0)) to a 1 when U-NR1 returns to $B. The MC145576 continually monitors the error on its recovered signal. If the internally monitored error rate becomes too large, MC145576 loses data transparency and U-NR1 changes to $A or $8 and issues an interrupt.

**NOTE:** Loss of Superframe Synchronization always means that data transparency is lost, but loss of data transparency does not always mean that Superframe Synchronization is lost. Also, loss of signal always means that Superframe Synchronization is lost. There is no time limit on how long U-NR1 may read as $A when data transparency is lost. There is a 480-ms time limit on U-NR1 reading as $8. ANSI T1.601 only indicates that U-interface transceivers must deactivate when Superframe Synchronization or receive signal is lost for more than 480 ms. If the error condition goes away, U-NR1

returns to $B and an interrupt is generated, if enabled. Loss of Superframe Synchronization may be due to a high internally detected error rate on recovered data or the temporary loss of received signal.

#### 9.2.1.4 NT Deactivation Procedures and Warm Start

ANSI T1.601 specifies that NT can not initiate deactivation. The MC145576 deactivates to a warm start condition when Deactivation Request (U-NR2(b2)) is set to a 1 prior to LT deactivating the U-interface. This should be done in response to the M4 channel DEA bit being received as 0 by NT when the loop is active. If Deactivation Request (U-NR2(b2)) is not set to a 1 before LT deactivates the U-interface, MC145576 deactivates to a cold start condition and gives an error indication interrupt. Deactivation Request is automatically set if the M4 maintenance bits are operated with automatic verification of activation and deactivation. So when LT deactivates the line, NT deactivates to a warm start condition. See **Section 5.3.3.10** and **Section 5.3.4.8** for more information.

#### 9.2.1.5 Initial State of B1 and B2 Channels

The MC145576 comes out of hardware or software reset with customer data disabled. This corresponds to Customer Enable (U-NR2(b0)) cleared to 0. When the M4 channel Verified ACT/DEA mode is not used, the Customer Enable (U-NR1(b0)) bit must be set to a 1 to enable data transparency when U-NR1 becomes $B after initial activation. The B1, B2, and D channels transmitted on the IDL interface are automatically enabled after the MC145576 activates. Data on the B1 channel from the U-interface corresponds to data in the B1 channel timeslot on the IDL interface. Data on the B2 channel from the U-interface corresponds to data on the B2 channel timeslot on the IDL interface. The B1 and B2 channel timeslots on the IDL interface can be swapped by setting Swap B1/B2 (U-NR5(b0)) to a 1.

#### 9.2.1.6 Additional Notes—Maintenance Channel Bits

The received EOC, M4, M5, and M6 channel bits are available in registers R6, BR1, and BR3 once linkup has been attained. The Customer Enable bit (U-NR2(b0)) affects only the two B channels and the D channel. See **Section 5.3.3.1** through **Section 5.3.3.4** and **Section 5.3.3.10** for a full description of the maintenance channel bits and their control.

## 9.2.2 S/T-Interface Operations

CCITT I.430, ETSI ETS 300012, and ANSI T1.605 define five information states for the S/T -interface. When the NT is in the fully operational state, it transmits INFO 4. When the TE is in the fully operational state, it transmits INFO 3. INFO 1 is transmitted by the TE when it wants to wake up the NT. INFO 2 is transmitted by the NT when it wants to wake up the TE, or in response to the TE's transmitted INFO 1. These states cause unique patterns of symbols to be transmitted over the S/T-interface. Only when the S/T loop is in the fully activated state are the 2B+D channels of data transmitted over the interface.

### 9.2.2.1 Transmission States for MC145576 S/T-Interface

The MC145576 S/T-interface can be in any of the transmission states shown in **Table 9-3**.

**Table 9-3. NT Mode Transmission States**

| Information State | Description |
|---|---|
| INFO 0 | The NT transmits 1s in every bit position. This corresponds to no signal being transmitted. |
| INFO 2 | The NT sets its B1, B2, D, and E channels to 0. The A bit is set to 0. (See **Section 9.2.2.9**). |
| INFO 4 | INFO 4 corresponds to frames containing operational data on the B1, B2, D, and E channels. The A bit is set to 1. |

### 9.2.2.2 Activation of S/T Loop by TE

The TE activates an inactive loop by transmitting INFO 1 to the MC145576. The MC145576, upon detecting INFO 1 from the TE, responds with INFO 2. The TE, upon receiving a signal from the NT, ceases transmission of INFO 1, reverting to transmitting INFO 0. After synchronizing to the received signal and having fully verified that it is INFO 2, the TE responds with INFO 3, thus activating the loop.

### 9.2.2.3 Activation Procedures Ignored

The MC145576 has the capability of being forced into the highest transmission state. This is accomplished by setting S/T-BR7(b7) to a 1. Thus, when this bit is set in the NT, it forces the NT to transmit INFO 4.

**NOTE:** CCITT I.430, ETSI ETS 300012, and ANSI T1.605 specifications allow a TE to be activated by reception of INFO 4, without having to go through the intermediate handshaking. This is to allow for the situation where a TE is connected to an already active loop. However, an NT can not be activated by a TE sending it INFO 3, without going through the intermediate INFO 1, INFO 2, INFO 3, and INFO 4 states. This Activation Procedures Ignored feature is provided for test purposes, allowing the NT to forcibly activate the TE(s).

#### 9.2.2.4 Frame Sync/NT Mode

When the S/T interface is receiving INFO 3 from the TE(s) and has achieved frame synchronization, it sets the FSYNC status bit S/T-NR1(b0) high. See **Section 5.4.1.2** for detailed information.

#### 9.2.2.5 Activation Indication

S/T-NR1(b3), the Activation Indication bit, signifies when the loop is fully active. For the MC145576, this corresponds to the NT transmitting INFO 4 and receiving INFO 3. When the loop is in the fully active state, S/T-NR1(b3) is internally set high.

#### 9.2.2.6 S/T-NR1(b2) Error Indication (EI)

S/T-NR1(b2) is set by the MC145576 S/T interface to indicate an error condition has been detected by the activation state machine of the transceiver, as outlined in CCITT I.430, ETSI ETS 300012, and ANSI T1.605. The low-to-high level transition of the EI bit corresponds to the EI1 error indication reporting, while the high-to-low level transition of the EI bit corresponds to the EI2 error indication reporting recovery. Note that S/T-NR1(b2) is a read only bit.

#### 9.2.2.7 Deactivation Procedures

CCITT I.430, ETSI ETS 300012, and ANSI T1.605 specifications dictate that only an NT can deactivate the S/T loop. Intuitively, this has to be the case because in a passive bus if one TE sends INFO 0, seeking to deactivate the loop, the other TE's INFO 3 simply overrides it. An NT transmits INFO 0 to the TE(s) when it wishes to deactivate the S/T loop. This is done by setting S/T-NR2(b2) Deactivation Request to a 1. Note that this bit is internally reset to 0 after the internal activation state machine has recognized its active transition.

#### 9.2.2.8 Initial State of B1 and B2 Channels

For the MC145576, S/T-NR5(b3–b2) corresponds to IDLE B1 channel on S/T loop, and IDLE B2 channel on S/T loop, respectively. The device comes out of a hardware or software reset with these two bits reset to 0. Thus, the NT comes out of reset with the B1 and B2 channels enabled. When the NT is transmitting INFO 4, data on the B1 and B2 IDL timeslots will be modulated onto the S/T loop. Setting either of these nibble bits idles the corresponding B channel on the S/T loop. Note that putting a B channel in the idle mode affects only the transmitted B channel. The demodulated B data is still transmitted out on IDL Tx, in accordance with the IDL specification.

### 9.2.2.9 Additional Notes

The following notes provide additional operational information:

- **Echo Channel**—The NT demodulates the 2B+D data received from the TE(s). In addition to passing this data onto the network, the NT echoes the D channel data back to the TE(s) using the echo channel. This echo channel is monitored by the TEs and used in the D channel contention algorithm.
- **A Bit**—An S/T frame consists of 48 bauds. In the NT to TE direction, one of these bauds is for the A bit. The A bit is set to 1 when the S/T loop is in the fully activated state and is set to 0 at all other times. Thus, when the NT is transmitting INFO 2, the A bit is set to 0. When the NT is transmitting INFO 4, the A bit is set to 1.
- **SCP Indication of Transmit and Receive States**—There are two SCP bits, S/T-BR11(b5–b4), used to signify what INFO state the MC145576 S/T-interface is receiving. In addition to this, S/TR-BR11(b3–b2) are used to signify what INFO state the MC145576 is transmitting. Refer to **Section 5.4.2.10** for a detailed description of these bits.

## 9.3 GCI Activation/Deactivation Time Diagrams

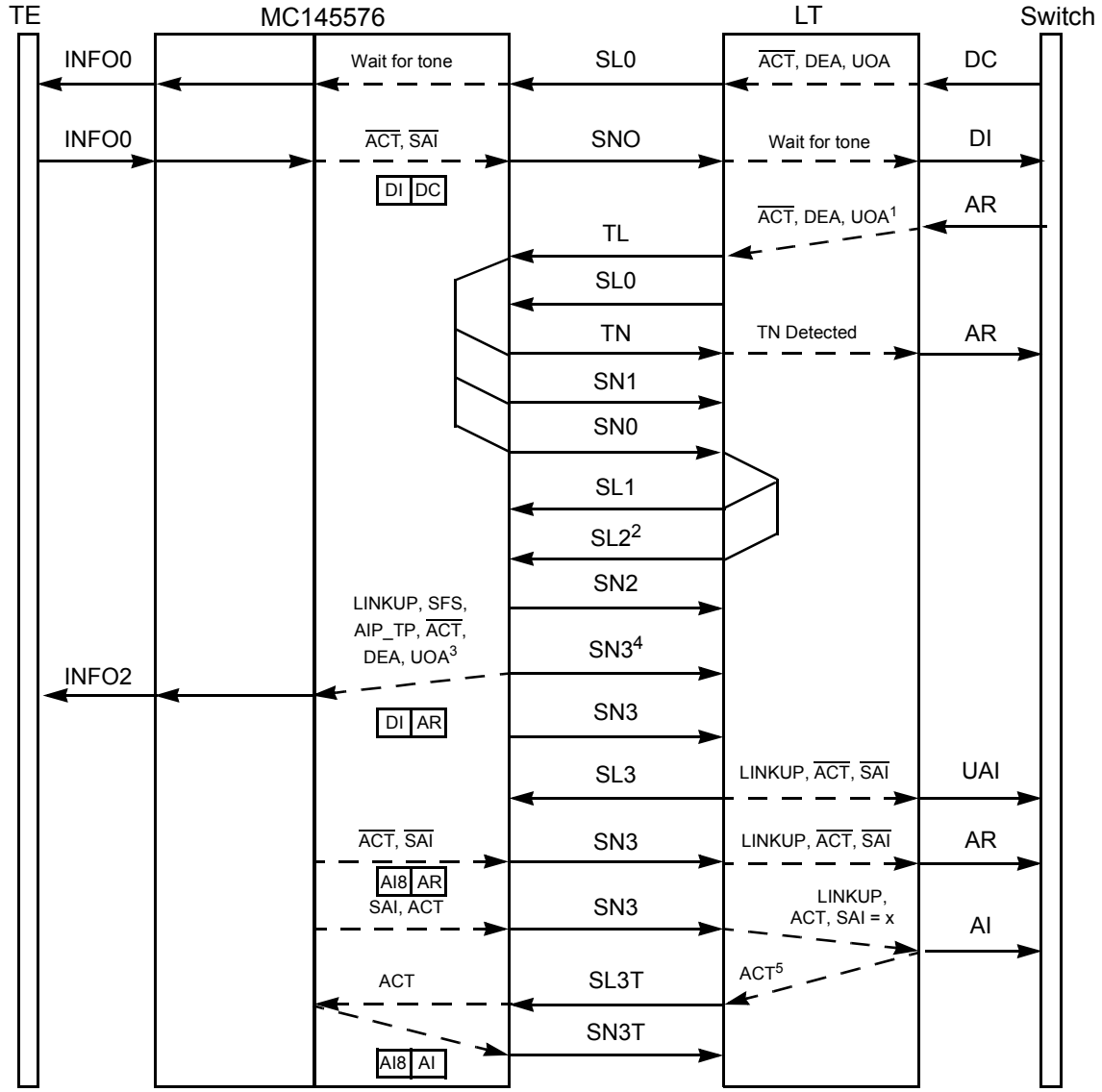
This section contains the time flow diagrams that detail the various activation and deactivation scenarios for the MC145576 transceivers. **Figure 9-2** through **Figure 9-17** are the activation diagrams for the MC145576 operating in GCI mode.

### 9.3.1 Introduction

Activation can be initiated from all three interfaces: LT, TE, and GCI. In the Activation/Deactivation Flow Diagrams the LT interface in shown on the right, the S/T-interface (TE) is shown on the left, and the GCI terminal interface is shown in the middle and indicated in the figures by the following format:

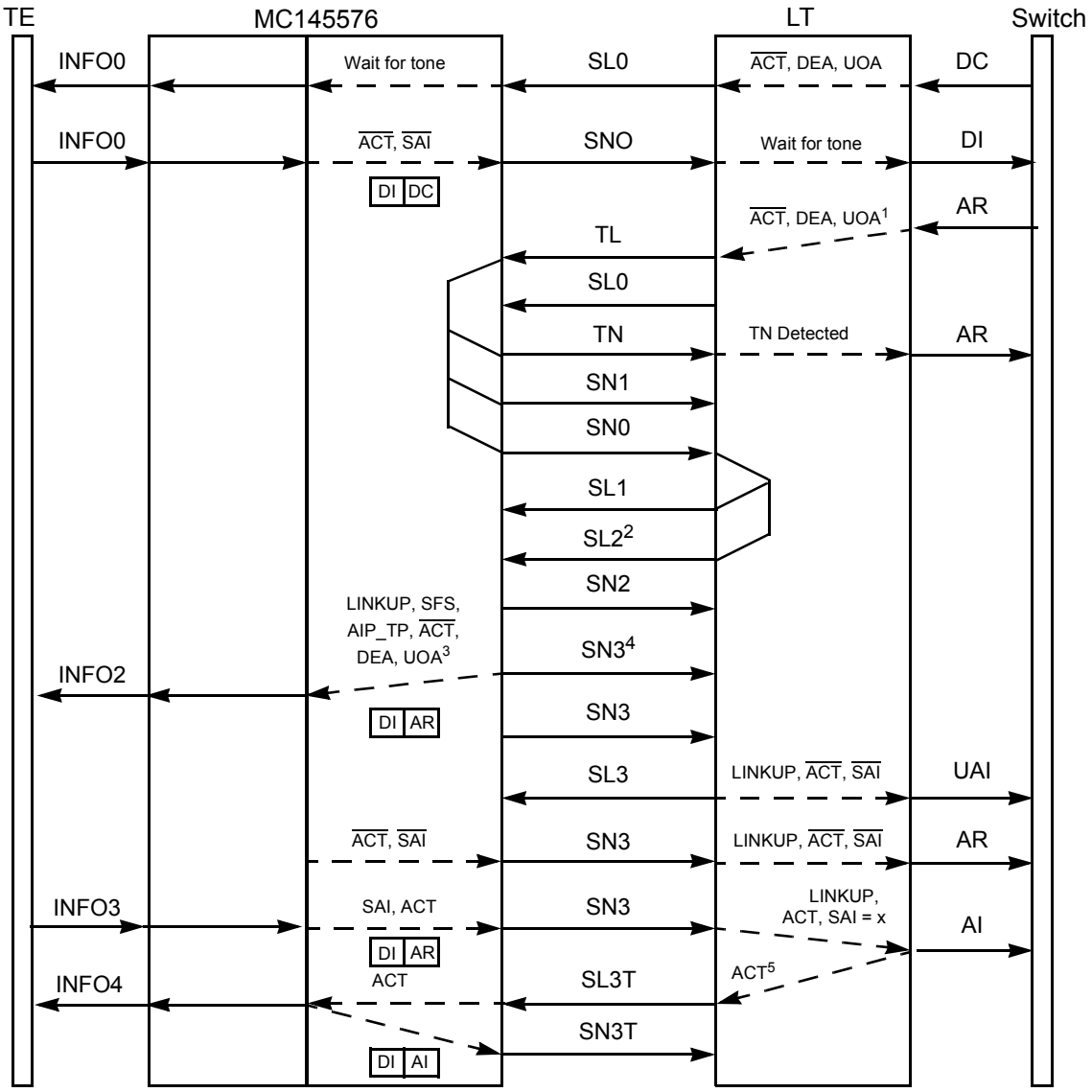
| COM | IND |
|---|---|
| AI8 | AI |

### 9.3.2 LT Initiated Activation.



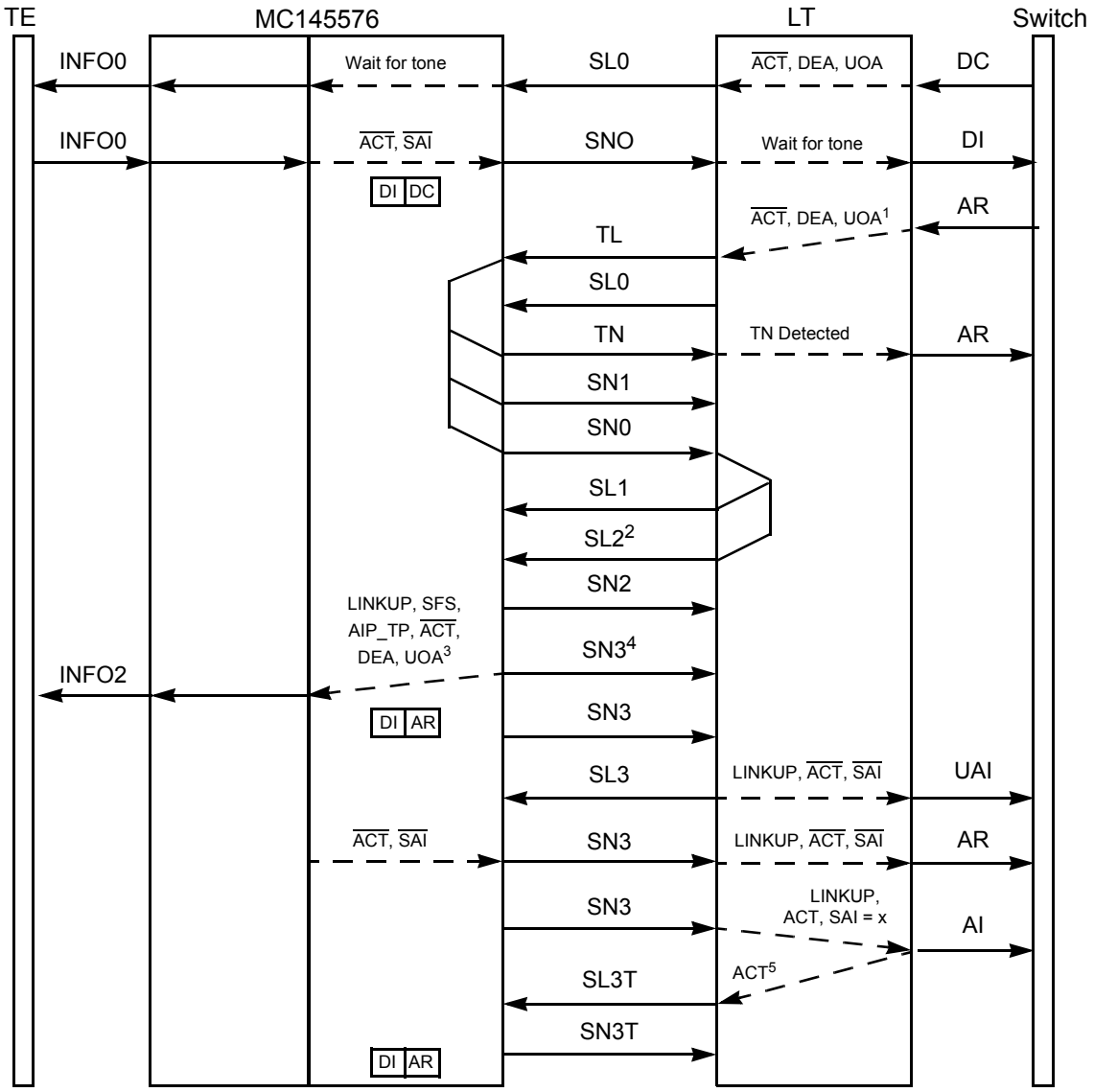

**Notes:** **1.** No change in transmitted maintenance bits at this time.
**2.** Maintenance bits are sent with meaningful data (Normal field in Table 5, T1E1.4).
**3.** Linkup, SFS, AIP_TP correspond to NR1 bits 3, 1, and 0 respectively.
**4.** No change in upstream maintenance bits; ACT = 0, SAI = 0.
**5.** The downstream ACT bit is set by issuance of the AI.

**Figure 9-2.** Time Diagram for Total Activation Initiated by the LT with Terminal-only Connection



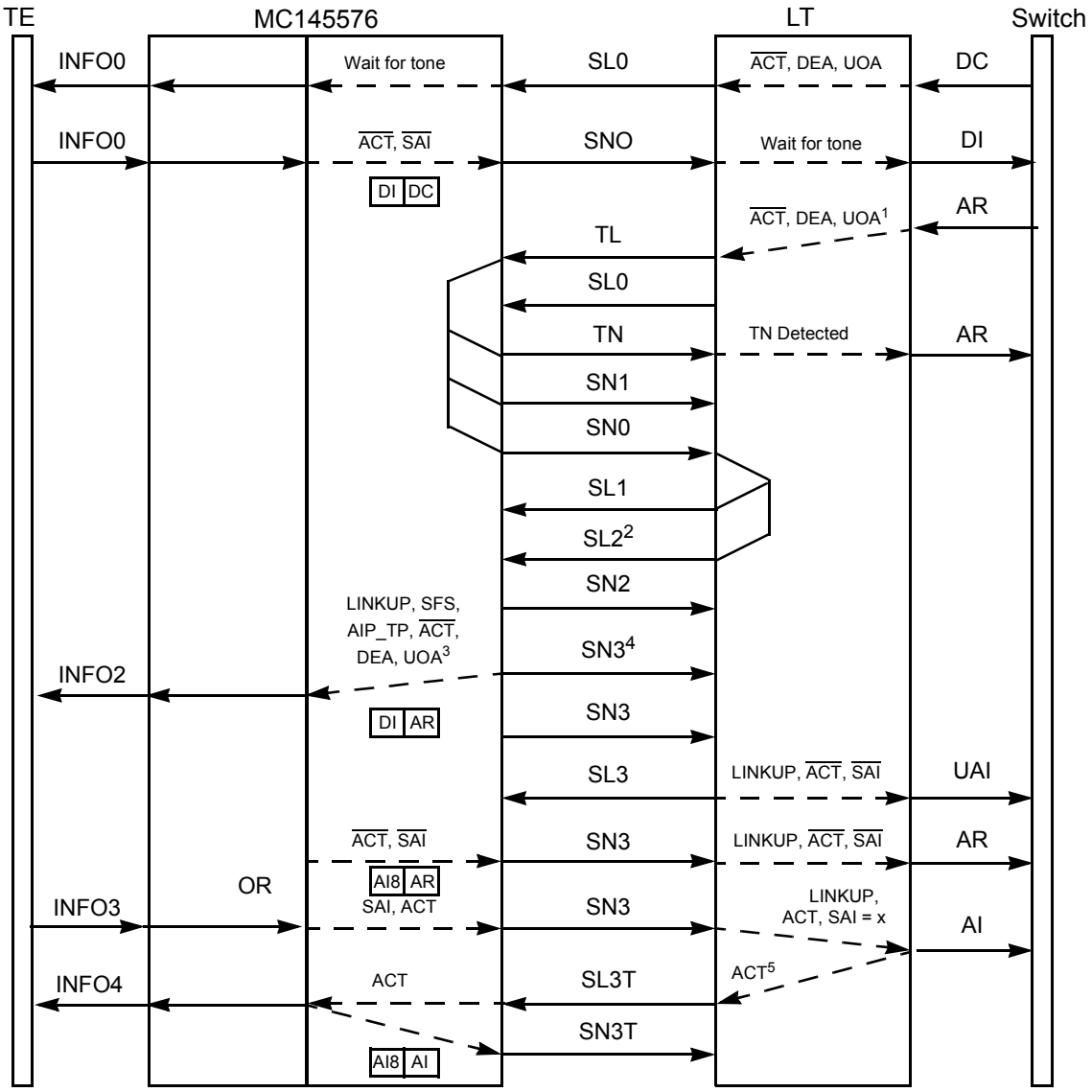

**Notes:** **1.** No change in transmitted maintenance bits at this time.
**2.** Maintenance bits are sent with meaningful data (Normal field in Table 5, T1E1.4).
**3.** Linkup, SFS, AIP_TP correspond to NR1 bits 3, 1, and 0 respectively.
**4.** No change in upstream maintenance bits; ACT = 0, SAI = 0.
**5.** The downstream ACT bit is set by issuance of the AI.

**Figure 9-3.** Time Diagram for Total Activation Initiated by the LT with TE-only Connection




**Notes:** **1.** No change in transmitted maintenance bits at this time.
**2.** Maintenance bits are sent with meaningful data (Normal field in Table 5, T1E1.4).
**3.** Linkup, SFS, AIP_TP correspond to NR1 bits 3, 1, and 0 respectively.
**4.** No change in upstream maintenance bits; ACT = 0, SAI = 0.
**5.** The downstream ACT bit is set by issuance of the AI.

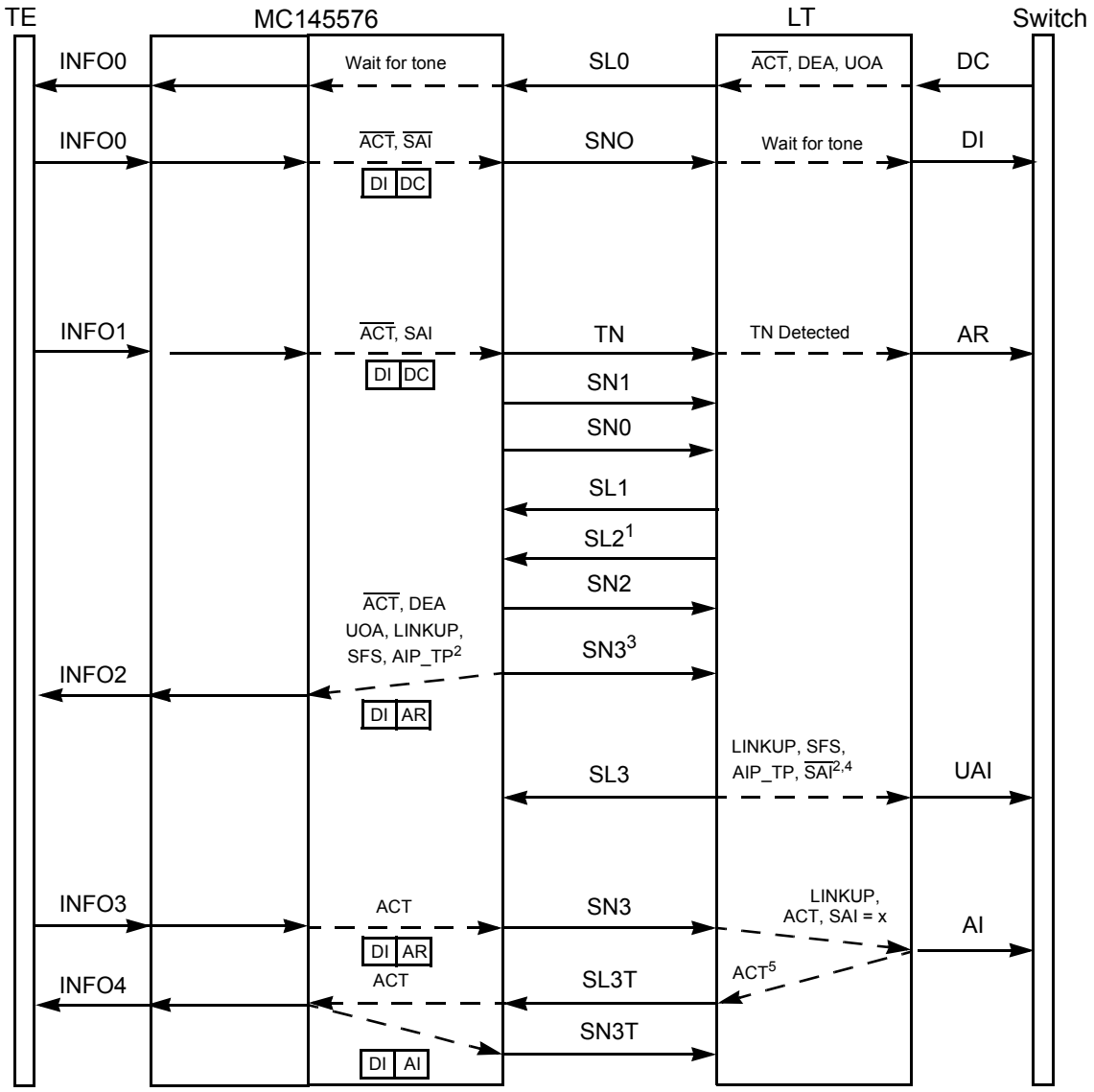
**Figure 9-4.** Time Diagram for Total Activation Initiated by the LT with No TE or Terminal Connected




**Notes:** **1.** No change in transmitted maintenance bits at this time.
**2.** Maintenance bits are sent with meaningful data (Normal field in Table 5, T1E1.4).
**3.** Linkup, SFS, AIP_TP correspond to NR1 bits 3, 1, and 0 respectively.
**4.** No change in upstream maintenance bits; ACT = 0, SAI = 0.
**5.** The downstream ACT bit is set by issuance of the AI.

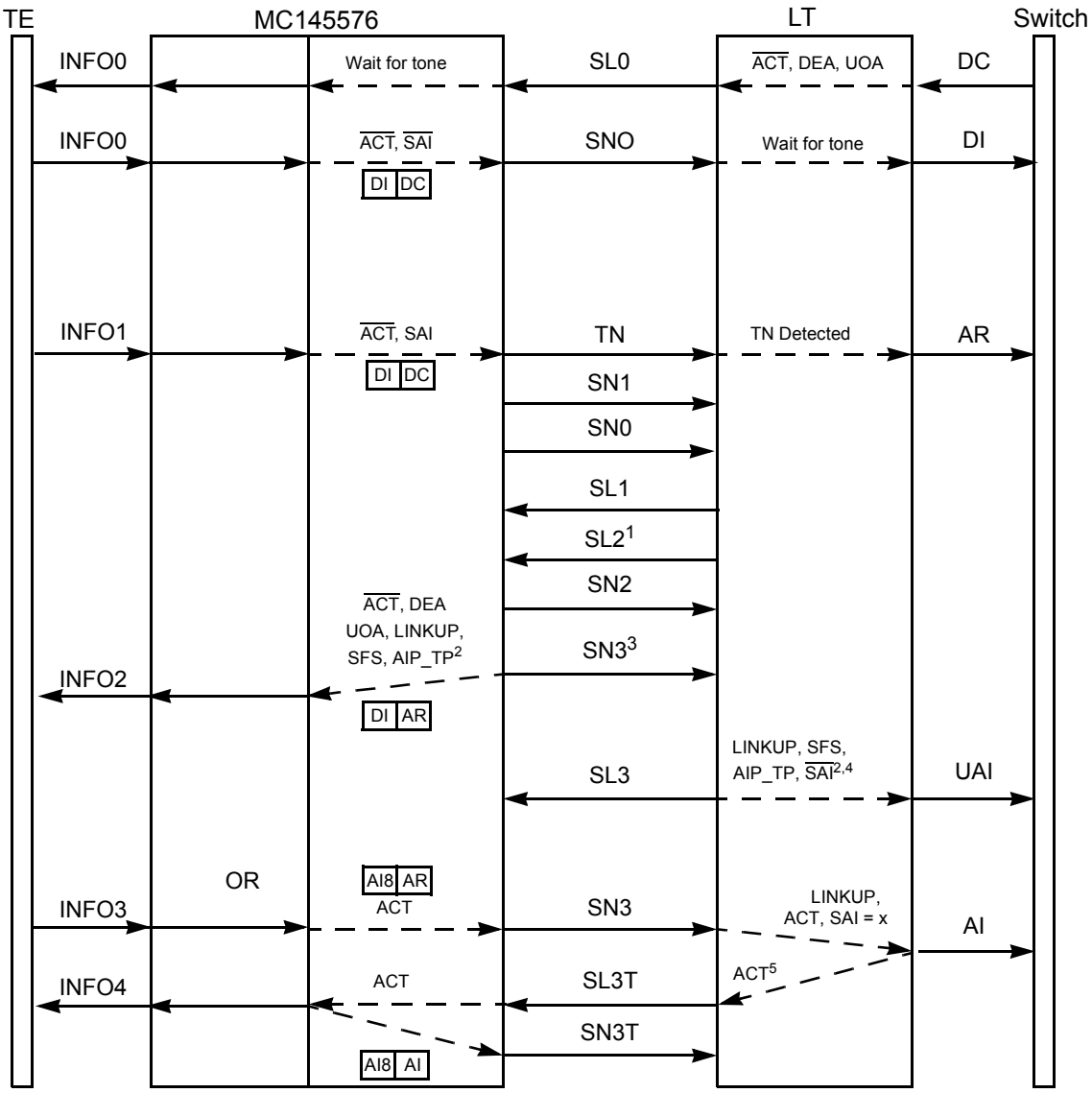
**Figure 9-5.** Time Diagram for Total Activation Initiated by the LT with Both TE and Terminal Connections

### 9.3.3 TE Initiated Activation




**Notes:** **1.** Maintenance bits are sent with meaningful data (Normal field in Table 5, T1E1.4).
**2.** Linkup, SFS, AIP_TP correspond to NR1 bits 3, 1, and 0 respectively.
**3.** No change in upstream maintenance bits; ACT = 0, SAI = 0.
**4.** Because the upstream SAI bit is set by the upstream AR command, the indication UAI is never issued, and AR continues to appear on the C/I channel.
**5.** The downstream ACT bit is set by issuance of the AI.

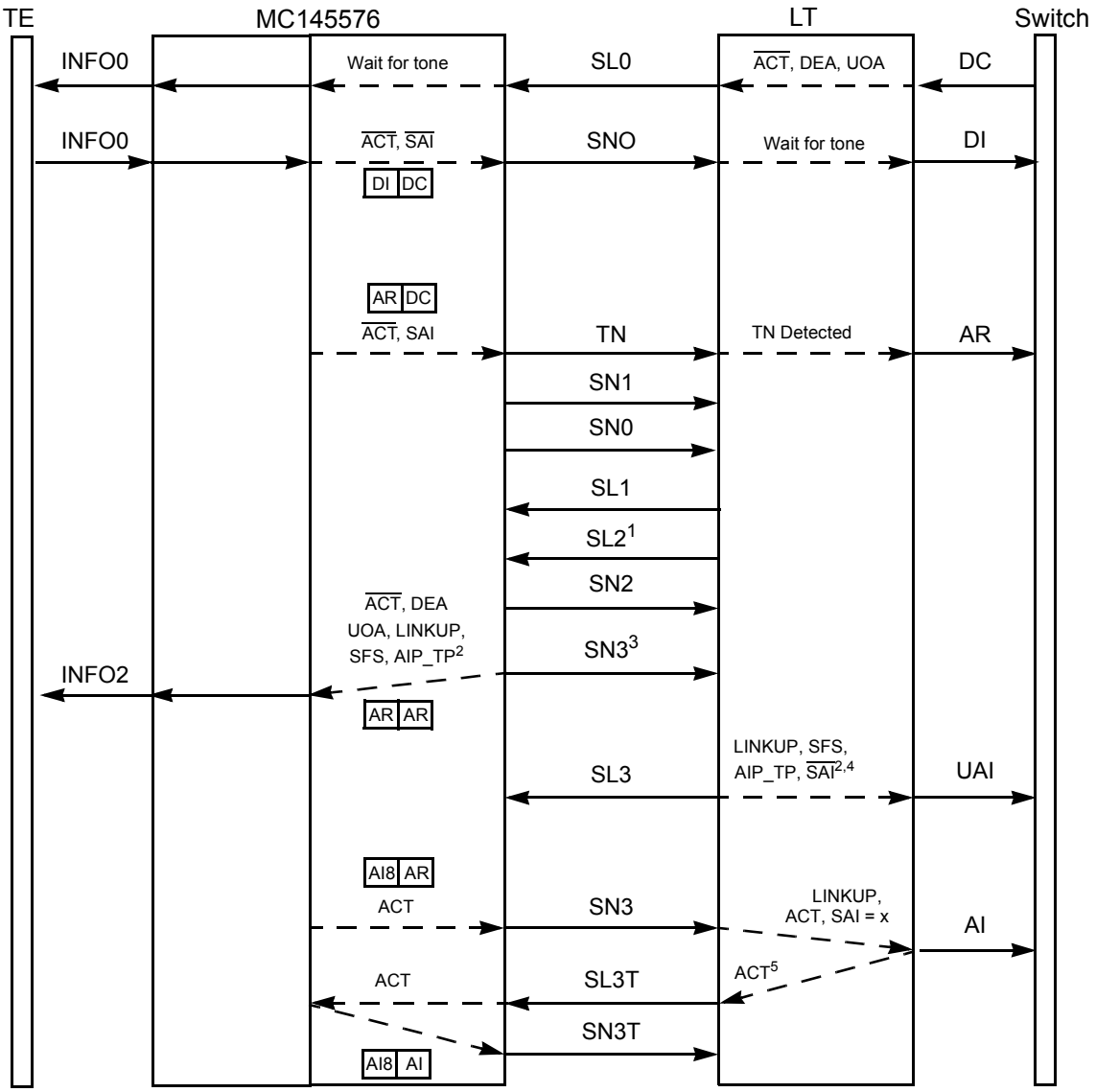
**Figure 9-6.** Time Diagram for Total Activation Initiated by the Terminal Equipment with No Terminal Connection




**Notes:**
1. Maintenance bits are sent with meaningful data (Normal field in Table 5, T1E1.4).
2. Linkup, SFS, AIP_TP correspond to NR1 bits 3, 1, and 0 respectively.
3. No change in upstream maintenance bits; ACT = 0, SAI = 0.
4. Because the upstream SAI bit is set by the upstream AR command, the indication UAI is never issued, and AR continues to appear on the C/I channel.
5. The downstream ACT bit is set by issuance of the AI.

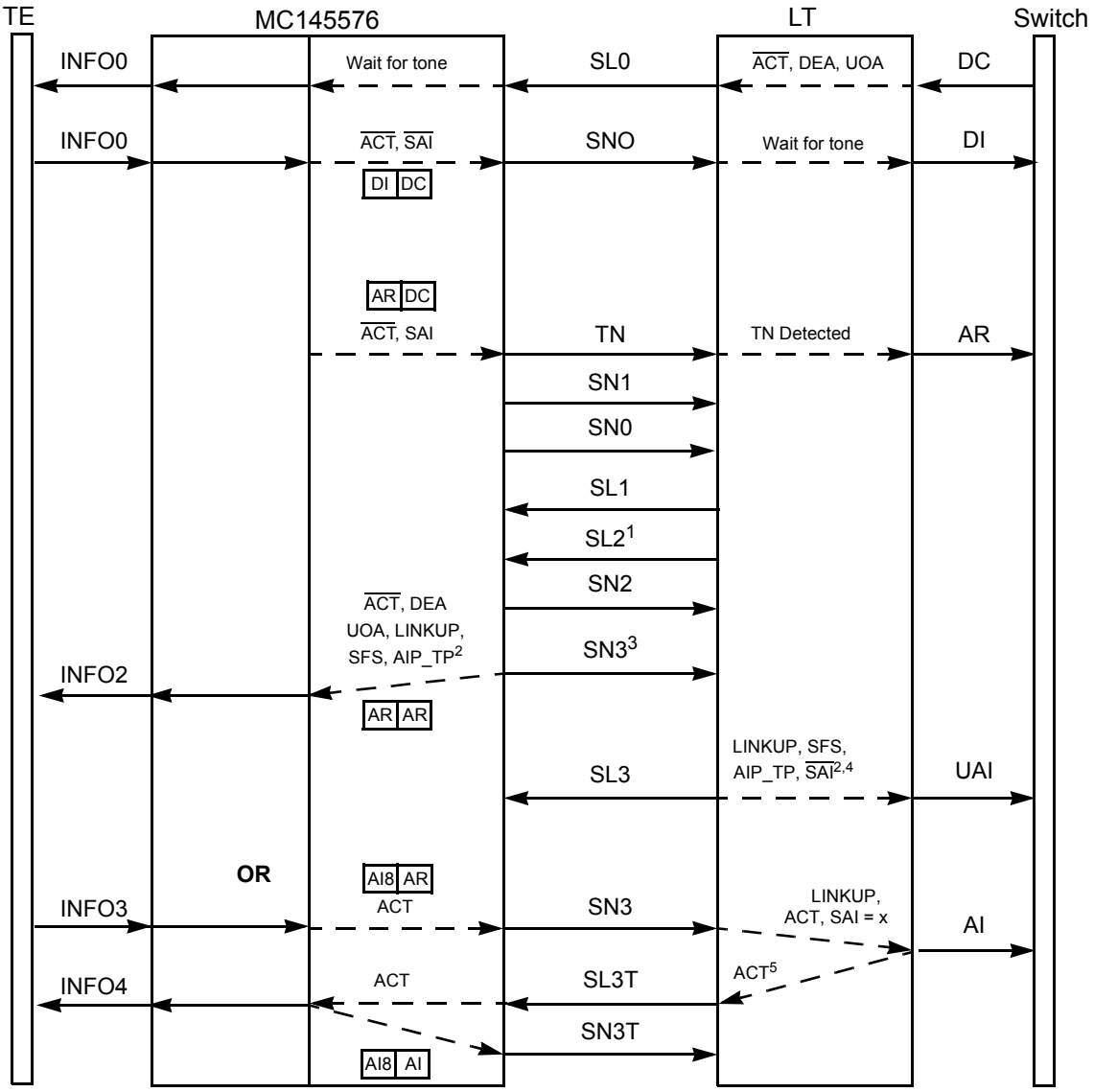
**Figure 9-7.** Time Diagram for Total Activation Initiated by the Terminal Equipment with Terminal Connection

### 9.3.4 Terminal Initiated Activation




**Notes:** **1.** Maintenance bits are sent with meaningful data (Normal field in Table 5, T1E1.4).
**2.** Linkup, SFS, AIP_TP correspond to NR1 bits 3, 1, and 0 respectively.
**3.** No change in upstream maintenance bits; ACT = 0, SAI = 0.
**4.** Because the upstream SAI bit is set by the upstream AR command, the indication UAI is never issued, and AR continues to appear on the C/I channel.
**5.** The downstream ACT bit is set by issuance of the AI.

**Figure 9-8.** Time Diagram for Total Activation Initiated by the Terminal with No TE Connection




**Notes:**
1. Maintenance bits are sent with meaningful data (Normal field in Table 5, T1E1.4).
2. Linkup, SFS, AIP_TP correspond to NR1 bits 3, 1, and 0 respectively.
3. No change in upstream maintenance bits; ACT = 0, SAI = 0.
4. Because the upstream SAI bit is set by the upstream AR command, the indication UAI is never issued, and AR continues to appear on the C/I channel.
5. The downstream ACT bit is set by issuance of the AI.

**Figure 9-9.** Time Diagram for Total Activation Initiated by the Terminal with TE Connection

### 9.3.5 LT Initiated Deactivation

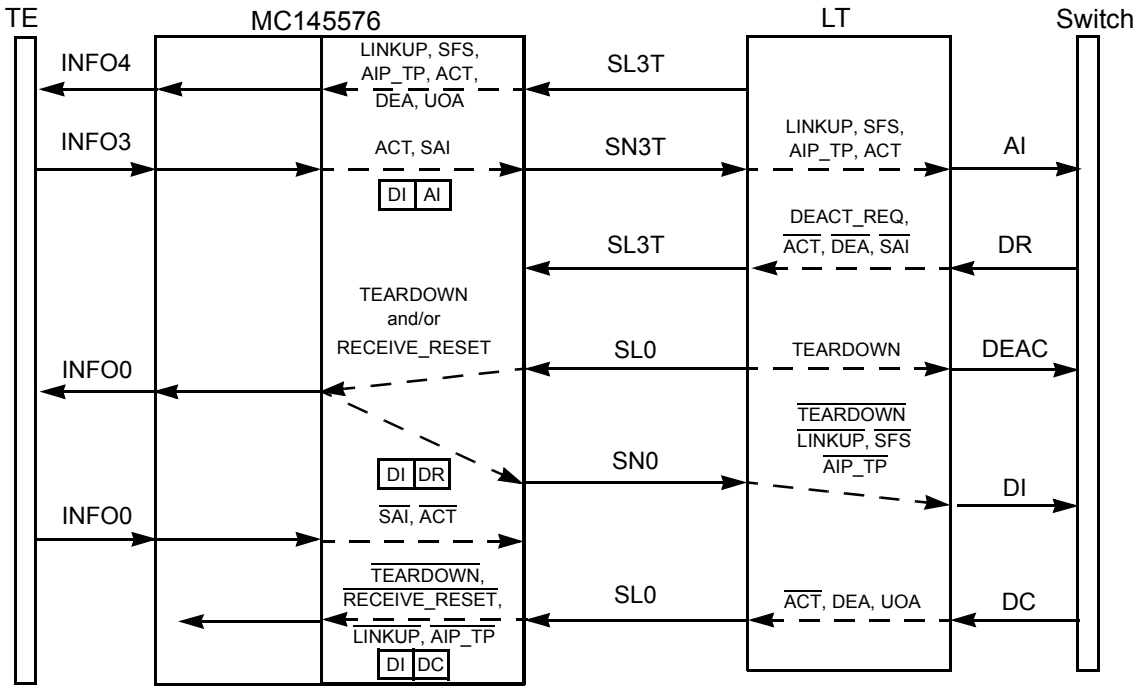



**Figure 9-10.** Time Diagram for Deactivation with TE Connection (Always Initiated by the LT)

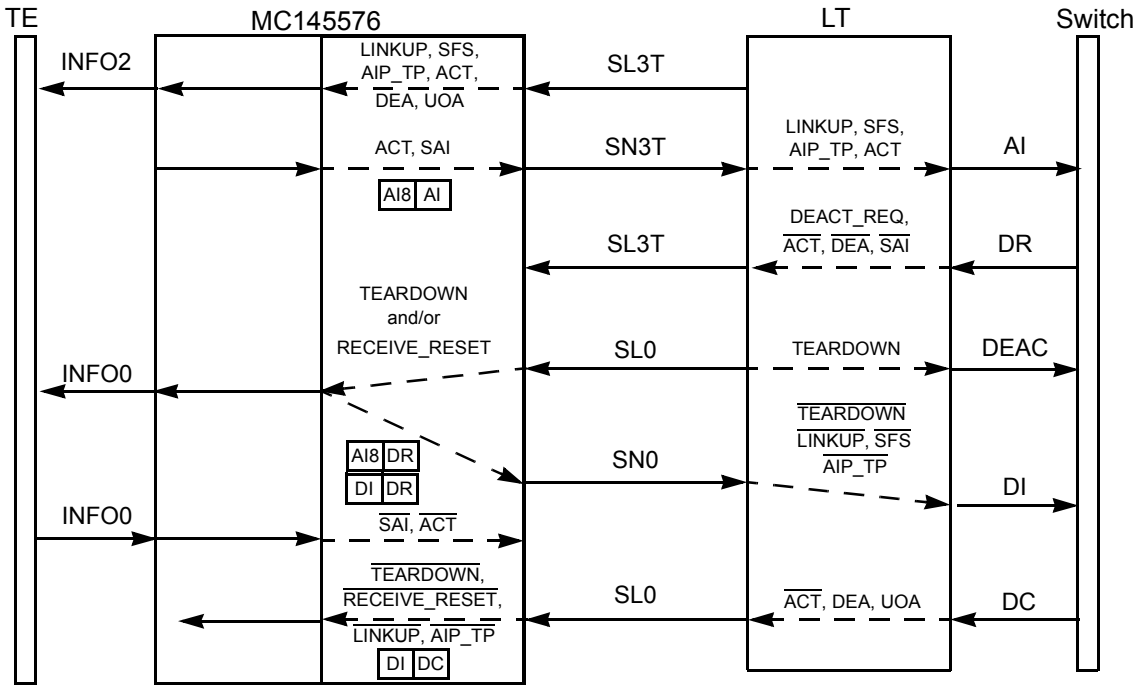



**Figure 9-11.** Time Diagram for Deactivation with Terminal-only Connection (Always Initiated by the LT)

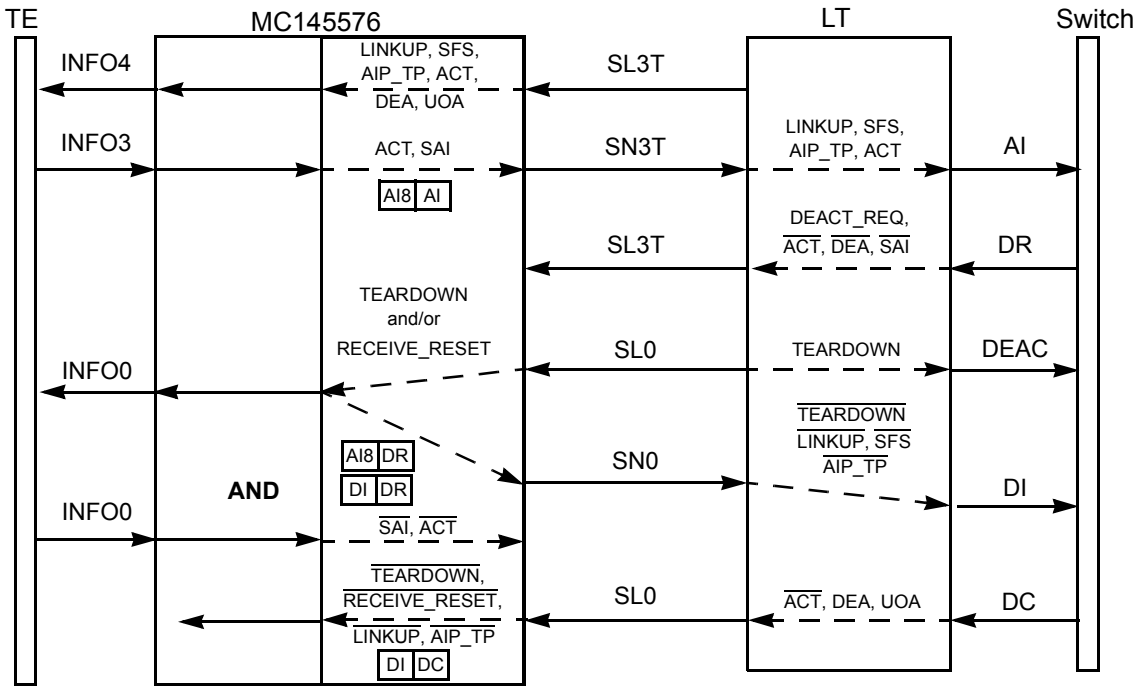



**Figure 9-12.** Time Diagram for Deactivation with Both TE and Terminal Connections (Always Initiated by the LT)

### 9.3.6 U-Interface Only Activation

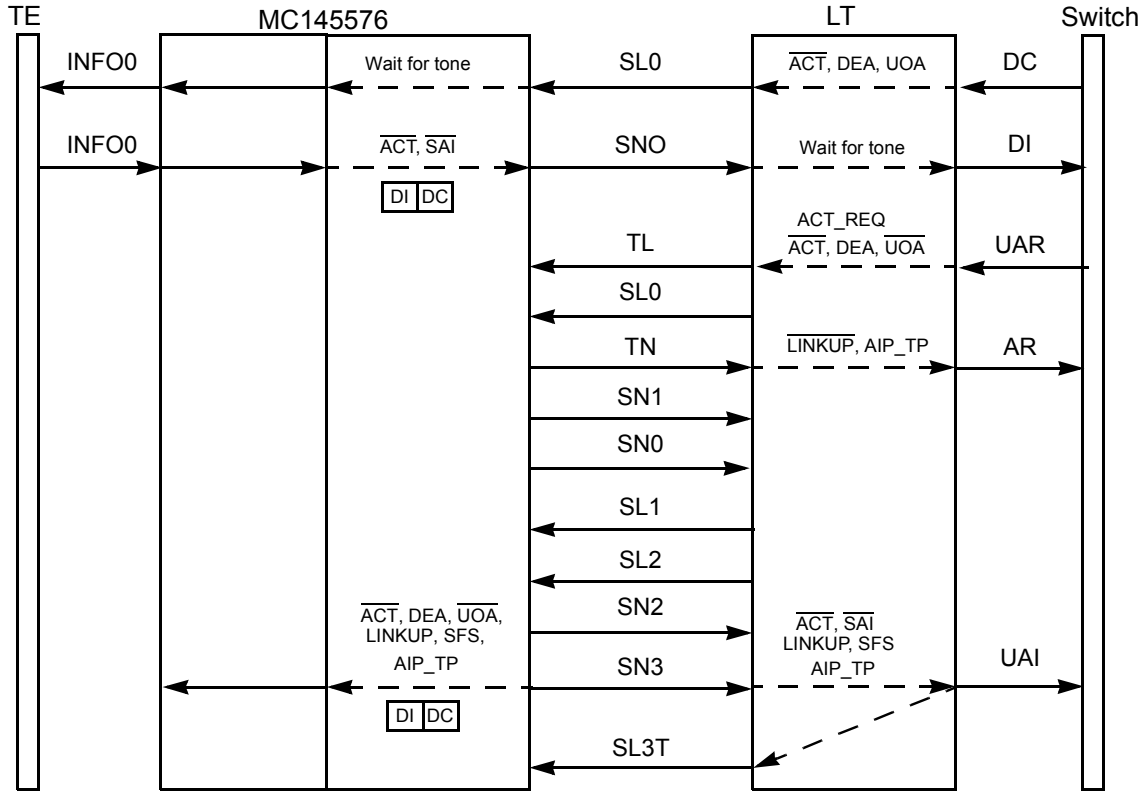



**Figure 9-13.** Time Diagram of a U-Only Activation (Always Initiated by the LT)

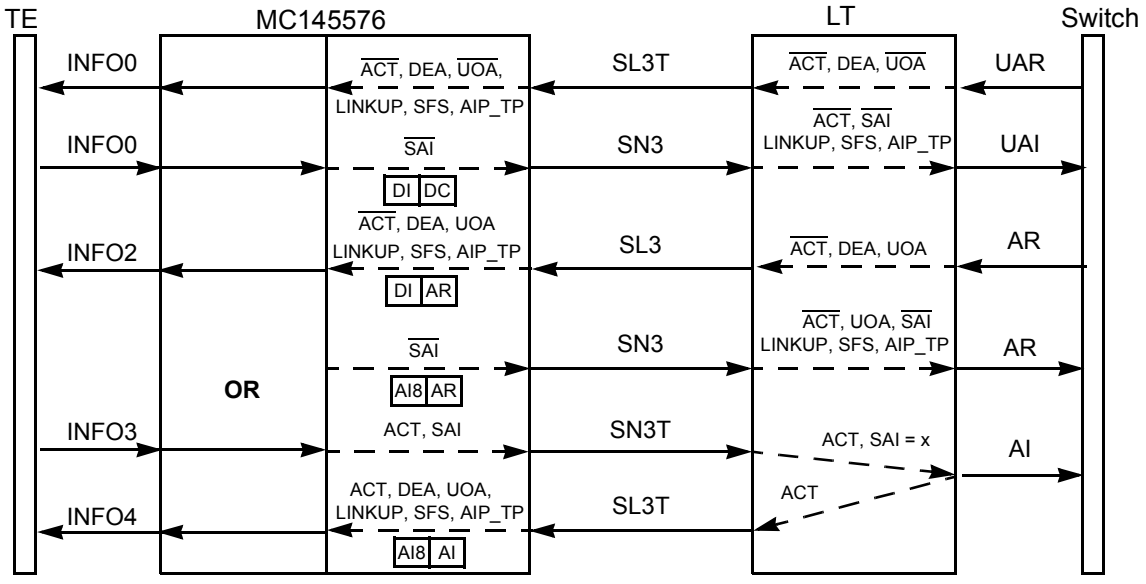



**Figure 9-14.** Time Diagram for a Transition from DSL-Only Activation to Total Activation Initiated by the LT

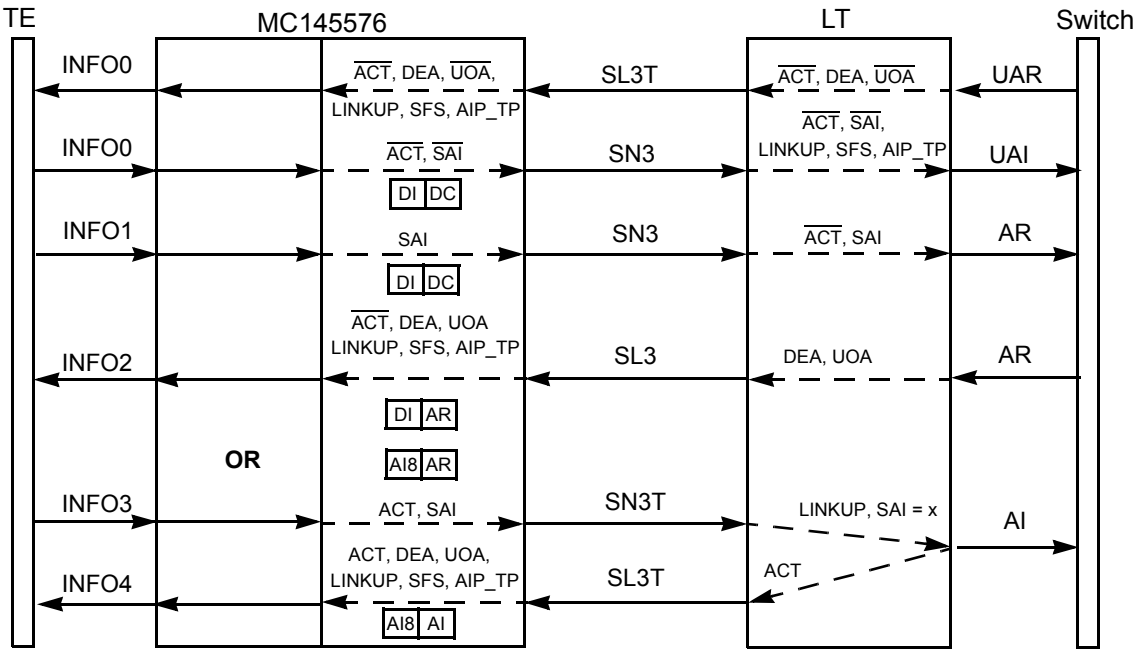



**Figure 9-15.** Time Diagram for a Transition from DSL-Only Activation to Total Activation Initiated by the TE With Terminal Connection

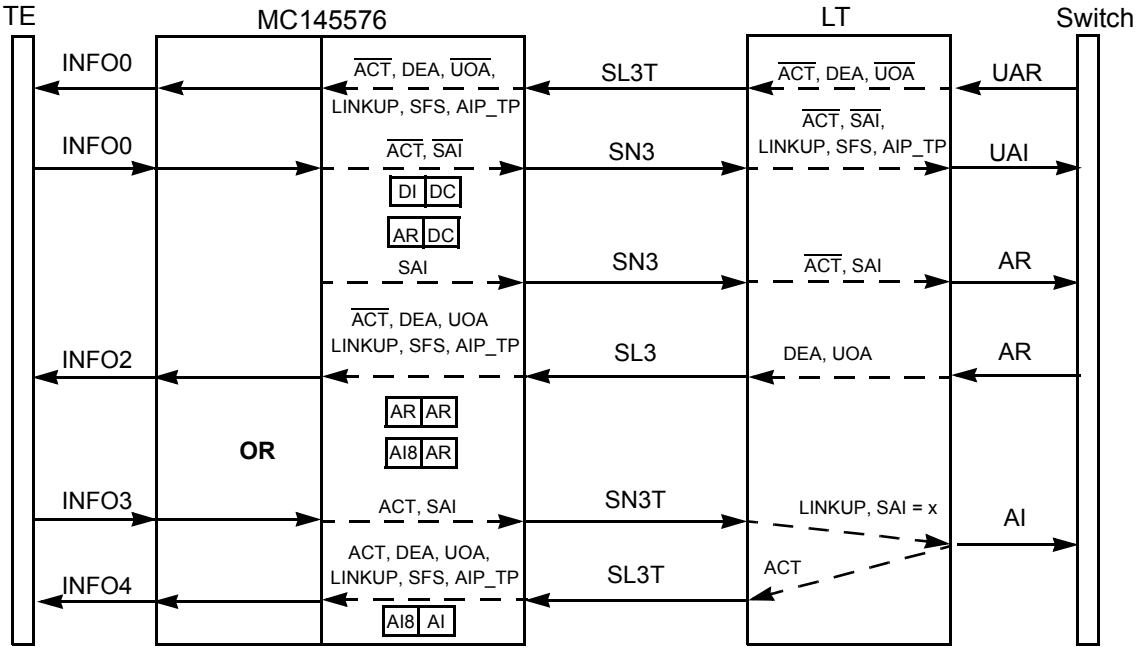
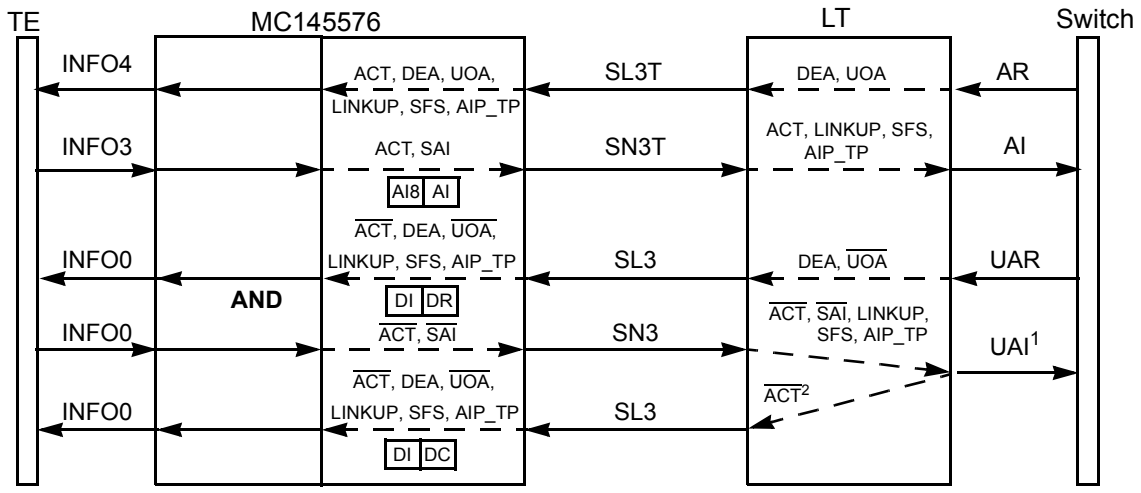



**Figure 9-16.** Time Diagram for a Transition from DSL-Only Activation to Total Activation Initiated by the Terminal With TE Connection




**Notes:** **1.** If the received ACT = 0 and SAI = 0 do not occur at the same time in the LT, it is possible that prior to the UAI indication, AR will be issued by the LT, until the moment in which both maintenance bits are 0 in the LT. Then, UAI will be issued, as shown.

**2.** The ACT bit is reset automatically by the MC145576 without any special command.

**Figure 9-17.** Time Diagram for a Transition from Total Activation to DSL-Only Activation (Always Initiated by the LT)

# 10

# Transmission Line Interface Circuitry

## 10.1 S/T Interface

The MC145576 has an ISDN S/T interface fully compliant with ITU .430, ETSI ETS 300012, and ANSI T1.605. As such it is designed to interface with a four wire transmission medium, one pair being the transmit path, the other pair the receive path. TxP-T and TxN-T, a fully differential output transmit pair from the MC145576, is designed to interface to the transmit pair of the transmission medium via auxiliary discrete components and a 1:2.5 turns ratio transformer. RxP-T and RxN-T form a high-impedance differential input pair used for coupling the receive line signal through a 1:2.5 turns ratio transformer. This interface is the same as that used with the MC145574, S/T Transceiver.

### 10.1.1 S/T Transmit Line Interface Circuitry

The TxP-T and TxN-T pins on the MC145576 act as a current limited differential voltage source pair. The TxP-T and TxN-T pair behave as active drivers when creating logical zero line signals (CCITT I.430 and ANSI T1.605 define the nominal pulse amplitude to be 750 mV, zero to peak, for a 50-ohm load) and are high-impedance outputs when generating logical one signals. The transmit circuitry within the S/T interface is designed to operate with a 1:2.5 turns ratio line interface transformer. The transmit transformer is similar in design to the receive transformer.

The TxP-T and TxN-T pair operate as a 2.8-volt current limited differential voltage source. As such two 5% series resistors should be inserted in the line interface circuit such that the combined resistance of these two resistors and the winding resistance of the transformer is 145 ohms. The current limit value is set by circuitry within the S/T transceiver and is approximately 9 mA.

The TxP-T and TxN-T transmit pair supply a current such that a positive potential is created between the TxP-T and TxN-T pins, respectively, when transmitting the F frame bit of each frame. The TxP-T and TxN-T line drive circuit of the MC145576 is designed such that the device will continue to provide a high-impedance circuit to the transmit pair of the S/T loop when power is removed (i.e., when the circuit between $V_{DD}$ and $V_{SS}$ becomes a short circuit). **Figure 10-1** illustrates the recommended line interface and protection circuitry for interfacing the MC145576 to the S/T loop.

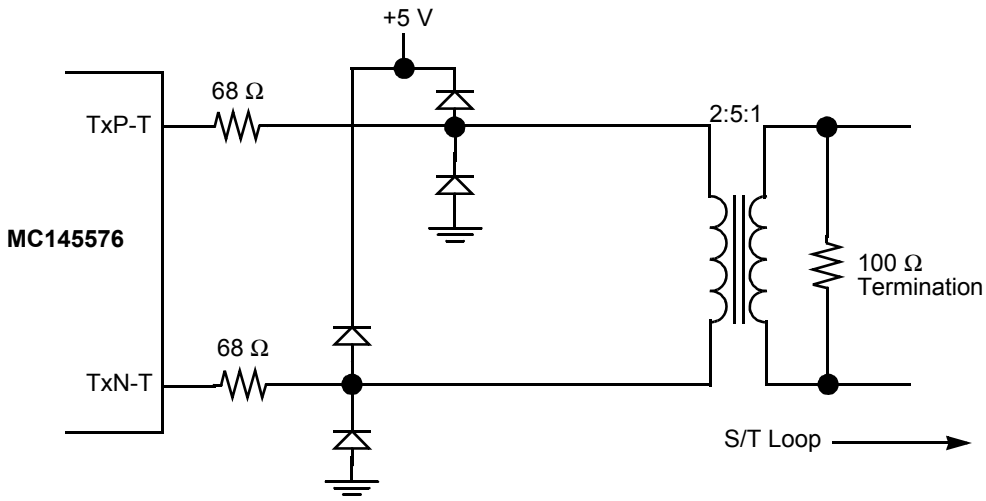



**Figure 10-1.** S/T Transmit Line Interface Circuit

## 10.1.2 S/T Receive Line Interface Circuitry

The RxP-T and RxN-T pins serve as a fully differential input pair for the line signal from the S/T loop. The input impedance seen looking into the combination of the MC145576 and the associated receive line interface circuitry (as shown in **Figure 10-2**) exceeds the CCITT I.430 and ANSI T1.605 requirements under all conditions. The receive line circuitry within the S/T interface is designed to operate with a 1:2.5 turns ratio transformer. The receive transformer is similar in design to the transmit transformer and recommended suppliers of these transformers are included. The receive circuitry within the MC145576 automatically adapts to the optimum ternary detection thresholds for receiving the incoming line signal, regardless of the S/T loop bus configuration. The minimum ternary detection threshold is 90 mV, referenced to signal ground. This value then sets the absolute maximum attenuation that can exist, before detection of the incoming signal becomes impossible. The RxP-T and RxN-T pair is not sensitive to the polarity of their connection to the line interface circuitry. **Figure 10-2** illustrates the recommended line interface and protection circuitry for interfacing the MC145576 S/T interface to the loop.

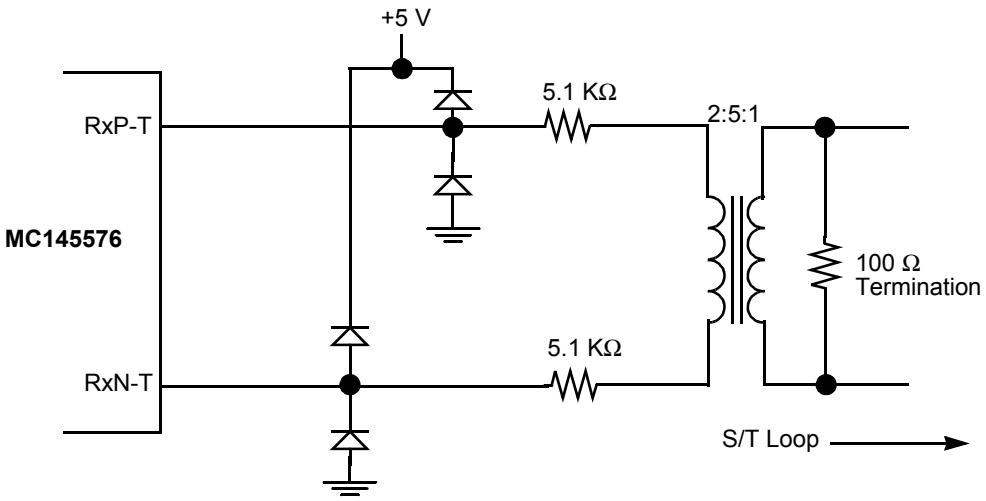



**Figure 10-2.** S/T Receive Line Interface Circuit

**NOTE:** The following descriptions apply to the circuits shown in **Figure 10-1** and **Figure 10-2**.

- Diodes are 1N4148.
- All resistors are 1/4 watt.

#### 10.1.2.1 Termination Resistors

The 100-ohm termination resistors in the transmit and receive Line circuitry as shown in **Figure 10-1** and **Figure 10-2** are mandatory when operating as an NT in accordance with CCITT I.430 and ANSI T1.605.

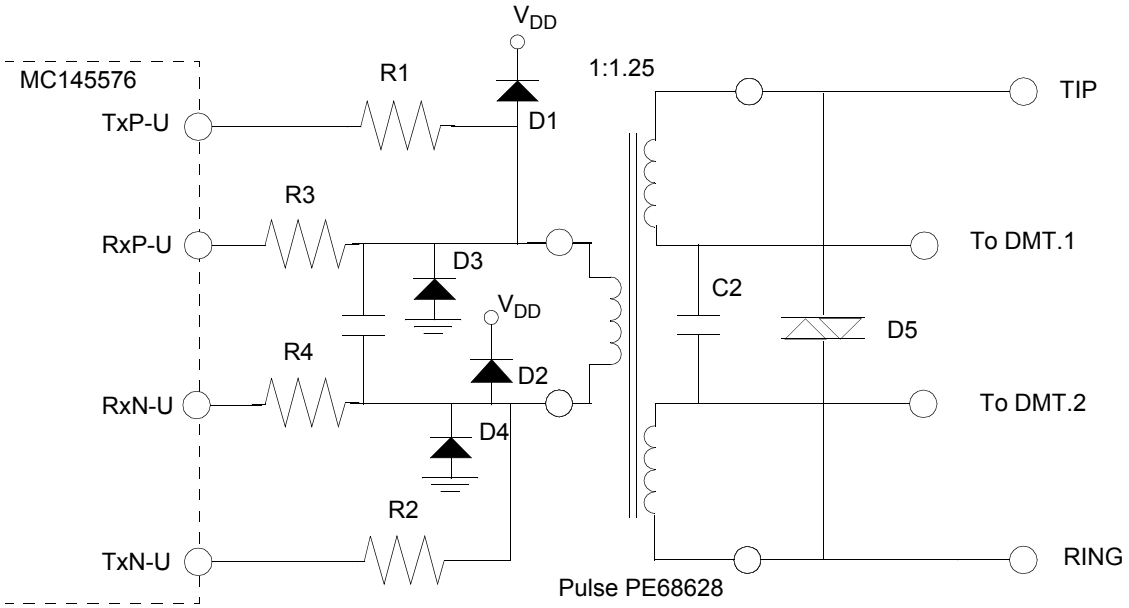
#### 10.1.2.2 Protection Diodes

CCITT I.430 and ANSI T1.605 specify that the S/T interface voltage cannot exceed 1.6 times the nominal voltage of 750 mV (= 1.2 V). Since the MC145576 is designed to operate with 2.5:1 turns ratio transformers, then the diode structure as illustrated in **Figure 10-1** and **Figure 10-2** is required to provide protection, while not adversely affecting the S/T interface when power is removed from the device. This diode structure is also useful in the application to protect the circuit against electrostatic discharges (ESD) and latchup.

## 10.2 U-Interface 2B1Q Line Connection

**Figure 10-3** shows the recommended 2B1Q interface network for U-interface connection. Component specifications are shown in **Table 10-1**. This section contains additional information for selecting and procuring the parts in this circuitry.

**NOTE:** This interface is the same as that used with the MC145572 U Transceiver.




**Notes:** **1.** The Zeners or surge protectors depend on electrical safety requirements.
**2.** DMT = DC Metallic Termination.
**3.** The nearest standart component value for the tolerance given can be used.

**Figure 10-3.** Recommended 2B1Q U Interface Connection

**Table 10-1. 2B1Q Line Interface Components Values**

| Component | Description |
|---|---|
| C1 | 0.015 µF ceramic NPO, COG, polypropylene or polystyrene, low dissipation factor, low dielectric absorption. See **Section D.2.2** for guidelines to calculate this value. |
| C2 | 1.0 µF, 200 V non polarized. |
| R1, R2 | 35 Ω, 1%, metal film or other high quality low distortion resistor. See **Section D.2.1** for guidelines to calculate this value. |
| R3, R4 | 20 Ω, 1% (optional, provide greater surge current protection. |
| D1, D2 | MMBD7000LT1. |
| D3, D4 | IN5232B 5.6 V Zener. |
| D5 | Sidactor, Teccor P1300EA70. |
| T1 | Pulse engineering PE68628. |

The transformer reference schematic is shown in **Figure 10-4**, and the specifications are listed in **Table 10-2**. Any transformer manufactured to this specification must be verified for compliant transmission performance. It is also suggested that transformers manufactured for use in loop powered systems be required to remain within specification up to the maximum loop current which may be as high as 60 mA.

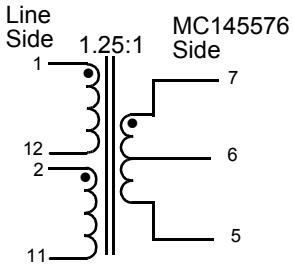



**Figure 10-4.** Schematic Reference for U-Interface Transformer

**Table 10-2. U-Interface Transformer Specifications**

| Parameter | Pins Under Test | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Operating Temperature | — | –40 | +85 | °C | — |
| Breakdown Voltage V ac (t = 1 s) | Each winding to all others and core | 1500 | — | V ac | 1 |
| Surge Voltage per Bellcore TR-NWT-001089 Issue 1, Table 4-2 | Each winding to all others and core | 2500 | — | V dc | 1 |
| DC Insulation Resistance (500 Vdc) | Each winding to all others and core | 500 | — | MΩ | |
| DC Resistance<br>(T = 25° C)<br>(Valhalla 4100) | (1–12)<br>(2–11)<br>(7–5) | 1<br>1<br>1 | 6<br>6<br>9 | Ω | 2 |
| Transformation Ratio (0.1 Vac, 20 kHz)<br>(Waynekerr 3245) | (1–12):(2–11)<br>(1–12:7–5) | 0.99<br>0.615 | 1.01<br>0.635 | — | |
| Inductance at 0.1 V ac, 10 kHz, and 0.0 A dc or 0.08 A dc (Waynekerr 3245) | (1–11) strap (2–12) | 26.5 | 29.5 | mH | 3 |
| Leakage Inductance at 0.01 V ac, 100 kHz | (7–5) strap<br>(1–12) (2–11) | — | 20.0 | µH | |
| Total Harmonic Distortion at 80 mA Winding Current, 4 V pk-pk (Measured Between 500 Hz–100 KHz) | (7–5):(1–11) strap<br>(12–2) | — | –55 | dB | |
| Peak Winding Current | (1–11) strap (2–12) | 20 | — | mA dc | 4 |

**Notes:** **1.** European countries may have significantly higher requirements.
**2.** DC winding resistance should be kept as low as possible since it can change by ± 25% over the temperature range of –40 to +85°C. If the dc winding resistance is low with respect to the value of the series resistors connected between the Tx pins and the transformer, a change in temperature will have a lower effect on the output pulse amplitude than if the transformer dc winding resistance is a relatively high value and the series resistors have a lower value.
**3.** The operating point on B-H curve should be well below the knee (i.e., no saturation).
**4.** Since European ISDN power feeding and pair gain currents are greater, the value should be increased to 60 mA for such applications.

# 11

# Product Specifications

## 11.1 Absolute Maximum Ratings

**Table 11-1.** Absolute Maximum Ratings

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| DC Supply Voltage | $V_{DD}$ | –0.5 to 7.0 | V |
| Voltage, Any Pin to $V_{SS}$ | $V_{in}$ | –0.3 to $V_{DD}$ +0.3 | V |
| DC Current, Any Pin (see Note) | $I_{in}$ | ±10 | mA |
| Operating Temperature | $T_A$ | –20 to +70 | °C |
| Storage Temperature | $T_{stg}$ | –85 to +150 | °C |

**Note:** Except for $V_{DD}$, $V_{SS}$, TxP, and TxN.

## 11.2 Recommended Operating Conditions

**Table 11-2.** Recommended Operating Conditions

| Parameter | Pins | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DC Supply Voltage | $V_{DD}$ | 4.75 | 5.0 | 5.25 | V |
| Voltage Regulator | — | 2.5 | — | 2.8 | V |

## 11.3 Power Consumption

**Table 11-3.** Power Consumption

| MC145576 State | Pins | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Activated **worst case**—Transmit 96 kHz with loopback on S/T Loop and SN2 free running on U loop | | — | -- | 340 | mW |
| Activated—INFO2 on S/T loop, ETSI loop 1 on U loop | | — | 250 | — | mW |
| Activated—INFO4 on S/T loop, ETSI loop 1 on U loop, random data | | — | 245 | — | mW |
| Activated—INFO2 on S/T loop, ETSI loop 2 on U loop | | — | 215 | — | mW |
| Activated—INFO4 on S/T loop, ETSI loop 2 on U loop, random data | | — | 210 | — | mW |
| Deactivated—Sleep Mode | | — | 18 | 22 | mW |

## 11.4 U-Interface Performance

**Table 11-4.** U-Interface Performance

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Cold Start Time, NT Mode | — | 2.3 | 4 | s |
| Warm Start Time, NT Mode | — | 75 | — | ms |
| Transmit Linearity | 45 | 55 | — | dB |
| Differential Receiver Sensitivity | | 50 | 80 | mV |

## 11.5 DC Electrical Characteristics

**Table 11-5.** DC Electrical Characteristics

| Parameter | Test Conditions | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| High-Level Input Voltage, except $\overline{\text{RESET}}$ | | $V_{IH}$ | 2.0 | — | V |
| Low-Level Input Voltage, except $\overline{\text{RESET}}$ | | $V_{IL}$ | –0.3 | 0.8 | V |
| High-Level Input Voltage, $\overline{\text{RESET}}$ | | $V_{IH}$ | 3.75 | — | V |
| Low-Level Input Voltage, $\overline{\text{RESET}}$ | | $V_{IL}$ | — | 1.25 | V |
| High-Level Output Voltage ($I_{OH}$=-400 µA) | | $V_{OH}$ | 2.4 | — | V |
| Low-Level Output Voltage ($I_{OL}$= 5 mA) | | $V_{OL}$ | | .5 | V |
| $\overline{\text{IRQ}}$/DFSC Output Current | $V_{OL}$ = 0.4 V | $I_O$ | — | 8 | mA |
| $\overline{\text{IRQ}}$/DFSC High Impedance/Output Off State | | $R_{off}$ | 100 | — | kΩ |
| Input Capacitance, Digital Pins | | $C_{in}$ | — | 10 | pF |
| Input/High Impedance Leakage Current | $V_{DD}$ = 5.25 V | $I_{in}$ | | 5 | µA |
| $XTAL_{in}$ High-Level Input | | | 3.5 | — | V |
| $XTAL_{in}$ Low-Level Input | | | — | 1.5 | V |
| $XTAL_{out}$ High Output Current | $V_{OH}$ = 2.5 V | $I_{OH}$ | –8 | –1 | mA |
| $XTAL_{out}$ Low Output Current | $V_{OL}$ = 2.5 V | $I_{OL}$ | 1 | 8 | mA |

**Note:** All digital outputs except $XTAL_{out}$ are tri-stateable regardless of their normal operating conditions.

## 11.6 2B1Q Interface Electrical Characteristics

**Table 11-6. Pins TxP and TxN** ($R_L$ = 60 Ω from TxP to TxN)

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Output Resistance—Full Power Mode | — | — | 0.05 | Ω |
| Output Resistance—Power Down Mode | — | 10 | 30 | Ω |
| Output Resistance—Absolute Power Down Mode | — | 10 | 30 | Ω |
| Output Peak Voltage from TxP to TxN | — | + 4.0 | — | $V_{pk}$ –$V_{pk}$ |
| Output Load Capacitance | — | — | 47 | nF |

**Table 11-7.** Pins RxP and RxN

| Parameter | Min | Max | Unit |
|---|---|---|---|
| Input Resistance—Full Power Mode | 1 | — | MΩ |
| Input Resistance—Power Down Mode | 1 | — | MΩ |
| Input Resistance—Absolute Power Down Mode | 1 | — | MΩ |
| Input Voltage Range for RxP or RxN | $((V_{DD} - V_{SS})/2) - 0.5$ | $((V_{DD} - V_{SS})/2) + 0.5$ | V |

## 11.7 S/T-Interface Analog Characteristics

**Table 11-8.** S/T-Interface Analog Characteristics

| Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|
| TxP/TxN Drive Current—$R_L$ = 50 Ω | 5.4 | 6.0 | 6.6 | mA |
| (TxP – TxN) Voltage Limit on the S/T Loop side | — | — | 1.17 | Vpeak |
| Rx Input Sensitivity, Normal Mode (RxP – RxN) | 90 | — | — | mVpeak |
| Rx Input Sensitivity, Sleep Mode (RxP – RxN) | 220 | — | — | mVpeak |

## 11.8 IDL Timing Characteristics

**Table 11-9.** IDL Timing Characteristics

| Ref. No. | Parameter | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| 1 | FSC Period | 125 | 125 | — | µs | 1 |
| 2 | Delay From the Rising Edge of DCL to the Rising Edge of FSC | — | | 30 | ns | |
| 3 | Delay From the Rising Edge of DCL to the Falling Edge of FSC | — | | 30 | ns | |
| 4 | DCL Clock Period | 488 | | 1953 | ns | 2 |
| 5 | DCL Pulse Width High, Nominal 512 kHz<br>2.048 MHz<br>DCL Clock 249 Pulse Width High 2.048 MHz<br>DCL Clock 59 Pulse Width High 512 kHz | 878<br>210<br>160<br>825 | | 1074<br>265<br>315<br>1120 | ns | 3 |
| 6 | DCL Pulse Width Low | 45 | | 55 | % of DCL Period | 4 |
| 7 | Delay From Rising Edge of DCL to Low-Z and Valid Data on $D_{out}$ | — | | 30 | ns | |
| 8 | Delay From Rising Edge of DCL to Data Valid on $D_{out}$ | 5 | | 30 | ns | |
| 9 | Delay From Rising Edge of DCL to Hi-Z on $D_{out}$ | — | | 30 | ns | |
| 10 | Data Valid on $D_{in}$ Before Falling Edge of DCL ($D_{in}$ Setup Time) | 25 | | — | ns | |
| 11 | Data Valid on $D_{in}$ After Falling Edge of DCL ($D_{in}$ Hold Time) | 25 | | — | ns | |

**Notes:**
1. FSC occurs on average every 125 µs.
2. The DCL Frequency may be 512 kHz or 2.048 MHz.
3. The duty cycle of DCL is between 45% and 55% when operated in master timing mode. This duty cycle is guaranteed for all DCL clocks except the clock that is used for making timing adjustments in order to maintain synchronization with the received signal when operating in NT mode. In NT master mode the MC145576 conveys timing adjustments over the DCL clock of the device. This is done by adding or subtracting a single 20.48 MHz clock period of 48 ns to the high phase of DCL clock on two successive IDL frames once per U-Interface basic frame. The total adjustment is 96 ns distributed over the two IDL frames. When DCL is configured for 2.048 MHz the adjustment occurs during clock pulse number 249 after FSC. The count starts at clock pulse 0 for the DCL clock immediately following FSC. When DCL is configured for 512 kHz the adjustment occurs during DCL pulse number 59. It is important to remember this when using the timeslot assigner since it is possible to program it to transfer 2B or D data during the clock period where the timing adjustment is being made and this may effect setup and hold times for other components in a system.
4. The pulse width during the low phase of the clock varies between 45% and 55% of the nominal frequency. Timing adjustments are not made during the low phase of DCL.

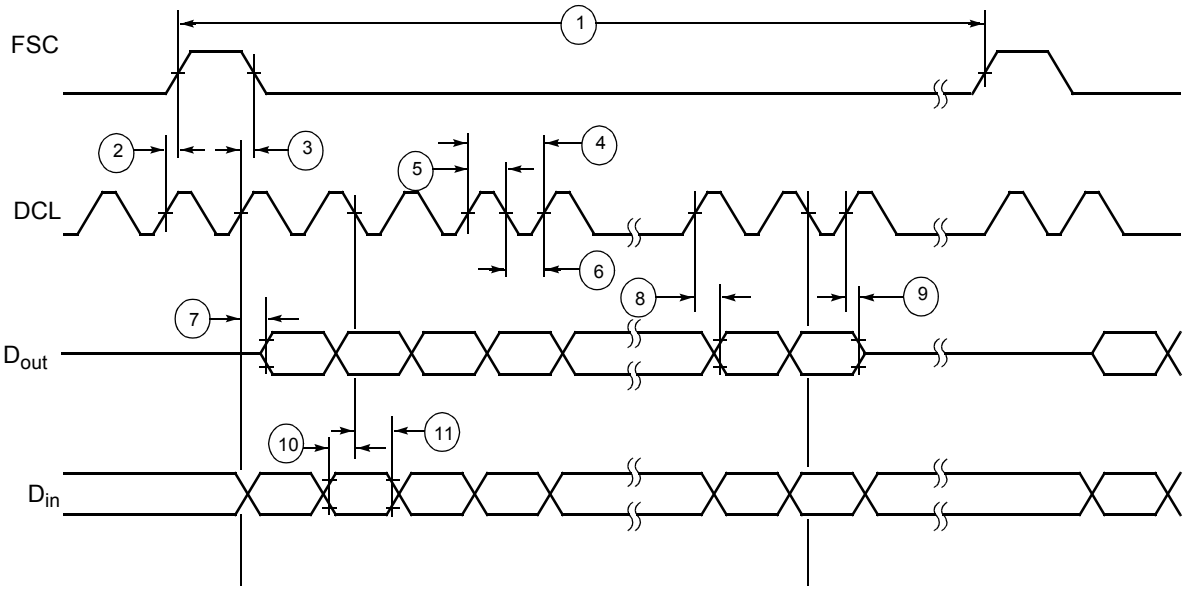



**Figure 11-1.** IDL Timing, 8/10-Bit Formats

## 11.9 GCI Timing Characteristics

**Table 11-10.** GCI Timing Characteristics

| Ref. No. | Parameter | | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| 20 | Delay From Rising Edge of DCL to FSC Output High | | — | | 30 | ns | |
| 21 | Delay From Rising Edge of DCL to FSC Output Low (Normal Frame) | | — | | 30 | ns | 1 |
| 22 | Delay From Rising Edge of DCL to FSC Output Low (Superframe Marker) | | — | | 30 | ns | 2 |
| 23 | DCL Clock Period | | 488 | | 1953 | ns | 3 |
| 24 | DCL Pulse Width High<br><br>DCL Clock 249 Pulse Width High<br>DCL Clock 59 Pulse Width High | 512 kHz<br>2.048 kHz<br>2.048 MHz<br>512 kHz | 878<br>210<br>160<br>825 | | 1074<br>265<br>315<br>1120 | ns | 4 |
| 25 | DCL Pulse Width Low | | 45 | | 55 | % of DCL Period | |
| 26 | DCL Fall Time | | 5 | | 15 | ns | |
| 27 | DCL Rise Time | | 5 | | 15 | ns | |
| 28 | Delay From Rising Edge of FSC to Low-Z and Valid Data on $D_{out}$ | | — | | 40 | ns | |
| 29 | Delay From Rising Edge of DCL to Data Valid on $D_{out}$ | | — | | 35 | ns | |
| 30 | Delay From Rising Edge of DCL Hi-Z on $D_{out}$ | | 5 | | 35 | ns | |
| 31 | Data Valid on $D_{in}$ Before Rising Edge of DCL | | 25 | | — | ns | |
| 32 | Data Valid on $D_{in}$ After Rising Edge of DCL | | 25 | | — | ns | |

**Notes:**
1. The FSC pulse is normally 2 DCL clock periods wide.
2. The FSC pulse is only one DCL clock period wide at the start of a superframe. Every 96th FSC pulse marks the start of a superframe.
3. The DCL frequency may be 512 kHz or 2.048 MHz.
4. The duty cycle of DCL is between 45% and 55% when operated in master timing mode. This duty cycle is guaranteed for all DCL clocks except the clock that is used for making timing adjustments in order to maintain synchronization with the received signal when operating in NT mode. In NT master mode the MC145576 conveys timing adjustments over the DCL clock of the device. This is done by adding or subtracting a single 20.48 MHz clock period of 48 ns to the high phase of DCL clock on two successive GCI frames once per U-Interface basic frame. The total adjustment is 96 ns distributed over the two frames. When DCL is configured for 2.048 MHz the adjustment occurs during clock pulse number 249 after FSC. The count starts at clock pulse 0 for the DCL clock immediately coincident with FSC being driven high. When DCL is configured for 512 kHz the adjustment occurs during DCL pulse number 59. It is important to remember this when programming the GCI timeslot since it is possible for data to be transferred during the clock period where the timing adjustment is being made and this may effect setup and hold times for other components in a system.

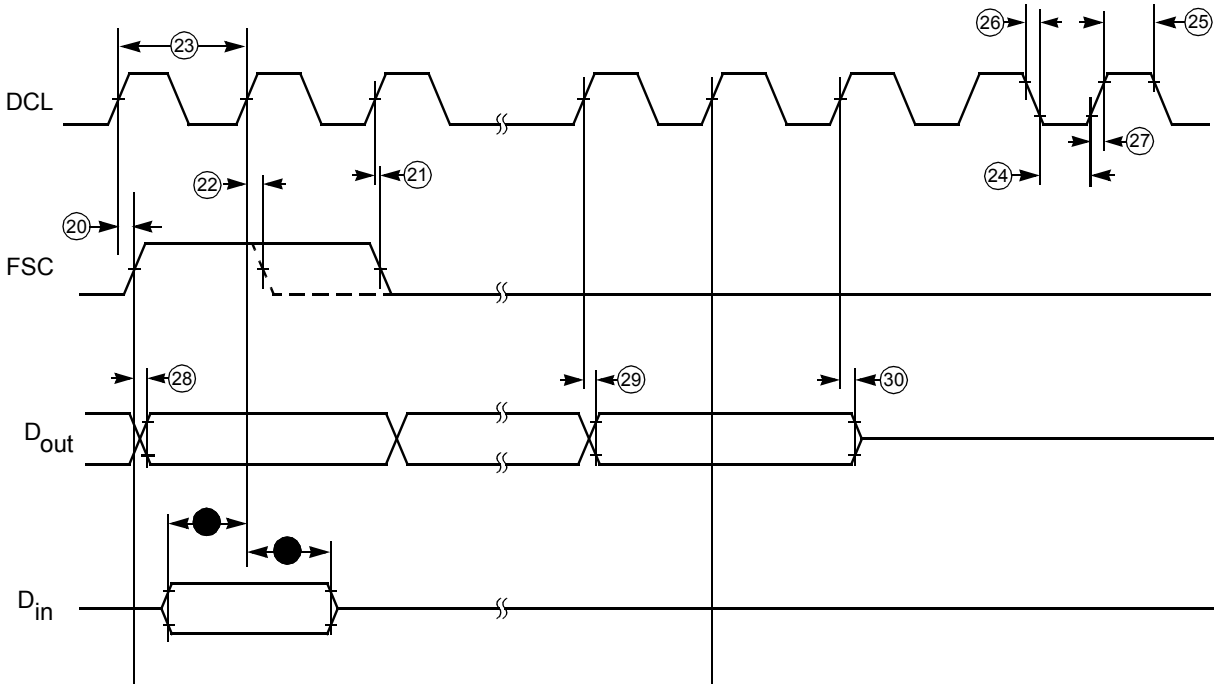



**Figure 11-2. GCI Master Timing**

## 11.10 SCP Timing Characteristics

**Table 11-11.** SCP Timing Characteristics

| Ref. No. | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| 40 | SCPCLK Rising Edge Before SCPEN(L)_T and SCPEN(L)_U Falling Edge | 40 | — | ns |
| 41 | $\overline{\text{SCPEN}}$ Falling Edge Before SCPCLK Rising Edge | 40 | — | ns |
| 42 | SCP Rx Data Valid Before SCPCLK Rising Edge (Setup Time) | 20 | — | ns |
| 43 | SCP Rx Data Valid After Rising Edge of SCPCLK (Hold Time) | 20 | — | ns |
| 44 | SCPCLK Frequency | — | 4.1 | MHz |
| 45 | SCPCLK Width Low | 50 | — | ns |
| 46 | SCPCLK Width High | 50 | — | ns |
| 47 | SCPCLK Rising Edge Before SCPEN(L_T and SCPEN(L)_U) Rising Edge[2] | 40 | — | ns |
| 48 | $\overline{\text{SCPEN}}$ Rising Before SCP CLK Rising Edge[2] | 40 | — | ns |
| 49 | SCPCLK Falling Edge to SCP Tx low impedance | — | 40 | ns |
| 50 | SCPCLK Falling Edge (While SCP EN(L) is Low) to SCP Tx Data Valid | — | 40 | ns |
| 51 | $\overline{\text{SCPEN}}$ Rising Edge to SCP Tx high impedance | — | 30 | ns |
| 52 | $\overline{\text{SCPEN}}$ Falling Edge to SCP Tx Active (Byte Mode) | 0 | 40 | ns |

**Notes:** **1.** Measurements are made from the point at which they achieve their guaranteed minimum or maximum logic levels.

**2.** $\overline{\text{SCPEN}}$ must rise between the rising edge of the eighth SCPCLK and the rising edge of the ninth SCPCLK for an 8-bit access or the access will be ignored. For a 16-bit access, $\overline{\text{SCPEN}}$ must rise between the rising edge of the sixteenth SCPCLK and the rising edge of the seventeenth SCPCLK or the access will be ignored.

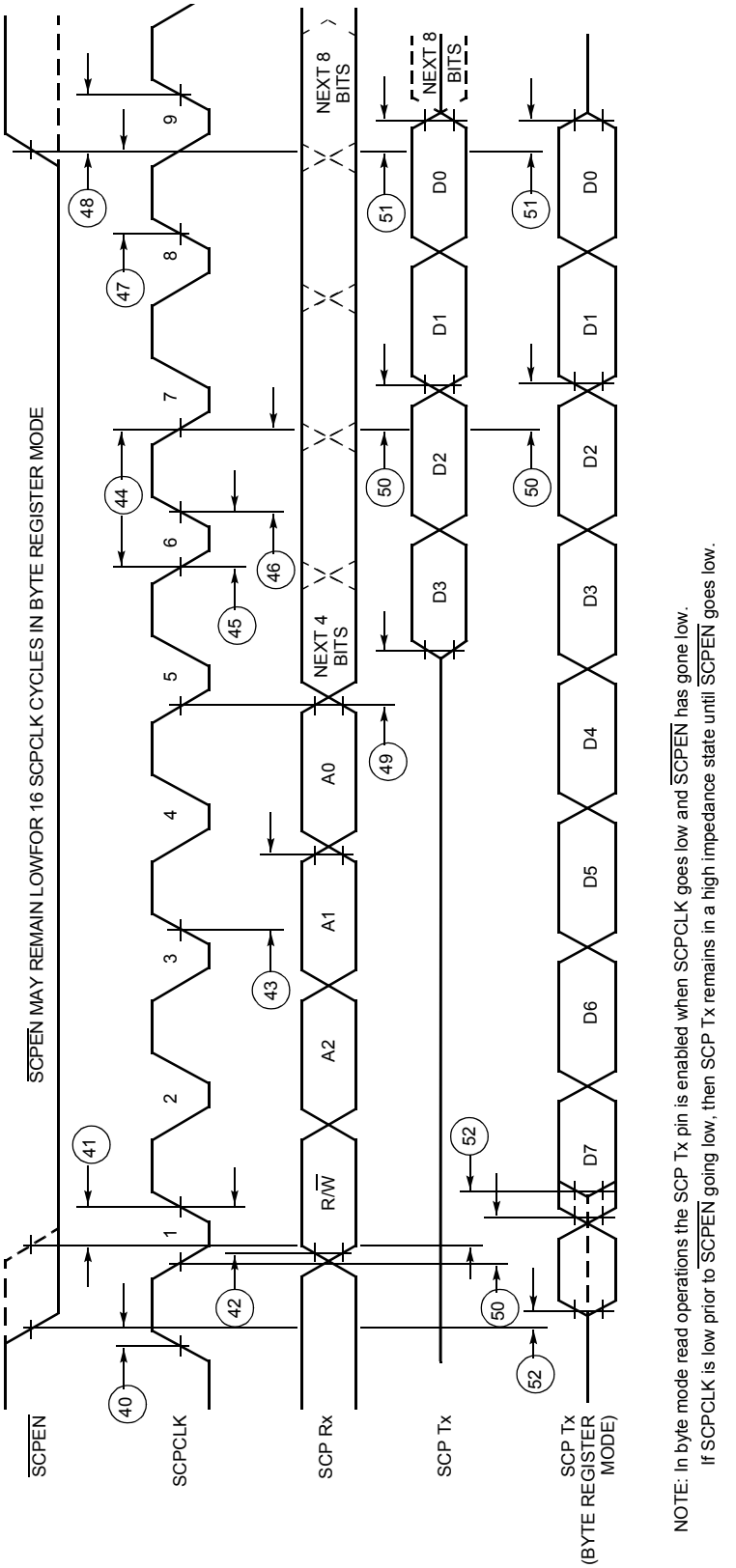



**Figure 11-3.** Serial Control Port (SCP) Interface Timing

## 11.11 D Channel Timing Characteristics (IDL Mode)

**Table 11-12.** D Channel Timing Characteristics

| Reference Number | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| 60 | DREQUEST Valid Before Falling Edge of FSC | 30 | | ns |
| 61 | DREQUEST Valid After Falling Edge of FSC | 30 | | ns |
| 62 | DGRANT Valid Before Falling Edge of FSC | 50 | | µs |

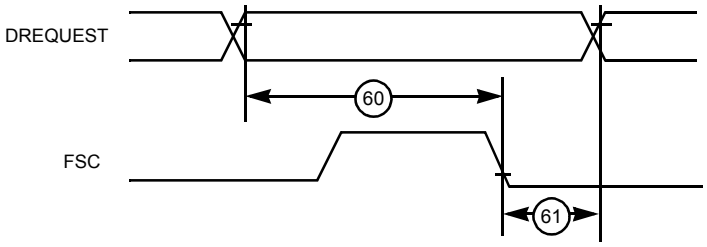



**Figure 11-4.** DREQUEST Timing

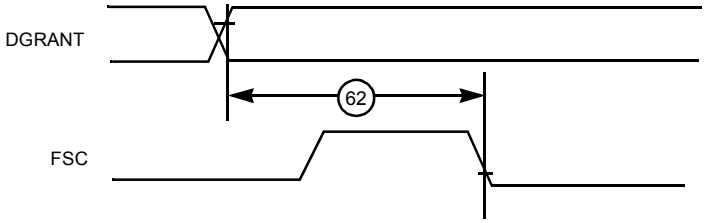



**Figure 11-5.** DGRANT Timing

# 12

# Mechanical Data

## 12.1 Pin Assignments

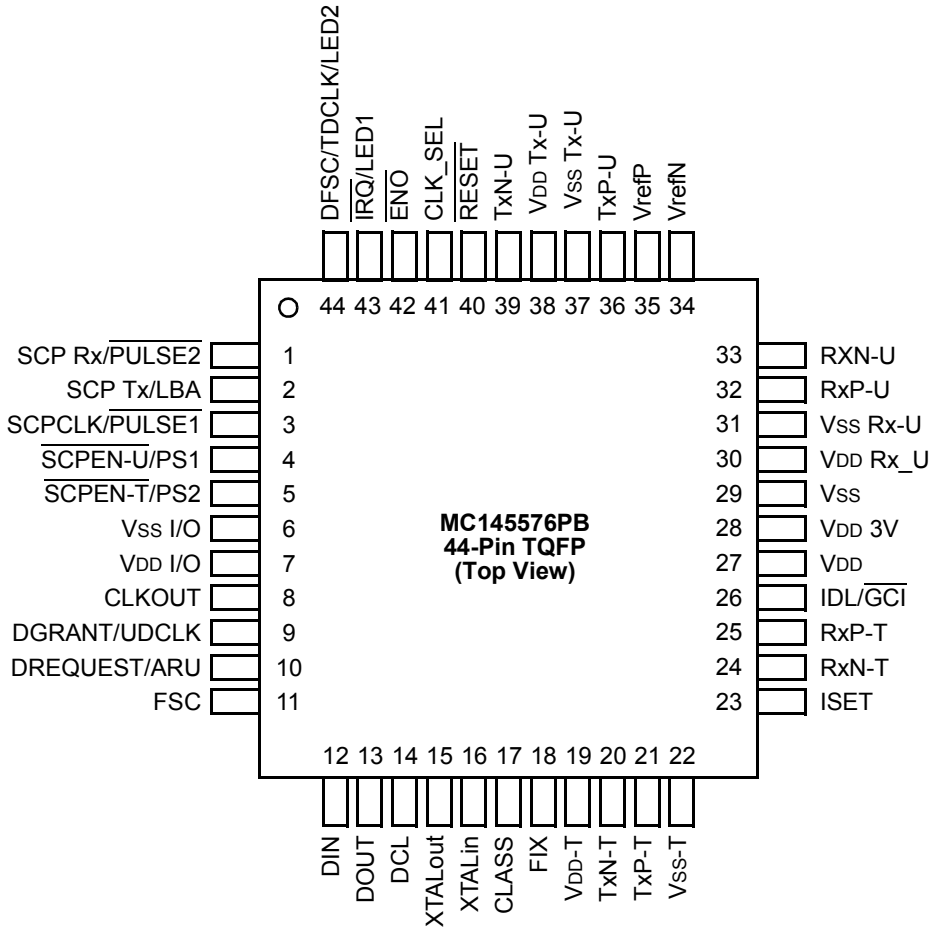
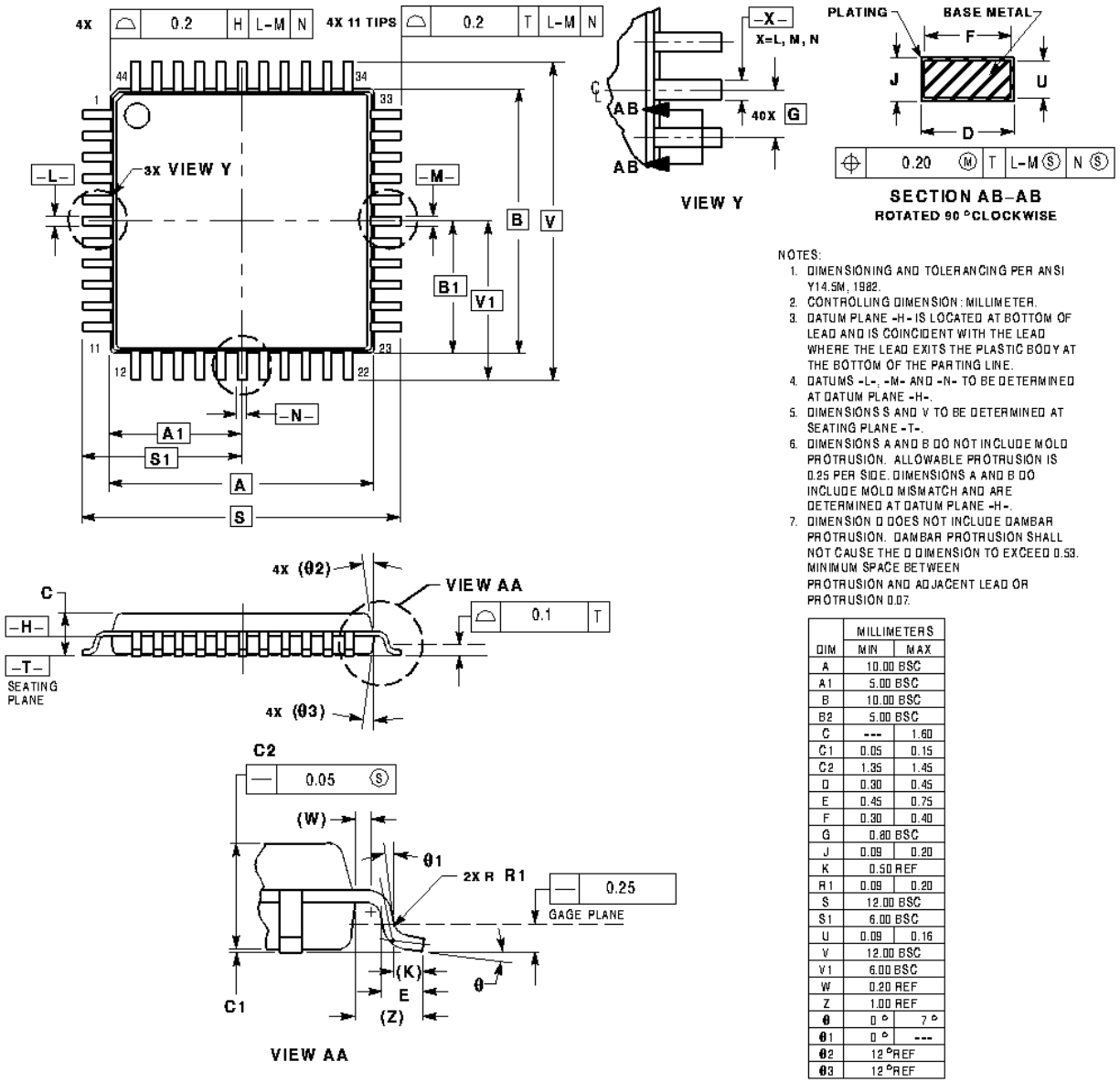



**Figure 12-1.** MC145576 Pinout Drawing

revised 8/28/1998

## 12.2 Package Description




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -L-, -M- AND -N- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -T-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.53. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 10.00 BSC | |
| A1 | 5.00 BSC | |
| B | 10.00 BSC | |
| B2 | 5.00 BSC | |
| C | --- | 1.60 |
| C1 | 0.05 | 0.15 |
| C2 | 1.35 | 1.45 |
| D | 0.30 | 0.45 |
| E | 0.45 | 0.75 |
| F | 0.30 | 0.40 |
| G | 0.80 BSC | |
| J | 0.09 | 0.20 |
| K | 0.50 REF | |
| R1 | 0.09 | 0.20 |
| S | 12.00 BSC | |
| S1 | 6.00 BSC | |
| U | 0.09 | 0.16 |
| V | 12.00 BSC | |
| V1 | 6.00 BSC | |
| W | 0.20 REF | |
| Z | 1.00 REF | |
| θ | 0° | 7° |
| θ1 | 0° | --- |
| θ2 | 12° REF | |
| θ3 | 12° REF | |

**CASE 824D-02**
**ISSUE A**

**DATE 08/09/95**

**Figure 12-2.** MC145576 44-pin TQFP Package Drawing

# A

# MC145576 Evaluation Board

## A.1 Introduction

The MC145576EVK board provides Motorola ISDN customers a convenient and efficient vehicle for evaluation of the MC145576 ISDN Single Chip NT1.

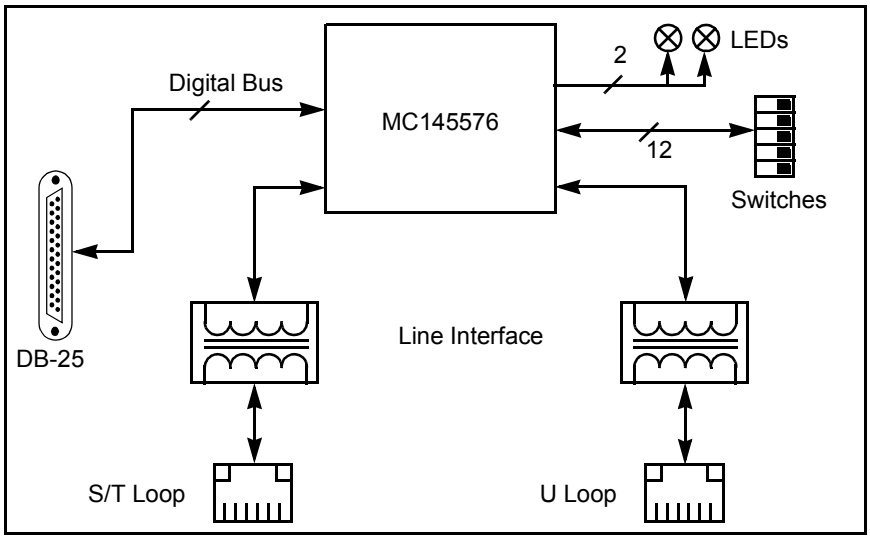



**Figure A-1.** MC145576EVK Block Diagram

## A.2 MC145576EVK in NT1 Mode

NT1 Mode is the default configuration of the MC145576EVK board. The board acts as a complete NT1 (U and S/T loops connectors, indication LEDs, test modes, PS1 and PS2 control) but without the power recovering functions. Since this is an evaluation board and not a reference design, the MC145576EVK is powered by an external 5V power supply. There is no power feeding circuitry that recovers the power from the U line. Another connector can be used to provide +40V power supply down to the TE through the S/T line (+40V and +5V power supplies have separated grounds).

## A.3 MC145576EVK in Smart NT1 Mode

The MC145576EVK can be configured to provide a terminal access to the MC145576, which is required for the SMART NT1 applications. The terminal access can be IDL/SCP or GCI. The digital bus (IDL/SCP or GCI) as well as several other control signals are routed to a DB25 connector. There is no processor on the board to control the MC145576, but Motorola has designed a board (based on the HC11 and a FPGA) and PC-based software that can be directly connected to the MC145576EVK board. This MC145576DRV board, which works only in IDL/SCP mode, provides quick access to the internal registers, gated clocks, and the Smart NT1 activation/deactivation state machine.

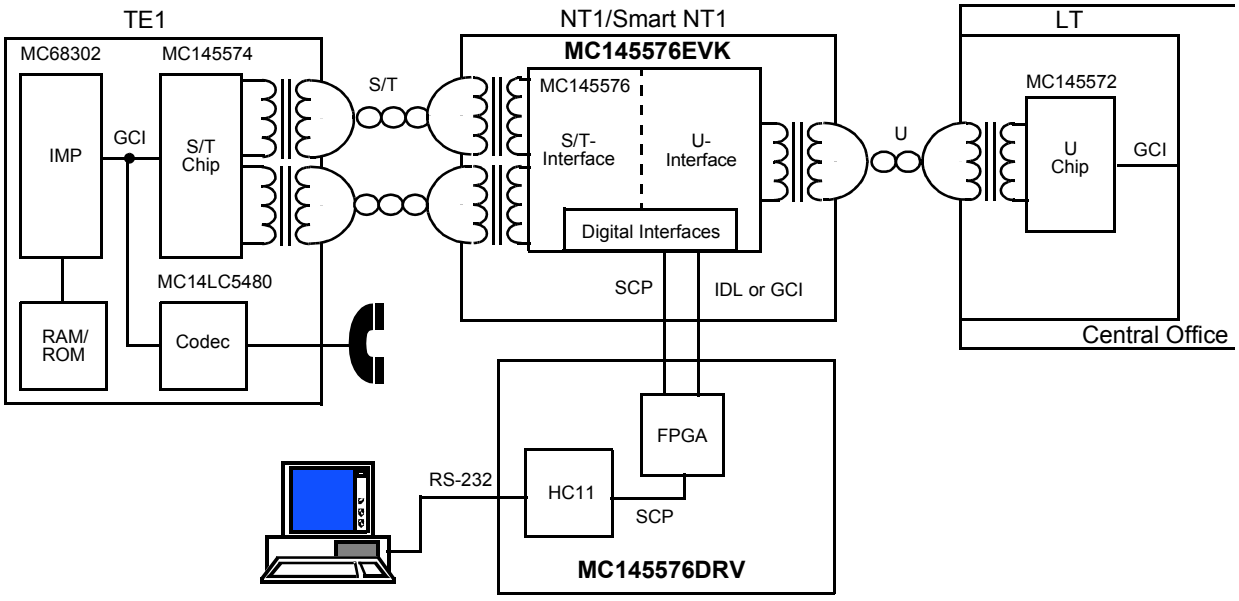



**Figure A-2.** Smart NT1 Configuration with MC145576EVK and MC145576DRV

## A.4 MC145576DRV Features

- PC-based operation
- Resident firmware monitor for user control of board
- Smart NT1 activation and deactivation software
- MC68HC11 Assembly language source code available
- On-board 68HC11 Microcontroller with resident monitor software
- Convenient access to key signals
- Requires only a +5 V power supply (the MC145576EVK supplies board power)
- Gated data clocks provided for bit error rate testing
- Can be used as a MC145576 development tool
- RS-232 (V.28) serial port for terminal interface

# B

# Component Sourcing

## B.1 Overview

The MC145576 integrates features of the MC145572 ISDN U-Interface Transceiver and the MC145574 ISDN S/T-Interface Transceiver in a single chip. This section discusses the requirements for each of these interfaces. The following information is provided to assist in sourcing the various parts used in the application of the MC145576 transceivers. The detailed specifications for these parts are available from the manufacturer and information presented here is only as current as the printing of this document. Contact your local Motorola representative or the Motorola factory applications staff for the latest updates on this information.

**NOTE:** Motorola has conducted limited evaluation of third party components for use with the MC145576. This limited review suggests that the components included here appear to be suitable for applications using the MC145576. However, the evaluation did not include all specifications or parameters that may be applicable to particular designs, and the vendors included here represent only a partial list of component manufacturers. Motorola does not guarantee that these third party components will work in all applications. It is the responsibility of the equipment designer to verify that these components are suitable for their intended application.

## B.2 MC145576 Transformers Third Party Sources

**Table B-1** lists manufacturers of line interface transformers for use with the MC145576.

**Table B-1 MC145576 Line Interface Circuit Transformer Manufacturers**

| Manufacturer | U Transformer | S/T Transformer | Internet Contact Address |
|---|---|---|---|
| APC | X | X | www.apcisdn.com |
| Midcom | X | X | www.midcom-inc.com |
| Pulse Engineering | X | X | www.pulseeng.com |
| Schott Corporation | | | www.schottcorp.com |
| Secre | X | X | ourworld.compuserve.com/ homepages/secre_comp |
| TDK | | | www.tdk.com |
| Universal | X | X | www.umec-europe.com |
| VAC | X | X | www.vacuumschmelze.de |

**NOTE:** Motorola can not recommend one manufacturer over another and in no way implies that this is a complete list.

### B.2.1 Crystal Specification

The MC145576 requires a pullable crystal because it has an on-chip VCXO. The specification assumes network timing tolerance of ± 5 ppm. The total pullability is 250 ppm.

**Table B-2 Crystal Specifications**

| Characteristic | Specified Value |
|---|---|
| Operating Frequency | 20.48 MHz |
| Crystal Shunt Capacitance | $C_0$ = 7.0 pF |
| Uncertainty at rated $C_L$ | ± 50 ppm over temperature, calibration, and 10-year aging[1,2] |
| Equivalent series resistance | $R_S \leq 20$ ohms @ 1 mW drive |
| Pull range | 250 ppm minimum pullability over a $C_L$ range of 15 to 45 pF |
| Package | QC49 |
| Calibration Load Capacitance | 24 pF |

**Notes:** **1.** –40 to +85ºC required for transmission applications.
**2.** For general terminal adapter applications, use 0–70ºC.

**Table B-3 Crystal Vendors**

| Manufacturer | Internet Contact Address |
|---|---|
| Connor-Winfield | conwin.com |
| ECLIPTEK | www.ecliptek.com |
| Hy-Q International | www.hy-q.co.uk |
| IQD | www.iqdcrystals.com |
| KONY | www.kony.co.kr |
| LPE/Telequarz | www.telequarz.de |
| Manudax | www.manudax.fr |
| Precision Devices | www.pdixtal.com |
| SaRonix | www.saronix.com |
| Telecona | www.telecona.com |

## B.2.2 ISDN Call Control Source Code

The following vendors provide ISDN call control and applications source code. These suppliers support most of the various national and regional ISDN call control specifications on a world-wide basis. This list may not be complete.

**Table B-4 ISDN Call Control Source Code Suppliers**

| Manufacturer | Street Address | Internet Contact Address |
|---|---|---|
| Link Technology | 23 Crescent Drive<br>Holland, PA 18966<br>email: linkisdn@interramp.com | www.linktechnology.com |
| OMNITEL | 31 rue Jean Rostand<br>91893 ORSAY CEDEX France | www.omnitel.com |
| OMNITEL | 3880 S. Bascom Ave., Suite 116<br>San Jose, CA 95124 U.S.A.<br>email: 102766.2525@compuserve.com | www.omnitel.com |
| telenetworks | 625 Second Street<br>Petaluma, CA 94952 U.S.A.<br>e-mail: info@tn.com | www.telenetworks.com |
| TeleSoft International, Inc. | 4029 S. Capital of Texas Hwy., Suite 220<br>Austin, TX 78704 U.S.A.<br>e-mail: sales@telesoft-intl.com | www.telesoft-intl.com |
| Trillium Digital Systems, Inc. | 2001 S. Barrington Ave.,<br>Suite 215<br>Los Angeles, CA 90025 U.S.A. | www.trillium.com |

# C

# Printed Circuit Board Layout

## C.1 Overview

The MC145576 is manufactured using high speed CMOS VLSI process technology to implement the mixed signal processing functions required in the device. The U-interface of the MC145576 has a high resolution Σ-Δ ADC and a precision DAC, in addition to three high speed digital signal coprocessors. The fully differential analog circuit design techniques used for this device result in superior performance for the ADC, DAC, and Tx Driver sections. Special attention was given to the design of the MC145576 to reduce sensitivity to noise, including power supply rejection and susceptibility to radio frequency noise. This special attention to circuit design, results in an ADC with greater than 84 dB dynamic range on the same monolithic chip as the digital signal coprocessors clocking at 10.24 MHz, all of which operates on a single 5 V power supply. This device was designed to ease the task of PCB layout, but due to the wide analog dynamic range and high digital clock rate, special care should be taken during PCB layout to assure optimum transmission performance.

**NOTE:** When laying out the PCB, do not run any digital signals through the line interface region of the board. Switching noise from the digital signals can be coupled into the line interface and reduce performance, especially on long loops. Wire wrap is not recommended for prototyping.

## C.2 Printed Circuit Board Mounting

The device should be soldered to the PC board for production manufacturing. If the device is to be used in a socket, it should be placed in a low parasitic pin capacitance socket of 1.5 pF or less.

## C.3 Power, Ground, and Noise Considerations

The most important considerations for PCB layout deal with noise. This includes noise on the power supply, noise generated by the digital circuitry on the device, and coupling digital signals into the analog signals. The best PCB layout methods to prevent noise-induced problems are:

- Keep digital signals as far away from analog signals as possible.
- Use short, low inductance traces for the analog circuitry to reduce inductive, capacitive, and radio frequency noise sensitivities.
- Use short, low inductance traces for digital circuitry to reduce inductive, capacitive, and radio frequency radiated noise.
- Bypass capacitors should be connected between the $V_{DD}$ and $V_{SS}$ pairs with minimal trace length. These capacitors help supply the instantaneous currents of the digital circuitry, in addition to decoupling the noise that may be generated by other sections of the device or other circuitry on the power supply.
- Use short, wide, low inductance traces to connect all of the $V_{SS}$ ground pins together and, with one trace, connect all of the $V_{SS}$ ground pins to the power supply ground. Depending on the application, a double sided PCB with a $V_{SS}$ ground plane under the device connecting all of the digital and analog $V_{SS}$ pins together would be a good grounding method. A multi-layer PCB with a ground plane connecting all of the digital and analog $V_{SS}$ pins together would be the optimal ground configuration. These methods will result in the lowest resistance and the lowest inductance in the ground circuit. This is important to reduce voltage spikes in the ground circuit resulting from the high speed digital current spikes. Suppressing these voltage spikes on the integrated circuit is the reason for multiple $V_{SS}$ ground leads.
- Use short, wide, low inductance traces to connect all of the $V_{DD}$ power supply pins together and, with one trace, connect all of the $V_{DD}$ power supply pins to the 5-V power supply. Depending on the application, a double sided PCB with $V_{DD}$ bypass capacitors to the $V_{SS}$ ground plane under the device, as described in item 5 above, may complete the low impedance coupling for the power supply. For a multi-layer PCB with a power plane, connecting all of the digital and analog $V_{DD}$ pins to the power plane would be the optimal power distribution method. The integrated circuit layout and packaging considerations for the 5-V $V_{DD}$ power circuit are essentially the same as for the ground circuit.
- Motorola recommends that a four layer board be used. It is possible to use a two layer board but special care must be taken.
- The 20.48 MHz crystal must be located as close as possible to the MC145576 package. This is required to minimize parasitic capacitances between crystal traces and ground.

## C.4 Oscillator Layout Guidelines

All traces must be as short as possible to reduce stray capacitance and inductance. The traces to $XTAL_{in}$ and $XTAL_{out}$ must be kept as short as possible with minimal width to keep stray capacitance less than 1 pF. Other digital signals should not be routed near the crystal traces. Any passive components for the oscillator or PLL should have short leads and should be soldered to the PC board. Wherever possible the layout should be symmetrical, so the stray capacitances from each pin of the crystal to ground are equal.

## C.5 2B1Q Interface Guidelines

The line interface into and out of the device is differential, implying symmetry. It is recommended that the layout of the 2B1Q interface be as symmetrical as possible to avoid any imbalances to this circuit. Do not run any digital traces through the line interface region of the printed circuit board.

# D

# Line Interface Circuit Component Value Calculations

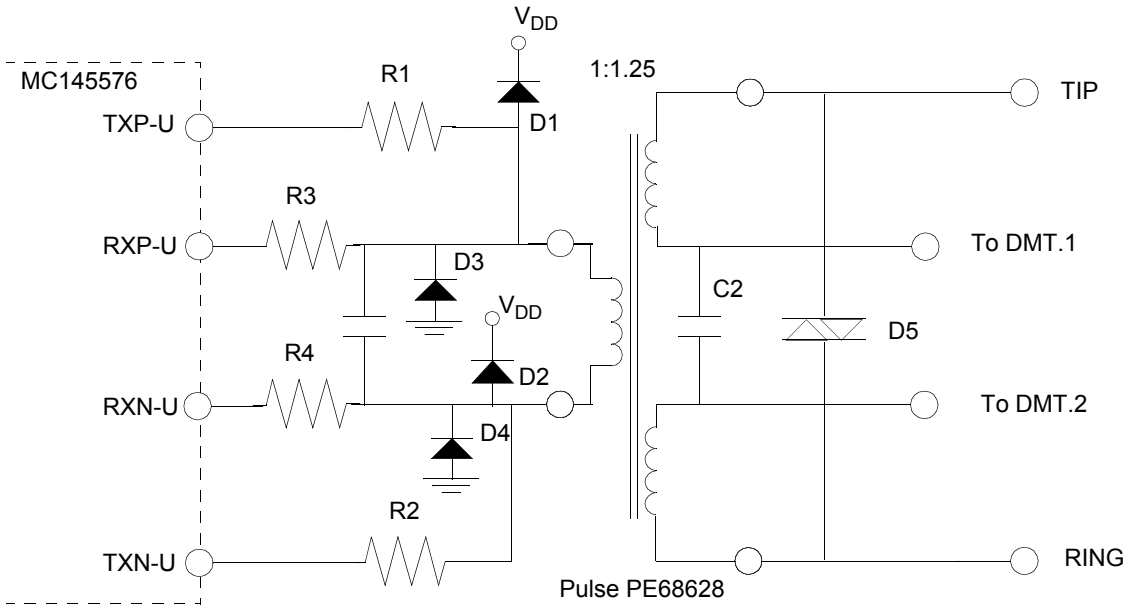
## D.1 Overview

This appendix provides information abtou the MC145576 2B1Q Inteface Circuit (excluding protection, dc termination, etc.) to compute optimal component values for line interface and transformer solutions. It also provides some basic information regarding the function of each of the components in the 2B1Q Interface Circuit.

## D.2 U-Interface 2B1Q Line Connection

**Figure D-1** shows the recommended 2B1Q interface network for U-interface connection. Component specifications are shown in **Table D-1**. This section contains additional information for selecting the parts in this circuitry.

**NOTE:** This interface is the same as that used with the MC145572 U Transceiver.




**Notes:** 1. The Zeners or surge protectors depend on electrical safety requirements.
2. DMT = DC Metallic Termination.
3. The nearest standart component value for the tolerance given can be used.

**Figure D-1.** Recommended 2B1Q U Interface Connection

**Table D-1. 2B1Q Line Interface Components Values**

| Component | Description |
|---|---|
| C1 | 0.015 µF ceramic NPO, COG, polypropylene or polystyrene, low dissipation factor, low dielectric absorption. See **Section D.2.2** for guidelines to calculate this value. |
| C2 | 1.0 µF, 200 V non polarized. |
| R1, R2 | 35 Ω, 1%, metal film or other high quality low distortion resistor. See **Section D.2.1** for guidelines to calculate this value. |
| R3, R4 | 20 Ω, 1% (optional, provide greater surge current protection. |
| D1, D2 | MMBD7000LT1. |
| D3, D4 | IN5232B 5.6 V Zener. |
| D5 | Sidactor, Teccor P1300EA70. |
| T1 | Pulse engineering PE68628. |

## D.2.1 Transmit Series Resistors

For the purpose of determining the required values for the transmit series resistors, a line interface circuit model, shown in **Figure D-2**, is used. The required values for transmit series resistors ($R_x$), depend on the amount of dc winding resistance of the transformer. The values of these resistors also depend on the impedance of the 1 µF dc blocking capacitor, Cb. Any resistors added to the line side of the transformer for primary circuit protection may be added to the dc winding resistance of the line side windings of the transformer. Portions of the line interface circuit are internal to the MC145576.

The total transmit circuit model is shown in **Figure D-3**. Due to the duplexer nature of the line interface circuit, $R_{xP}$ and $R_{xN}$ are at virtual signal ground for transmitted signals. Thus, each Rf appears in parallel with each Rg (see **Figure D-3**), but since Rg is so low, Rf can be ignored. The output impedance of the transmit drivers has been included in this model, but will be subsequently ignored due to its insignificant nature.

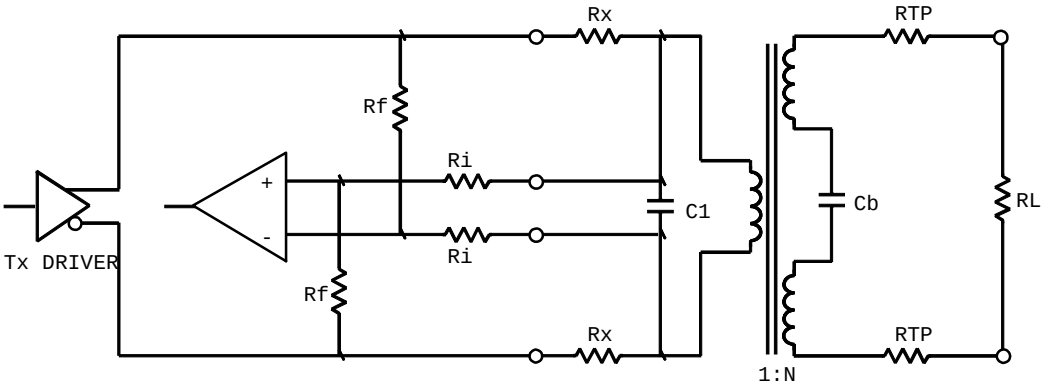



**Figure D-2.** Line Interface Circuit Model

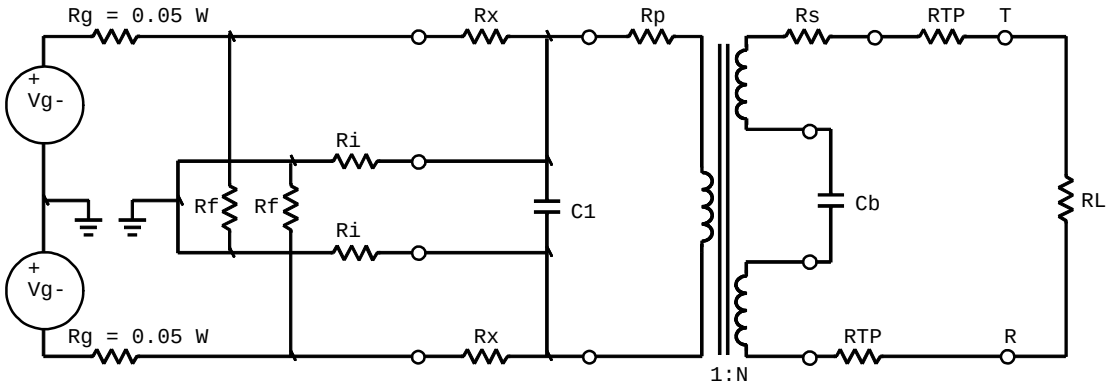



**Figure D-3.** Transmit Circuit Model

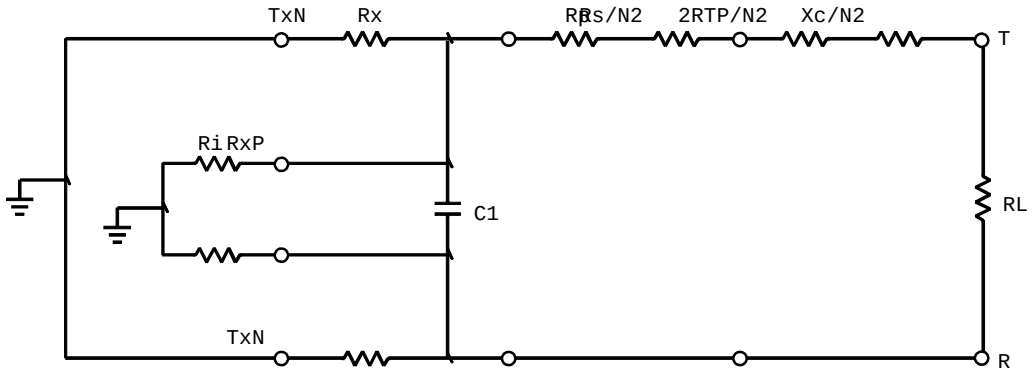



**Figure D-4.** Transformer Model

The transmit model is simplified to include the reflected impedances from the line side of the transformer. The output impedances of the transmit drivers are omitted here. This is shown in **Figure D-4**.

The impedance looking into the secondary side of the transformer must equal $R_L/(N^2)$ in order to terminate the line.

$$\frac{2R_x \cdot 2R_i}{2R_i + 2R_x} + R_P + \frac{R_s + X_e + (2 \cdot R_{TP})}{N^2} = \frac{R_L}{N^2}$$

Rearranging and solving for $R_x$ gives:

$$R_x = R_i \cdot \frac{R_L - (N^2 \cdot R_p) - (2 \cdot R_{TP}) - R_s - X_c}{X_c + R_S + (N^2 \cdot R_P) + (2 \cdot N^2 \cdot R_i) + (2 \cdot R_{TP}) - R_L}$$

Substituting in values for a prototype transformer:

- $R_p$ = 7.9 Ω and Rs = 8.2 Ω
- Xc = 1 / (j * 2 * PI * 40000 * 1E - 06) = - j4 Ω at 40 kHz
- Ri = 5000 Ω
- RTP = 5 Ω

we get:

$$R_{x""} = \frac{5000 \cdot (135 - (7.9 \cdot 1.25^2) - 8.2 - (2 \cdot 5) + j4)}{-j4 + 8.2 + (7.9 \cdot 1.25^2) + (2 \cdot 5000 \cdot 1.25^2) + (2 \cdot 5) - 135}$$

$$"" = 5000 \cdot \frac{104.5 + j4}{15520.5 - j4}$$

$$= 5000 \cdot \frac{104.6 < 2.19°}{15520.5 < -0.01°}$$

$$= 33.7\Omega < 2.20°$$

Since the reactive component is so small, having an angle of only 2.20°, it can be ignored when doing this analysis.

The equation for calculating $R_x$ can be reduced to:

$$R_x = \frac{R_i \cdot (R_L - (N^2 \cdot R_p) - (2 \cdot R_{TP}) - R_s)}{R_s + (N^2 \cdot R_p) + (2 \cdot N^2 \cdot R_i) + (2 \cdot R_{TP}) - R_L}$$

Substituting in values gives:

$$R_x'''' = 5000 \cdot \frac{135 - (7.9 \cdot 1.25^2) - 8.2 - (2 \cdot 5)}{8.2 + (7.9 \cdot 1.25^2) + (2 \cdot 5000 \cdot 1.25^2) + (2 \cdot 5) - 135}$$
$$= 33.65\Omega$$
$$= 33.7\Omega$$

## D.2.2 Transmit Noise Filter Capacitor

Once the transmit series resistor values have been calculated, the transmit noise filter capacitor can be calculated for a 160 kHz cutoff frequency. This capacitor in conjunction with the transmit series resistors acts as a low pass filter to remove the high frequency switching noise in the output signal of the MC145576 TxP and TxN pins.

$$C1 = \frac{1}{2 \cdot (2 \cdot PI \cdot f \cdot R_x)}$$
$$C1 = \frac{1}{2 \cdot (2 \cdot PI \cdot 160000 \cdot 33.7)}$$
$$C1 = 0.015\mu F$$

The nearest commercial value can be used.

The analysis yields the following line interface circuit (see **Figure D-5**).

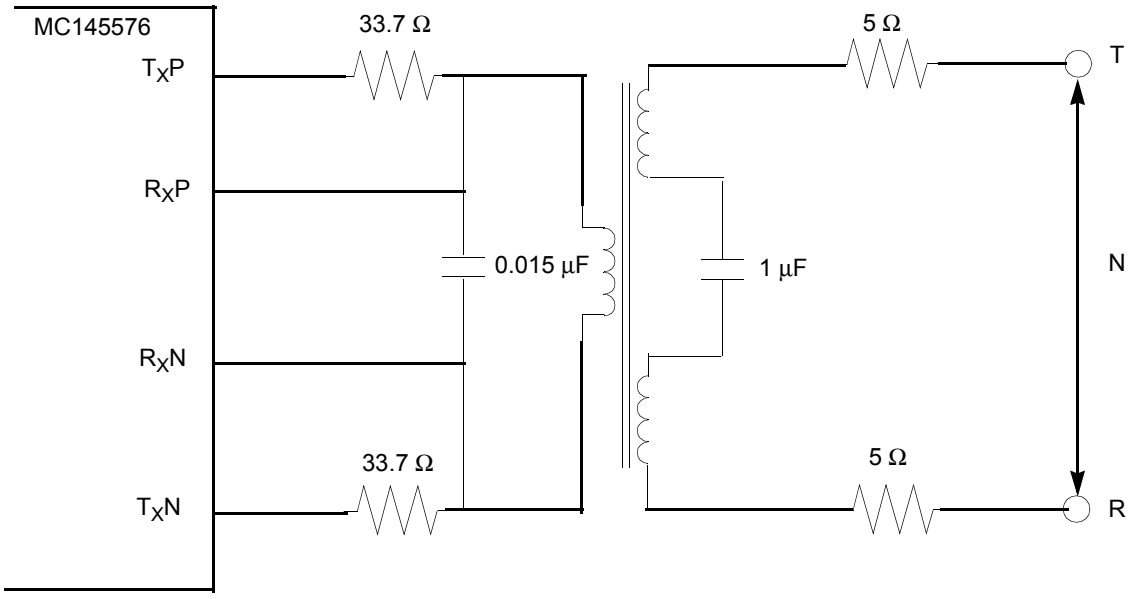



**Figure D-5.** Calculated Line Interface Circuit

# E

# Glossary of Terms and Abbreviations

The list contains terms found in this and other Motorola publications concerned with Motorola Semiconductor products for Communications.

| | |
|---|---|
| **A-Law** | A European companding/encoding law commonly used in PCM systems. |
| **A/B Signaling** | A special case of 8th-bit (LSB) signaling in a μ-law system that allows four logic states to be multiplexed with voice on PCM channels. |
| **Aliasing Noise** | A distortion component that is created when frequencies present in a sampled signal are greater than one-half the sample rate. |
| **Analog to Digital Converter (ADC)** | A converter that uniquely represents all analog input values within a specified total input range by a limited number of digital output codes, each of them exclusively representing a fractional part of the total analog input range. |
| **Answer Back** | A signal sent by receiving data-processing device in response to a request from a transmitting device, indicating that the receiver is ready to accept or has received data. |
| **Anti-Aliasing Filter** | A filter (normally low pass) that band limits an input signal *before sampling to prevent aliasing noise.* |
| **Asynchronous** | A mode of data transmission in which the time occurrence of the bits within each character or block of characters relates to a fixed time frame, but the start of each character or block of characters is not related to this fixed time frame. |
| **Attenuation** | A decrease in magnitude of a communication signal. |
| **Bandwidth** | The information-carrying frequencies between the limiting frequencies of a communication line or channel. |
| **Baseband** | The frequency band occupied by information-bearing signals before combining with a carrier in the modulation process. |
| **Baud** | A unit of signaling speed equal to the number of discrete signal conditions or events per second. This refers to the physical symbols/second used within a transmission channel. |
| **Bit Rate** | The speed at which data bits are transmitted over a communication path, usually expressed in bits per second. A 9600 bps terminal is a 2400 baud system with 4 bits/baud. |
| **Blocking** | A condition in a switching system in which no paths or circuits are available to establish a connection to the called party even though it is not busy, resulting in a busy tone to the calling party. |

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| **BORS(C)HT** | Battery, Overvoltage, Ringing, Supervision, (Codec), Hybrid, Test; the functions performed by a subscriber line card in a telephone exchange. |
| **Broadband** | A transmission facility whose bandwidth is greater than that available on voice-grade facilities. (Also called wide band.) |
| **C Message** | A frequency weighting that evaluates the effects of noise based on its annoyance to the -typical" subscriber of standard telephone service or the effects of noise (background and impulse) on voice-grade data service. |
| **Carrier** | An analog signal of fixed amplitude and frequency that combines with an information-bearing signal by modulation to produce an output signal suitable for transmission. |
| **CCITT** | Consultative Committee for International Telephone and Telegraph—An international standards group of European International Telecommunications Union. |
| **CCSN** | Common Channel Signaling Network. |
| **Central Office (CO)** | A main telephone office, usually within a few miles of a subscriber, that houses switching gear; commonly capable of handling about 10,000 subscribers. |
| **Channel Bank** | Communication equipment commonly used for multiplexing voice-grade channels into a digital transmission signal (typically 24 channels in the U.S. and 30 channels in Europe). |
| **CIDCW** | Calling Identity Delivery on Call Waiting—A subscriber feature which allows for the display of the time, date, number, and possible other information about the caller to the called party while the called party is off-hook. |
| **CLASS** | Custom Local Area Signaling Service—A set of services, enhancements, provided to TELCO customers which may include CND, CNAM, Message Waiting, and other features. |
| **CLID** | Calling Line IDentification—A subscriber feature which allows for the display of the time, date, number, and possible other information about the caller to the called party. |
| **CNAM** | Calling Name Delivery—A subscriber feature which allows for the display of the time, date, number, and name of the caller to the called party. |
| **CND** | Calling Number Delivery—A subscriber feature which allows for the display of the time, date, number, and possible other information about the caller to the called party. |
| **CODEC** | COder-DECoder—The A/D and D/A function on a subscriber line card in a telephone exchange. |
| **COFIDEC** | COder-Filter-DECoder—The combination of a codec, the associated filtering, and voltage references required to code and decode voice in a subscriber line card. |

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| **Common Mode Rejection** | The ability of a device having a balanced input to reject a voltage applied simultaneously to both differential-input terminals. |
| **Companding** | The process in which dynamic range compression of a signal is followed by expansion in accordance with a given transfer characteristic (companding law) which is usually logarithmic. |
| **Compander** | A combination of a compressor at one point in a communication path for reducing the amplitude range of signals, followed by an expander at another point for restoring the original amplitude range, usually to improve the signal-to-noise ratio. |
| **Conference Call** | A call between three or more stations, in which each station can carry on a conversation simultaneously. |
| **CPE** | Customer Premise Equipment—This could be a POTS phone, answering machine, fax machine, or any number of other devices connected to the PSTN. |
| **Crosspoint** | The operating contacts or other low-impedance-path connection over which conversations can be routed. |
| **Crosstalk** | The undesired transfer of energy from one signal path to another. |
| **CSN** | Circuit Switched Network. |
| **CTS** | Clear to send; a control signal between a modem and a controller used to initiate data transmission over a communication line. |
| **CVSD** | Continuous Variable Slope Delta (modulation); a simple technique to converting an analog signal (like voice) into a serial bit stream. |
| **D3** | D3 channel bank—A specific generation of AT&T 24-channel PCM terminal that multiplexes 24 voice channels into a 1.544 MHz digital bit stream. The specifications associated with D3 channel banks are the basis for all PCM device specifications. |
| **Digital to Analog Converter (DAC)** | A converter that represents a limited number of different digital input codes by a corresponding number of discrete analog output values. |
| **Data Compression** | A technique that provides for the transmission of fewer data bits than originally required without information loss. The receiving location expands the received data bits into the original bit sequence. |
| **dB (decibel)** | A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:<br>• 10 x log (P1/P2) for power measurements, and<br>• 20 x log (V1/V2) for voltage measurements. |
| **dBm** | An indication of signal power—1.0 mW across 600 Ω, or 0.775 volts rms, is defined as 0 dBm. Any other voltage level is converted to dBm by:<br>• dBm = 20 x log (Vrms/0.775), or<br>• dBm = [20 x log (Vrms)] + 2.22. |

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| **dBmO** | Signal power measured at a point in a standard test tone level at the same point. (i.e., dBmO = dBm = dBr, where dBr is the relative transmission level, or level relative to the point in the system defined as the zero transmission level point.) |
| **dBmOp** | Relative power expressed in dBmp. (See dBmO and dBmp.) |
| **dBmp** | Indicates dBm measurement made with a psophometric weighting filter. |
| **dBrn** | Relative signal level expressed in decibels above reference noise, where reference noise is 1 pW. Hence, 0 dBrn = 1 pW = –90 dBm. |
| **dBrnC** | Indicates dBrn measurement made with a C-message weighting filter. (These units are most commonly used in the U.S., where psophometric weighting is rarely used.) |
| **dBrnc0** | Noise measured in dBrnc referenced to zero transmission level. |
| **Decoding** | A process in which one of a set of reconstructed analog samples is generated from the digital character signal representing a sample. |
| **Delay Distortion** | Distortion that occurs on communication lines due to the different propagation speeds of signals at different frequencies, measured in microseconds of delay relative to the delay at 1700 Hz. (This type of distortion does not affect voice communication, but can seriously impair data transmission.) |
| **Delta Modulation** | A simple digital coding technique that produces a serial bit stream corresponding to changes in analog input levels; usually utilized in devices employing continuously variable-slope delta (CVSD) modulation. |
| **Demodulator** | A functional section of a modem that converts received analog line signals to digital form. |
| **DN** | Directory Number. |
| **Digital Telephone** | A telephone terminal that digitizes a voice signal for transmission and decodes a received digital signal back to a voice signal. (It will usually multiplex 64 kbps voice and separate data inputs at multiples of 8 kbps.) |
| **Distortion** | The failure to reproduce an original signal's characteristics (i.e., amplitude, phase, delay, etc.) accurately. |
| **DPSK** | Differential Phase Shift Keying—A modulation technique for transmission where the frequency remains constant but phase changes will occur from 90°, 180°, and 290° to define the digital information. |
| **DTMF** | Dual Tone Multi-Frequency—It is the tone dialing system based on outputting two non-harmonic related frequencies simultaneously to identify the number dialed. Eight frequencies have been assigned to the four rows and four columns of a typical keypad. |

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| **Duplex** | A mode of operation permitting the simultaneously two-way independent transmission of telegraph or data signals. |
| **Echo** | A signal that has been reflected or returned as a result of impedance mismatches, hybrid unbalance, or time delay. Depending upon the location of impedance irregularities and the propagation characteristics of a facility, echo may interfere with the speaker/listener or both. |
| **Echo Suppressor** | A device used to minimize the effect of echo by blocking the echo return currents; typically a voice-operated gate that allows communication one way at a time. |
| **Encoder (PCM)** | A device that performs repeated sampling, compression, and A/D conversion to change an analog signal to a serial stream of PCM samples representing the analog signal. |
| **Equalizer** | An electrical network in which phase delay or gain varies with frequency to compensate for an undesired amplitude or phase characteristic in a frequency-dependent transmission line. |
| **ET** | Exchange Termination (C.O. Switch). |
| **FDM** | Frequency-Division Multiplex—A process that permits the transmission of two or more signals over a common path by using a different frequency band for each signal. |
| **Four Wire Circuit** | The portion of a telephone, or central office, that operates on two pairs of wires. One pair is for the transmit path (generally from the microphone), and one pair is for the receive path (generally from the receiver). |
| **Frame** | A set of consecutive digit time slots in which the position of each digit slot can be identified by reference to a frame alignment. The frame alignment signal does not necessarily occur, in whole or in part, in each frame. |
| **Full Duplex** | A mode of operation permitting simultaneous transmission of information between two locations in both directions. |
| **Gain** | The change in signal amplitude (increase or decrease) after passing through an amplifier, or other circuit stage. Usually expressed in dB, an increase is a positive number, and a decrease is a negative number. |
| **Gain Tracking Error** | The variation of gain from a constant level (determined at 0 dBm input level) when measuring the dependence of gain on signal level by comparing the output signal to the input signal over a range of input signals. |
| **HDLC** | High-Level Data Link Control—A CCITT standard data communication line protocol. |
| **Half Duplex** | A transmission system that permits communication in one direction at a time. CB radios with push-to-talk switches and voice-activated speakerphones are half duplex. |

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| **Handset** | A rigid assembly providing both telephone transmitter and receiver in a form convenient for holding simultaneously to mouth and ear. |
| **Hookswitch** | A switch that connects the telephone circuit to the subscriber loop. The name derives from old telephones where the switch was activated by lifting the receiver off and onto a hook on the side of the phone. |
| **Idle Channel Noise (ICN)** | The total signal energy measured at the output of a device or channel under test when the input of the device or channel is grounded (often a wide-band noise measurement using a C-message weighting filter to band-limit the output noise). |
| **Intermodulation** | The modulation of the components of a complex wave by each other (in a nonlinear system). |
| **Intermodulation Distortion** | An analog line impairment when two frequencies interact to create an erroneous frequency, in turn distorting the data signal representation. |
| **IRED** | Infrared—Used as a wireless link for remote control or to transfer data. |
| **ISDN** | Integrated Services Digital Network—A communication network intended to carry digitized voice and data multiplexed onto the public network. |
| **Jitter** | A type of analog communication line distortion caused by abrupt, spurious signal variation from a reference timing position, and capable of causing data transmission errors, particularly at high speeds. (The variation can be in amplitude, time, frequency, or phase.) |
| **Key System** | A miniature PABX that accepts 4 to 10 lines and can direct them to as many as 30 telsets. |
| **µ-law** | A companding law accepted as the North American standard for PCM based systems. |
| **LAN** | Local Area Network—A data-only communication network between data terminals using a standard interface to the network. |
| **Line** | The portion of a circuit external to an apparatus that consists of the conductors connecting the apparatus to the exchange or connecting two exchanges. |
| **Line Length Compensation** | Also referred to as loop length compensation, it involves changing the gain of the transmit and receive paths, within a telephone, to compensate for different signal levels at the end of different line lengths. A short line (close to the CO) will attenuate signals less, and therefore less gain is needed. Compensation circuits generally use the loop current as an indication of the line length. |
| **Longitudinal Balance** | The common-mode rejection of a telephone circuit. |

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| **Loop** | The loop formed by the two subscriber wires (Tip and Ring) connected to the telephone at one end, and the central office (or PBX) at the other end. Generally it is a floating system, not referred to ground, or ac power. |
| **Loopback** | Directing signals back toward the source at some point along a communication path. |
| **Loop Current** | The dc current that flows through the subscriber loop. It is typically provided by the central office or PBX, and ranges from 20 to 120 mA. |
| **LT** | Line Termination (Line Card). |
| **MCU** | MicroComputer Unit (also MicroController Unit). |
| **MPU** | MicroProcessor Unit. |
| **Mu-Law** | A companding/encoding law commonly used in U.S. (same as µ-law). |
| **MUX** | Multiplex or multiplexer. |
| **Modem** | MOdulator-DEModulator; a unit that modulates and demodulates digital information from a terminal or computer port to an analog carrier signal for passage over an analog line. |
| **Multiframing** | When multiframing is enabled, 20 S/T frames are grouped together to provide maintenance subchannels between the TE and the NT. In the TE to NT direction, there is one subchannel called the Q channel. In the NT to TE direction, there are five subchannels called SC1 through SC5. Messages for the Q, SC1, and SC2 subchannels have been defined in CCITT I.430 and ANSI T1.605. Usage of the multiframing subchannels is not mandatory. |
| **Multiplex** | To simultaneously transmit two or more messages on a single channel. |
| **NT1** | Network Termination 1 (OSI Layer 1 Only). |
| **NT2** | Network Termination 2 (OSI Layers 2 and 3). |
| **Off-Hook** | The condition when the telephone is connected to the phone system, permitting loop current to flow. The central office detects the dc current as an indication that the phone is busy. |
| **On-Hook** | The condition when the telephone's dc path is open, and no dc loop current flows. The central office regards an on-hook phone as available for ringing. |
| **PABX** | Private Automatic Branch Exchange—A customer-owned, switchable telephone system providing internal and/or external station-to-station dialing. |
| **Pair** | The two associated conductors that form part of a communication channel. |

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| **Pass-Band Filter** | A filter used in communication systems that allows only the frequencies within a communication channel to pass, and rejects all frequencies outside the channel. |
| **PBX** | Private Branch Exchange—A class of service in standard Bell System terminology that typically provides the same service as PABX. |
| **PCM** | Pulse Code Modulation—A method of transmitting data in which signals are sampled and converted to digital words that are then transmitted serially, typically as 8-bit words. |
| **Phase Jitter** | Abrupt, spurious variations in an analog line, generally caused by power and communication equipment along the line that shifts the signal phase relationship back and forth. |
| **PLL** | Phase Lock Loop. |
| **PLL Frequency Synthesizer** | Phase Lock Loop frequency synthesizer—A frequency synthesizer utilizing a closed loop, as opposed to DDS (direct digital synthesis) which is not a closed loop. |
| **POTS** | Plain Old Telephone Service. |
| **Propagation Delay** | The time interval between specified reference points on the input and output voltage waveforms. |
| **Psophometric Weighting** | A frequency weighting similar to C-Message weighting that is used as the standard for European telephone system testing. |
| **PSN** | Packet Switched Network. |
| **PSTN** | Public Switched Telephone Network. |
| **Pulse Dialer** | A device that generates pulse trains corresponding to digits or characters used in impulse or loop-disconnect dialing. |
| **Quantizing Noise** | Signal-correlated noise generally associated with the quantizing error introduced by A/D and D/A conversions in digital transmission systems. |
| **REN** | Ringer Equivalence Number—An indication of the impedance, or loading factor, of a telephone bell or ringer circuit. An REN of 1.0 equals about 8 kΩ. The Bell system typically permits a maximum of 5.0 REN (1.6 kΩ) on an individual subscriber line. A minimum REN of 0.2 (40 kΩ) is required by the Bell system. |
| **Repeater** | An amplifier and associated equipment used in a telephone circuit to process a signal and retransmit it. |
| **Repertory Dialer** | A dialer that stores a repertory of telephone numbers and dials any one of them automatically on request. |
| **Ring** | One of the two wires connecting the central office to a telephone. The name derives from the ring portion of the plugs used by operators (in older equipment) to make the connection. Ring is traditionally negative with respect to Tip. |

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| **rms** | Root mean squared—This is the way ac voltage and amperage is evaluated mathematically to determine power consumption or dissipation measurements. |
| **RTS** | Request To Send—an EIA-232 control signal between a modem and user's digital equipment that initiates the data transmission sequence on a communication line. |
| **Sampling Rate** | The frequency at which the amplitude of an analog signal is gated into a coder circuit. The Nyquist sampling theorem states that if a band-limited signal is sampled at regular intervals and at a rate equal to or greater than twice the highest frequency of interest, the sample contains all the information of the original signal. The frequency band of interest in telephony ranges from 300 to 3400 Hz, so a sampling rate of 8 kHz provides dc to 4000 Hz reproduction. |
| **SCU** | Subscriber Channel Unit—The circuitry at a telephone exchange associated with an individual subscriber line or channel. |
| **Sidetone** | The sound fed back to the receiver as a result of speaking into the microphone. It is a natural consequence of the 2-to-4 wire conversion system. Sidetone was recognized by Alexander Graham Bell as necessary for a person to be able to speak properly while using a handset. |
| **Signaling** | The transmission of control or status information between switching systems in the form of dedicated bits or channels of information inserted on trunks with voice data |
| **Signal-to-Distortion Ratio (S/D)** | The ratio of the input signal level to the level of all components that are present when the input signal (usually a 1.020 kHz sinusoid) is eliminated from the output signal (e.g., by filtering) |
| **SLIC** | Subscriber Line Interface Circuit—A circuit that performs the 2-to-4 wire conversion, battery feed, line supervision, and common mode rejection at the central office (or PBX) end of the telephone line. |
| **Smart NT1** | Network Termination with integrated TA |
| **SOG Package** | Small-Outline Gull-wing package—Formerly SOIC with gull-wing leads. This package has leads which fold out from the body. |
| **SOJ Package** | Small-Outline J-lead package—Formerly SOIC with J leads. This package has leads which are tucked under the body. |
| **Speech Network** | A circuit that provides 2-to-4 wire conversion, (i.e., connects the microphone and receiver (or the transmit and receive paths) to the Tip and Ring phone lines). Additionally it provides sidetone control, and in many cases, the dc loop current interface. |
| **Subscriber Line** | The system, consisting of the user's telephone, the interconnecting wires, and the central office equipment dedicated to that subscriber (also referred to as a loop). |

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| **Switchhook** | A synonym for hookswitch. |
| **Syn (Sync)** | (1) A bit character used to synchronize a time frame in a time-division multiplexer. (2) A sequence used by a synchronous modem to perform bit synchronization or by a line controller for character synchronization. |
| **Synchronous Modem** | A modem that uses a derived clocking signal to perform bit synchronization with incoming data. |
| **T1 Carrier** | A PCM system operating at 1.544 MHz and carrying 24 individual voice-frequency channels. |
| **TA** | Terminal Adapter. |
| **Talkdown** | Missed signals in the presence of speech. Commonly used to describe the performance of a DTMF receiver when it fails to recognize a valid DTMF tone due to cancellation of that tone by speech. |
| **Talkoff** | False detections caused by speech. Commonly used to describe the performance of a DTMF receiver when speech, emulating DTMF, causes the receiver to believe it has detected a valid DTMF tone. |
| **Tandem Trunk** | See trunk. |
| **Telephone Exchange** | A switching center for interconnecting the lines that service a specific area. |
| **TE1** | Terminal Equipment 1 (ISDN Terminal). |
| **TE2** | Terminal Equipment 2 (Non-ISDN Terminal). |
| **TELETEX** | A text communication service between entirely electronic work stations that will gradually replace TELEX with the introduction of the digital network. (Not to be confused with teletext.) |
| **TELETEXT** | The name usually used for broadcast text (and graphics) for domestic television reception. (Not to be confused with teletex.) |
| **Time-Division Multiplex** | A process that permits the transmission of two or more signals over a common path by using a different time interval for each signal. |
| **Tin Cans and String** | A *crude analog communications system commonly used to introduce voice communications to children.* |
| **Tip** | One of the two wires connecting the central office to a telephone. The name derives from the tip of the plugs used by operators (in older equipment) to make the connection. Tip is traditionally positive with respect to ring. |
| **Tone Ringer** | The modern solid state equivalent of the old electromechanical bell. It provides the sound when the central office alerts the subscriber that someone is calling. Ringing voltage is typically 80-90 volts rms, 20 Hz. |

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| **Trunk** | A telephone circuit or channel between two central offices or switching entities. |
| **TSAC** | Time Slot Assigner Circuit—A circuit that determines when a CODEC will put its 8 bits of data on a PCM bit stream. |
| **TSIC** | Time Slot Interchange Circuit—A device that switches digital highways in PCM based switching systems; a -digital" crosspoint switch. |
| **Twist** | The amplitude ratio of a pair of DTMF tones. (Because of transmission and equipment variations, a pair of tones that originated equal in amplitude may arrive with a considerable difference in amplitude.) |
| **Two Wire Circuit** | Refers to the two wires connecting the central office to the subscriber's telephone. Commonly referred to as Tip and Ring, the two wires carry both transmit and receive signals in a differential manner. |
| **UDLT** | Universal Digital Loop Transceiver—A Motorola originated name for a voice/data transceiver circuit. |
| **VCO** | Voltage-controlled oscillator—Input is a voltage; output is a sinusoidal waveform. |
| **VCM** | Voltage-controlled multivibrator—Input is a voltage; output is a square wave. |
| **Voice Frequency** | A frequency within that part of the audio range that is used for the transmission of speech of commercial quality (i.e., 300-3400 Hz). |
| **Weighting Network** | A network whose loss varies with frequency in a predetermined manner. |

# F

# Standards Bodies

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