MC92600EVKUG
4/2004
Rev. 2

MC92600 Quad SerDes Evaluation Kit User's Guide

Devices Supported:
MC92600JUB
MC92600CJUB
MC92600ZTB

Contents

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Chapter 1
General Information

1.1 Introduction

This user's guide describes the MC92600EVK evaluation kit, which comes equipped with an evaluation board containing either the 217-pin PBGA version or the 196-pin FBGA version of MC92600, depending on which transceiver is being tested. It should be read in conjunction with the *MC92600 Quad 1.25 Gbaud SerDes User's Manual* (MC92600UM). The MC92600EVK evaluation board is intended for testing purposes only. Motorola does not guarantee its performance in a production environment.

1.2 Abbreviation List

Table 1-1 contains abbreviations used in this document.

Table 1-1. Acronyms and Abbreviated Terms

Term	Meaning
'1'	High logic level (nominally 2.5 or 3.3 V)
'0'	Low logic level (nominally 0.0 V)
BERC	Bit error rate checker
BIST	Built-in self-test
I/F	Interface
N/C	No connection
PN	Pseudo-noise
TDR	Time delay reflectometry

1.3 Related Documentation

Related documentation includes the following:

- *MC92600 Quad 1.25 Gbaud SerDes User's Manual* (MC92600UM)
- MPC948 Low Voltage 1:12 Clock Distribution Chip data sheet
- IEEE Std 802.3-2002®, Part 3: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications
- MC12429 High Frequency Clock Generator data sheet

1.4 Specifications

The MC92600EVK evaluation board specifications are provided in Table 1-2.

Table 1-2. MC92600EVK Evaluation Board Specifications

Characteristics		Specifications
Power supply		+5 V DC @ 1.0 A typical
Package		217 PBGA or 196 FBGA
Operating temperature		0°–30°C
Dimensions:	Height	305 mm
	Width	261 mm
	Thickness	2.1 mm

1.5 Development Board Features

The following are the functional, physical, and performance features of the MC92600EVK kit:

- Single, external 5.0-V power supply provides onboard voltage regulators for 3.3- and 1.8-V requirements.
- Onboard frequency synthesizer provides reference clock for a range of frequencies.
- 2×10 and 2×20 header connectors for parallel data and control interfaces
- SMA female connectors allow the use of a differential interface
- Two sets of 50-Ω etch test traces for TDR measurements

1.6 Block Diagram

Figure 1-1 shows the MC92600 evaluation board block diagram.

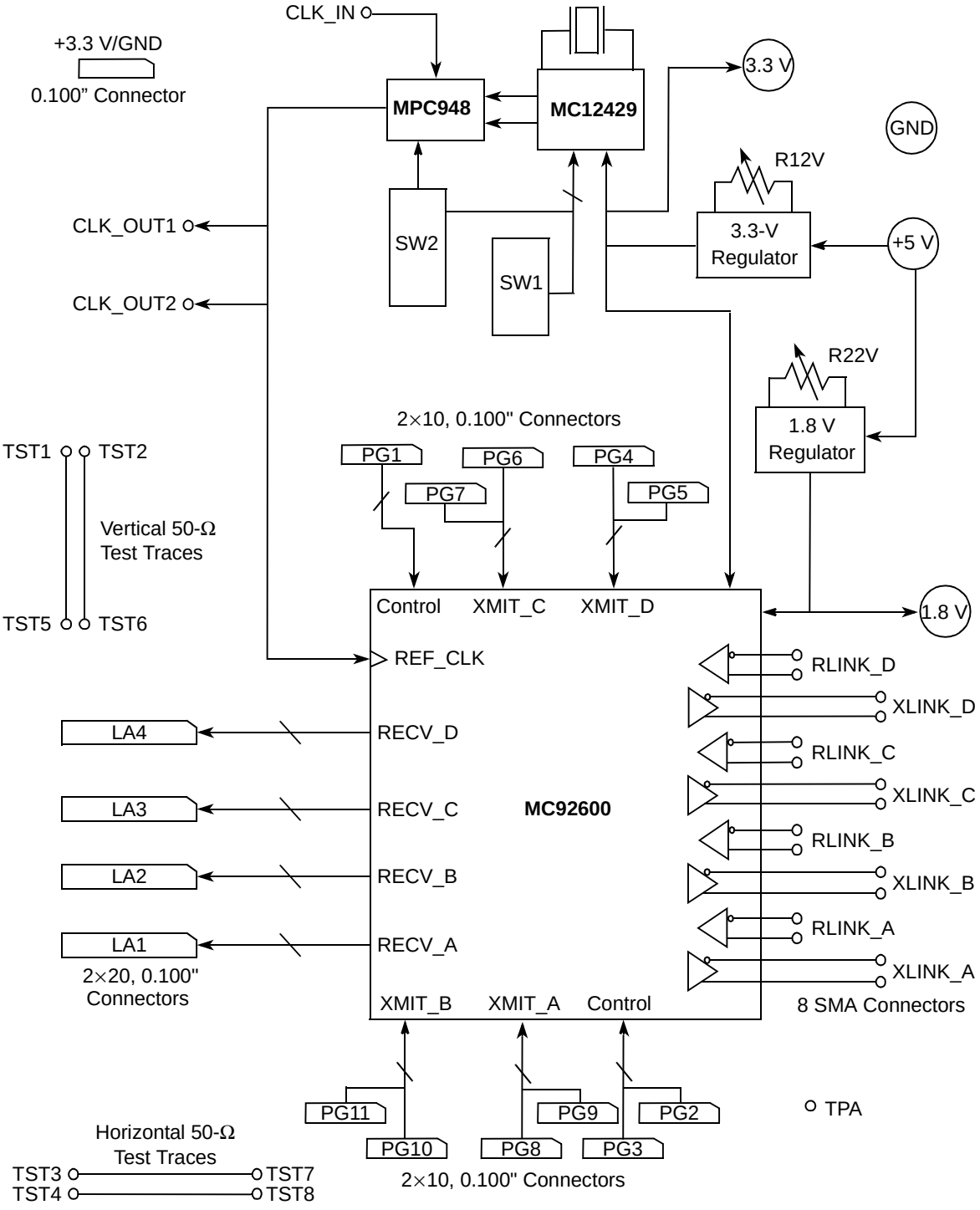

Figure 1-1. Block Diagram of the MC92600EVK Evaluation Board

1.7 Board Components

Table 1-3 is a list of major components of the MC92600EVK evaluation board.

Table 1-3. Board Components

Component	Description
2×10, 0.100" connector	PG1–PG11 provide access to the parallel inputs and control signals
2×20, 0.100" connectors	Connectors LA1–LA4 provide access to the parallel outputs RECV_A – RECV_D.
SMA connectors	Pairs of serial links that provide access to the MC92600 receivers and transmitters
1.8-V regulator	Power supply fed through 5.0-V external supply
3.3-V regulator	Power supply fed through 5.0-V external supply
MC12429	High frequency clock generator that generates a differential clock. It is programmable through onboard switches for a range of operating frequencies.
MPC948	Low voltage 1:12 clock distribution chip (LVPECL) that converts a differential clock signal into a TTL clock buffer
External clock	Supplied through CLK_IN
Vertical and horizontal test trace pairs	These traces (TST1–TST8) along with SMA connections facilitate TDR measurements of the characteristic impedance of representative board traces. Board traces are nominally 50 Ω ± 5%.
Dip switches	SW1 and SW2
3.3-V/GND connector	A power jump connector used for connecting static control bits to a logic 1.
TPA	PCB test socket, used for factory testing purposes only. This should remain disconnected at all times.

Chapter 2
Hardware Preparation and Installation

This chapter provides unpacking, hardware preparation, configuration, and installation instructions for the MC92600EVK evaluation kit.

2.1 Unpacking Instructions

Unpack equipment from the shipping carton. Refer to the packing list and verify that all items are present. Save the packing material for storing and reshipping of equipment.

NOTE

If the shipping carton is damaged on receipt, request the carrier's agent to be present during the unpacking and inspection of equipment.

Avoid touching areas of integrated circuitry; static discharge can damage circuits.

2.2 Kit Contents

The list in Table 2-1 shows the contents shipped with the MC92600EVK kit:

Table 2-1. Contents List for MC92600EVK

No.	Item Description
1	MC92600EVK evaluation board (either 217- or 196-pin version)
1	*MC92600EVK Quad SerDes Evaluation Kit User's Guide*
1	*MC92600 Quad 1.25 Gbaud SerDes User's Manual*
1	Set of MC92600EVK evaluation board schematics (5 pages)
1	Set of MC92600EVK evaluation board layout diagrams (8 pages)
50	0.100" shunts
12	Square pin receptacle patch cords

2.3 Hardware Preparation

To select the desired configuration and ensure proper operation of the MC92600EVK evaluation board, changes of the dip-switch settings may be required before installation.

The location of the switches, indicators, dip-switches, and connectors is illustrated in Figure 2-1.

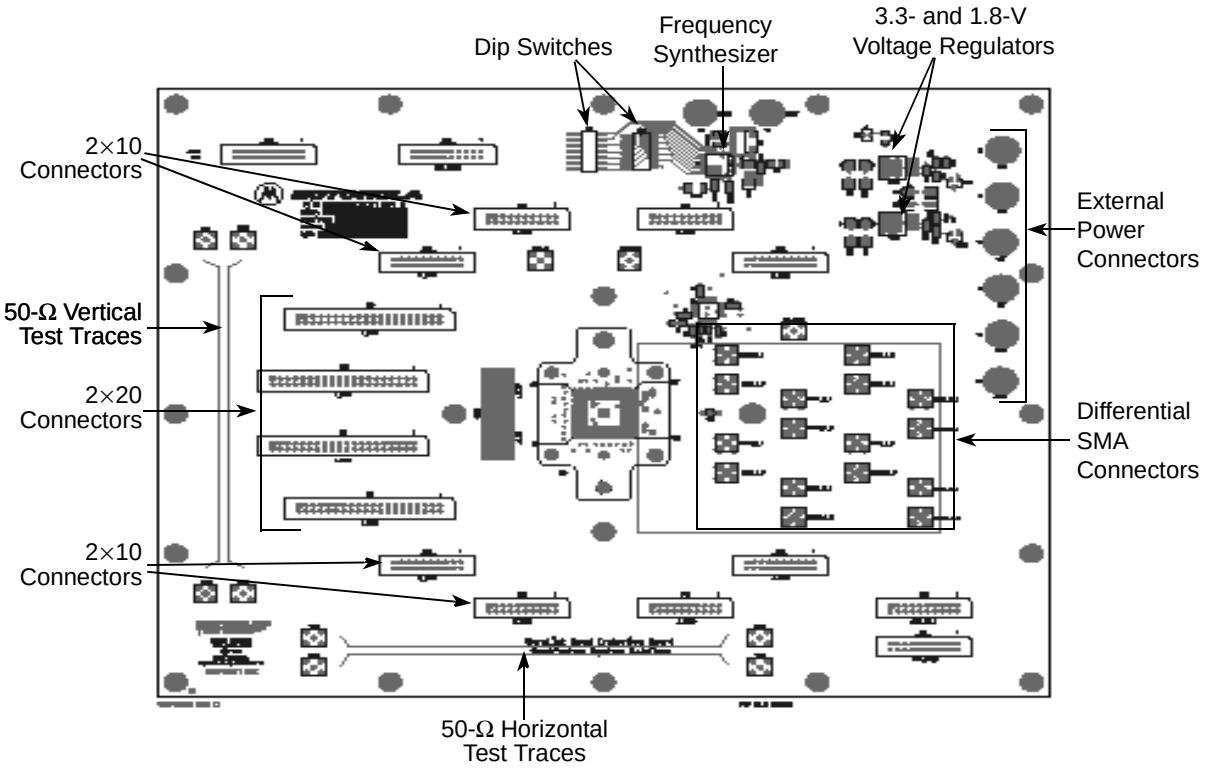

Figure 2-1. Top Side Part Location Diagram

2.4 Setting a Reference Clock Source

The input reference clock for the MC92600 can be supplied by two methods:

- Using the onboard MC12429 frequency synthesizer and MPC948 clock distribution chip (refer to Section 2.4.1, “How to Generate a Clock Frequency from the MC12429”)
- Directly driving an external reference clock into the MPC948 clock buffer circuit on the board (refer to Section 2.4.2, “How to Setup the External Reference Clock”)

2.4.1 How to Generate a Clock Frequency from the MC12429

The output frequency from the MC12429 frequency synthesizer is controlled by a 20-MHz quartz crystal oscillator and by the values programmed into the sythensizer's feedback and output dividers. The output frequency can be calculated from:

$$F_{out} = \left(\frac{F_{xtal}}{8}\right)\sum \frac{M}{2^{(N+1)}}$$

where:

F_{out} = output frequency,

F_{xtal} = quartz crystal oscillator frequency,

M = feedback divider value,

$2^{(N+1)}$ = output divider value.

Refer to the MC12429 data sheet for a detailed description of M and N.

The values for the feedback and output dividers can be set via dip switch packages SW1 and SW2, according to Table 2-2. SW2 switches 1–3 and SW1 switches 2–7 are the feedback divider switches that set the binary value of M[8:0]. Switches 4 and 5 of SW2 set the value of N[1:0] that controls the output divider.

Table 2-2. DIP Switch Connections

Switch Package	Switch No.	Connection	Description
SW1	1	MC12429—pin 6	Frequency synthesizer output enable, active high
	2	MC12429— pin 8	M[0]—feedback divider LSB
	3	MC12429—pin 9	M[1]—feedback divider
	4	MC12429—pin 10	M[2]—feedback divider
	5	MC12429—pin 11	M[3]—feedback divider
	6	MC12429—pin 12	M[4]—feedback divider
	7	MC12429—pin 13	M[5]—feedback divider
SW2	1	MC12429—pin 14	M[6]—feedback divider
	2	MC12429—pin 15	M[7]—feedback divider
	3	MC12429—pin 16	M[8]—feedback divider MSB
	4	MC12429—pin 17	N0—output divider control LSB
	5	MC12429—pin 18	N1—Output Divider Control MSB
	6	MPC948—pin 1	TTL_CLK SEL—TTL clock select

Table 2-3 lists applicable switch settings for dip switch packages SW1 and SW2 for commonly used clock frequencies.

Table 2-3. Frequency Synthesizer Switch Settings

SW 1 Switch Settings 7 6 5 4 3 2 1	SW2 Switch Settings 6 5 4 3 2 1	Output Frequency (MHz)	Output Divider $2^{(N + 1)}$	N[1:0]	Feedback Divider	M[8:0]
1 0 0 0 0 0 1	0 1 1 0 1 0	25.00	16	1 1	160	0 1 0 1 0 0 0 0 0
0 0 1 0 0 0 1	0 1 1 0 1 1	31.25	16	1 1	200	0 1 1 0 0 1 0 0 0
0 0 0 0 0 0 1	0 1 1 1 0 1	50.00	16	1 1	320	1 0 1 0 0 0 0 0 0
0 1 0 0 0 0 1	0 1 1 1 1 0	62.50	16	1 1	400	1 1 0 0 1 0 0 0 0
1 0 0 0 0 0 1	0 1 0 1 0 0	90.00	8	1 0	288	1 0 0 1 0 0 0 0 0
1 1 0 0 0 0 1	0 1 0 1 0 0	95.00	8	1 0	304	1 0 0 1 1 0 0 0 0
0 0 0 0 0 0 1	0 1 0 1 0 1	100.00	8	1 0	320	1 0 1 0 0 0 0 0 0
1 0 0 0 0 0 1	0 1 0 1 0 1	110.00	8	1 0	352	1 0 1 1 0 0 0 0 0
0 1 0 0 0 0 1	0 1 0 1 1 0	125.00	8	1 0	400	1 1 0 0 1 0 0 0 0

A switch in the ‘on’ position shorts the connection to ground and is equivalent to a logic ‘0.’ Switches 5 and 4 of SW2 represent N[1:0]. Switches 3–1 of SW2 and switches 7–2 of SW1 represent M[8:0]. SW2, switch 6 is the clock buffer TTL clock select and SW1, switch 1 is the frequency synthesizer output enable. The switch settings shown in Table 2-3 show the TTL clock select disabled and the frequency synthesizer enabled.

Specifications for the MC12429 state that the higher the synthesizer voltage-controlled oscillator frequency, the lower the clock jitter.

Figure 2-2 depicts an example switch setting for generating 62.5 MHz, where M[8:0] equals 400 and $2^{(N + 1)}$ equals 16.

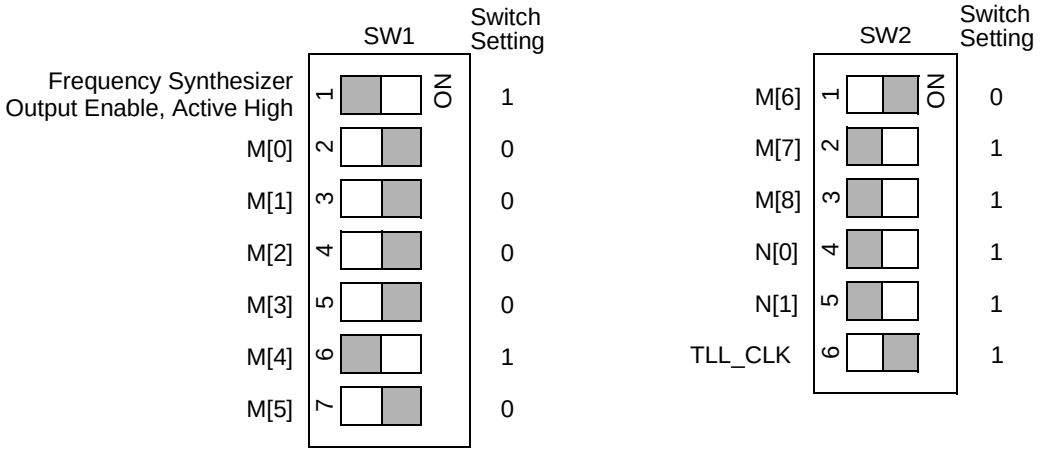

Figure 2-2. Switch Contact Settings for Generating a 62.5-MHz Reference Clock

2.4.2 How to Setup the External Reference Clock

To supply a reference clock, the frequency synthesizer and LVPECL conversion can be disabled via switches on SW1 and SW2:

- Set switch number 1 to a ‘0’ on SW1 to disable the frequency synthesizer
- Set switch number 6 on SW2 to a ‘1’ to disable the LVPECL inputs to the clock buffer.

The user must then supply a TTL level input clock via the SMA connector, CLK_IN. This input clock will be buffered by the MPC948 and connected to the REF_CLK input of the MC92600 and the CLK_OUT1 and CLK_OUT2 SMA connectors.

2.5 Contact Information

To ask questions about the MC92600 evaluation kit or to place an order for a kit please contact your local Motorola Field Applications Engineer.

Chapter 3
Operating Components

This chapter describes in detail the components of the MC92600EVK evaluation board.

3.1 MC12429 High Frequency Clock Generator

The MC12429 puts out a differential low-voltage, positive ECL (LVPECL) signal. This signal is converted and distributed by the MPC948 distribution chip.

3.2 MPC948 Low Voltage (1:12) Clock Distribution Chip

The MPC948 level-shifts, converts to single-ended, and buffers the differential signal generated by the MC12429. The resulting signal is a 50-Ω, series-terminated, +3.3-V peak-to-peak square wave. The chip has 12 outputs:

- Four outputs are connected to the REF_CLK input of the MC92600
- Eight outputs are divided between the two SMA connectors, CLK_OUT1 and CLK_OUT2.

These connections are conveniently placed to provide board synchronized trigger signals for use with laboratory equipment. For more information on the MPC948 and MC12429 refer to Motorola's website at http://www.motorola.com/semiconductors.

3.3 Power Supplies

The evaluation board requires a single 5.0-V supply. Fully operational, the board will draw a maximum current of 1.0 amp from the 5.0-V supply. Actual current consumption depends on the user set voltage levels, clock frequencies, and MC92600 operating mode. The board contains two +5.0-V connection posts and two ground connection posts. These duplicate connections simplify using a four-wire supply: supply and ground, force and sense.

The 5.0-V supply is used to power two onboard voltage regulators, VR33 and VR18. These regulators generate 3.3 and 1.8 V, respectively:

- The 3.3-V supply provides power to the MC92600 parallel I/O, as well as the frequency synthesizer and clock buffer chips. This supply can be varied over the range of 3.3 V ± 0.3 V using the R12V potentiometer.
- The 1.8-V supply, which is used to power the MC92600 transceivers and on-chip phase-locked loop (PLL), can be adjusted over the range 1.8 V ± 0.15 V using R22V. Both the 3.3- and 1.8-V supplies are accessible via connection posts.

3.4 Parallel I/O

The MC92600 parallel I/O is supplied by the +3.3-V voltage regulator and has a rail-to-rail signal swing. There are no bi-directional signals on the MC92600 or on the evaluation board.

3.4.1 Inputs: 2×10, 0.100" Connectors

The parallel inputs, both data and status, as well as the control inputs are connected to 2×10, 0.100" connectors, PG1–PG11. Figure 3-1 depicts the 2×10, 0.100" connector numbering scheme, with pin 1 being labelled on the board. A complete mapping of the MC92600 inputs to the 2×10, 0.100" connectors is listed in Table A-1 through Table A-11. For further description of the input functionality of the MC92600, refer to the *MC92600 Quad 1.25 Gbaud SerDes User's Manual*.

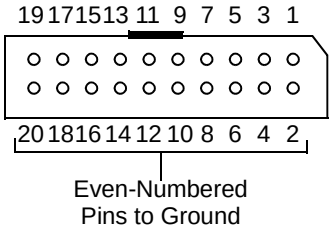

Figure 3-1. 2×10, 0.100" Input Connector Numbering Scheme (Top View)

3.4.2 Outputs: 2×20, 0.100" Connectors

All parallel outputs, both data and status bits are present at four 2×20, 0.100" connectors, LA1–LA4. Figure 3-2 depicts the 2×20, 0.100" output connector numbering scheme, with pin 1 labelled on the board. A complete mapping of the MC92600 outputs to the 2×20, 0.100" connectors is listed in Table A-12 through Table A-15. All even number pins are connected to ground. For further information regarding the MC92600 outputs, refer to the *MC92600 Quad 1.25 Gbaud SerDes User's Manual*.

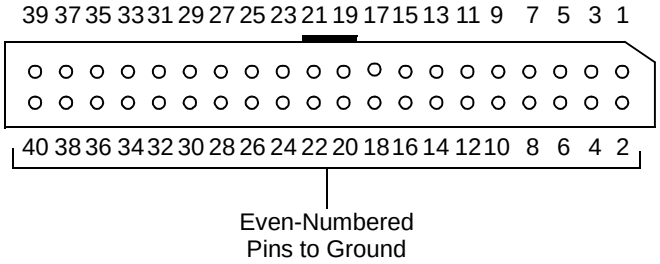

Figure 3-2. 2×20, 0.100" Output Connector Numbering Scheme (Top View)

3.4.3 +3.3-V and Ground (GND) Access Connections

The evaluation board also has one 2×10, 0.100" connector (PG12) with dedicated connections to the +3.3-V and ground planes. These can be useful for biasing parallel input signals using jumper cables. All even numbered pins are connected to ground and all odd numbered pins are connected to +3.3 V.

3.5 Serial I/O: SMA Connectors

All MC92600 high-speed serial differential inputs and outputs are connected to appropriately labeled pairs of SMA connectors through board traces with a characteristic impedance of 50 Ω (100-Ω differential). The input control bit MEDIA (see Table A-2) must be low to set the high-speed serial output driver impedance to 50-Ω, to match the trace impedance. The output driver requires a 50-Ω parallel termination to mid-rail (0.9 V nominal). If the termination voltage is not 0.9 V, the signal must be AC coupled. Since the board is DC coupled, AC coupling (DC blocking) must be done in-line.

During all testing, the serial transmitter outputs should be terminated with 50 Ω. This is done by connecting the serial transmitter outputs to the serial receiver inputs, to any laboratory equipment with 50-Ω input impedance through in-line AC coupling, or by terminating the outputs with 50-Ω SMA terminators.

3.6 Special Connections

The evaluation board also contains an oscilloscope PCB test socket, labelled TPA. When the MC92600 is configured for PLL test mode, this test socket enables special access to the PLL. This test mode is for factory testing purposes only. There are no in-system applications for this mode and test socket TPA should remain unconnected at all times. Refer to the *MC92600 Quad 1.25 Gbaud SerDes User's Manual* for more information.

3.7 Test Traces

The evaluation board has both vertical and horizontal 50-Ω test traces:

- Vertical: TST1–TST5 and TST2–TST6
- Horizontal: TST3–TST7 and TST4–TST8

3.8 Voltage Regulators

Both a 3.3- and a 1.8-V regulator are present on the board.

Chapter 4
Test Procedures

The MC92600 is a high-speed, full duplex, serial data interface that can be used to transmit and receive data. It contains a rich feature set which makes it adaptable to many applications. The MC92600EVK evaluation kit comes equipped to immediately demonstrate two of the MC92600 functions:

- Data-eye signal generation and observation (Section 4.2, “Data-Eye Signal Generation and Observation”)
- Bit error rate checking (Section 4.3, “Bit Error Rate Checking”)

Although full evaluation of the MC92600 can be performed using the evaluation kit, the details of testing in specific systems is left to the user. For more information regarding the MC92600 feature set, refer to the *MC92600 Quad 1.25 Gbaud SerDes User’s Manual*.

4.1 Laboratory Setup

To test the MC92600 using the MC92600EVK board, the equipment listed in Table 4-1 (or equivalent) is recommended.

Table 4-1. Recommended Test Equipment

Quantity	Equipment
1	MC92600 evaluation kit
1	Tektronix 11801C digital sampling oscilloscope containing: • 1—Tektronix SD-24 TDR/sampling head (20 GHz) • 3—Tektronix SD-26 sampling heads (20 GHz)
1	Hewlett Packard HP16700 logic analysis system containing: • 5—Hewlett-Packard HP16522A pattern generators • 2—Hewlett-Packard HP16557D logic analyzers
1	Hewlett Packard HP6624A system DC power supply
10	SMA male each end coax patch cords
2	SMA 3dB attenuators
3	SMA DC blockers (AC couplers)
10	50-Ω SMA terminations

4.2 Data-Eye Signal Generation and Observation

The MC92600 has an integrated, 23rd order, pseudo-noise (PN) pattern generator. The implementation of the 23-bit PN generator uses the polynomial:

$$f = 1 + x^5 + x^{23}$$

Stimulus from this generator can be used for system testing. Generation and observation of the data-eye produced by the PN generator requires the following:

- MC92600EVK evaluation board
- +5-V power supply
- High-speed digital sampling scope
- 0.100" shunts
- Single-pin receptacle patch cords

The shunts and patch cords are provided with the evaluation kit. The following sections describe how to setup the evaluation kit to observe the data-eye in full-speed mode.

4.2.1 Setting Up the Data-Eye Test Equipment

To generate a data-eye pattern, setup the MC92600EVK evaluation board using these steps:

1. Connect the test equipment as shown in Figure 4-1.
2. Configure the dip switches SW1 and SW2 as shown in Figure 4-1. Note that all unconnected serial transmitter outputs should be terminated to 50 Ω. This termination can be done by connecting the serial transmitter outputs to the serial receiver inputs or to 50-Ω SMA terminations.

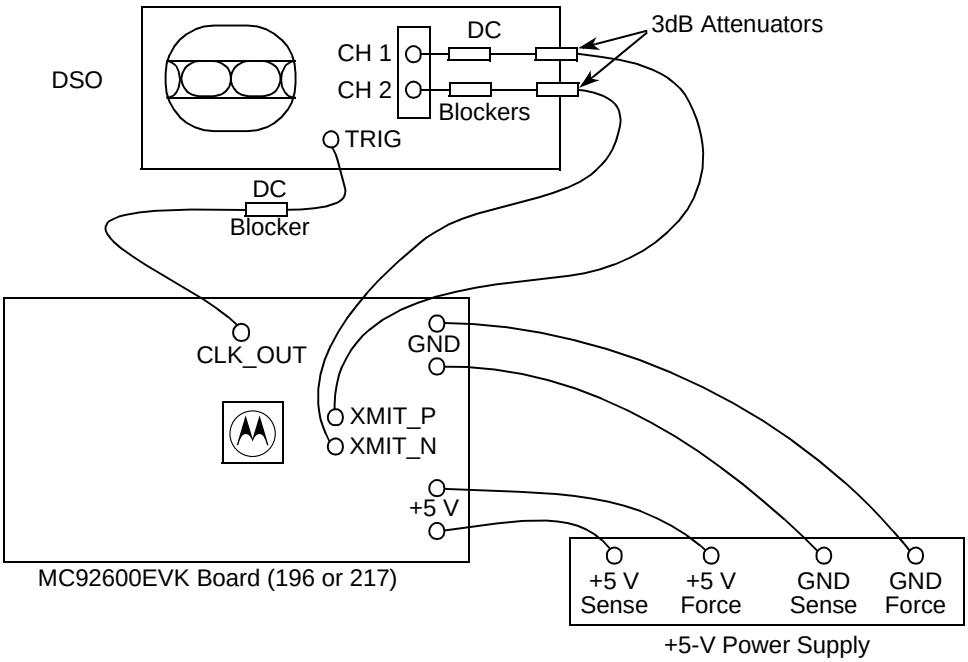

Figure 4-1. Data-Eye Observation Setup

4.2.1.1 Parallel Input Connections

The following parallel inputs must be biased according to Table 4-2. Ground connections can be made using the 0.100" shunts. Connections to +3.3 V can be made using the square pin receptacle patch cords. All even number pins on the connector headers are connected to the board's ground plane. All unlisted pins are not connected.

Table 4-2. Data-Eye Generation Parallel Input Biasing

Pin	CTRL_SIG_0 Signal	CTRL_SIG_0 Bias Level	Pin	A_XMIT0 Signal	A_XMIT0 Bias Level	Pin	A_XMIT1 Signal	A_XMIT1 Bias Level
1	REPE	GND	1	XMIT_A_0	GND	1	XMIT_A_K	+3.3V
3	RCCE	+3.3V	3	XMIT_A_1	GND	3	$\overline{\text{XMIT\_A\_IDLE}}$	GND
5	WSE	GND	5	XMIT_A_2	GND	5	—	N/C
7	HSE	GND	7	XMIT_A_3	GND	7	—	N/C
9	ADIE	GND	9	XMIT_A_4	GND	9	—	N/C
11	$\overline{\text{RESET}}$	Jumper to GND	11	XMIT_A_5	GND	11	—	N/C
13	DDR	GND	13	XMIT_A_6	GND	13	—	N/C
15	STNDBY	GND	15	XMIT_A_7	GND	15	—	N/C
17	—	N/C	17	—	N/C	17	—	N/C
19	GND	N/C	19	GND	N/C	19	GND	N/C

Pin	CTRL_SIG_1 Signal	CTRL_SIG_1 Bias Level	Pin	B_XMIT0 Signal	B_XMIT0 Bias Level	Pin	B_XMIT1 Signal	B_XMIT1 Bias Level
1	LBOE	GND	1	XMIT_B_0	GND	1	XMIT_B_K	+3.3V
3	LBE	GND	3	XMIT_B_1	GND	3	$\overline{\text{XMIT\_B\_IDLE}}$	GND
5	MEDIA	GND	5	XMIT_B_2	GND	5	—	N/C
7	TBIE	GND	7	XMIT_B_3	GND	7	—	N/C
9	—	N/C	9	XMIT_B_4	GND	9	—	N/C
11	—	N/C	11	XMIT_B_5	GND	11	—	N/C
13	—	N/C	13	XMIT_B_6	GND	13	—	N/C
15	—	N/C	15	XMIT_B_7	GND	15	—	N/C
17	—	N/C	17	—	N/C	17	—	N/C
19	GND	N/C	19	GND	N/C	19	GND	N/C

Pin	CTRL_SIG_2 Signal	CTRL_SIG_2 Bias Level	Pin	C_XMIT0 Signal	C_XMIT0 Bias Level	Pin	C_XMIT1 Signal	C_XMIT1 Bias Level
1	BSYNC_0	+3.3V	1	XMIT_C_0	GND	1	XMIT_C_K	+3.3V
3	BSYNC_1	GND	3	XMIT_C_1	GND	3	$\overline{\text{XMIT\_C\_IDLE}}$	GND
5	TST_1	GND	5	XMIT_C_2	GND	5	—	N/C
7	TST_0	+3.3V	7	XMIT_C_3	GND	7	—	N/C
9	WSE_GEN	GND	9	XMIT_C_4	GND	9	—	N/C
11	—	N/C	11	XMIT_C_5	GND	11	—	N/C
13	—	N/C	13	XMIT_C_6	GND	13	—	N/C
15	—	N/C	15	XMIT_C_7	GND	15	—	N/C
17	—	N/C	17	—	N/C	17	—	N/C
19	GND	N/C	19	GND	N/C	19	GND	N/C

Table 4-2. Data-Eye Generation Parallel Input Biasing (continued)

Pin	D_XMIT0 Signal	D_XMIT0 Bias Level	Pin	D_XMIT1 Signal	D_XMIT1 Bias Level
1	XMIT_D_0	GND	1	XMIT_D_K	+3.3V
3	XMIT_D_1	GND	3	$\overline{\text{XMIT\_D\_IDLE}}$	GND
5	XMIT_D_2	GND	5	—	N/C
7	XMIT_D_3	GND	7	—	N/C
9	XMIT_D_4	GND	9	—	N/C
11	XMIT_D_5	GND	11	—	N/C
13	XMIT_D_6	GND	13	—	N/C
15	XMIT_D_7	GND	15	—	N/C
17	—	N/C	17	—	N/C
19	GND	N/C	19	GND	N/C

4.2.2 Data-Eye Signal Test Procedure

1. Connect the evaluation board and test equipment as described in Section 4.2.1, “Setting Up the Data-Eye Test Equipment,” and Section 4.2.1.1, “Parallel Input Connections.” This will place the MC92600 in full-speed, PN generation mode with the MC92600 in reset mode.
2. Apply +5.0 V to the evaluation board. Verify the 3.3 V voltage at the T5 connector and use the R12V potentiometer to adjust the voltage, if necessary. At the T8 connector, verify the 1.8 V voltage but use the R22V potentiometer to adjust the voltage, if necessary.
3. On the oscilloscope, observe the XMIT_*x*_P or XMIT_*x*_N output. Because the chip is in reset, the transmitter should show a constant level at ground.
4. Connect the $\overline{\text{RESET}}$ (connector CTRL_SIG_0, pin 11) to a +3.3-V access connection.
5. Observe XMIT_*x*_P or XMIT_*x*_N. The transmitter should now be outputting random data. Setting the digital sampling oscilloscope in infinite persistence mode will display a data-eye. An example of a full-speed data-eye is shown in Figure 4-2.

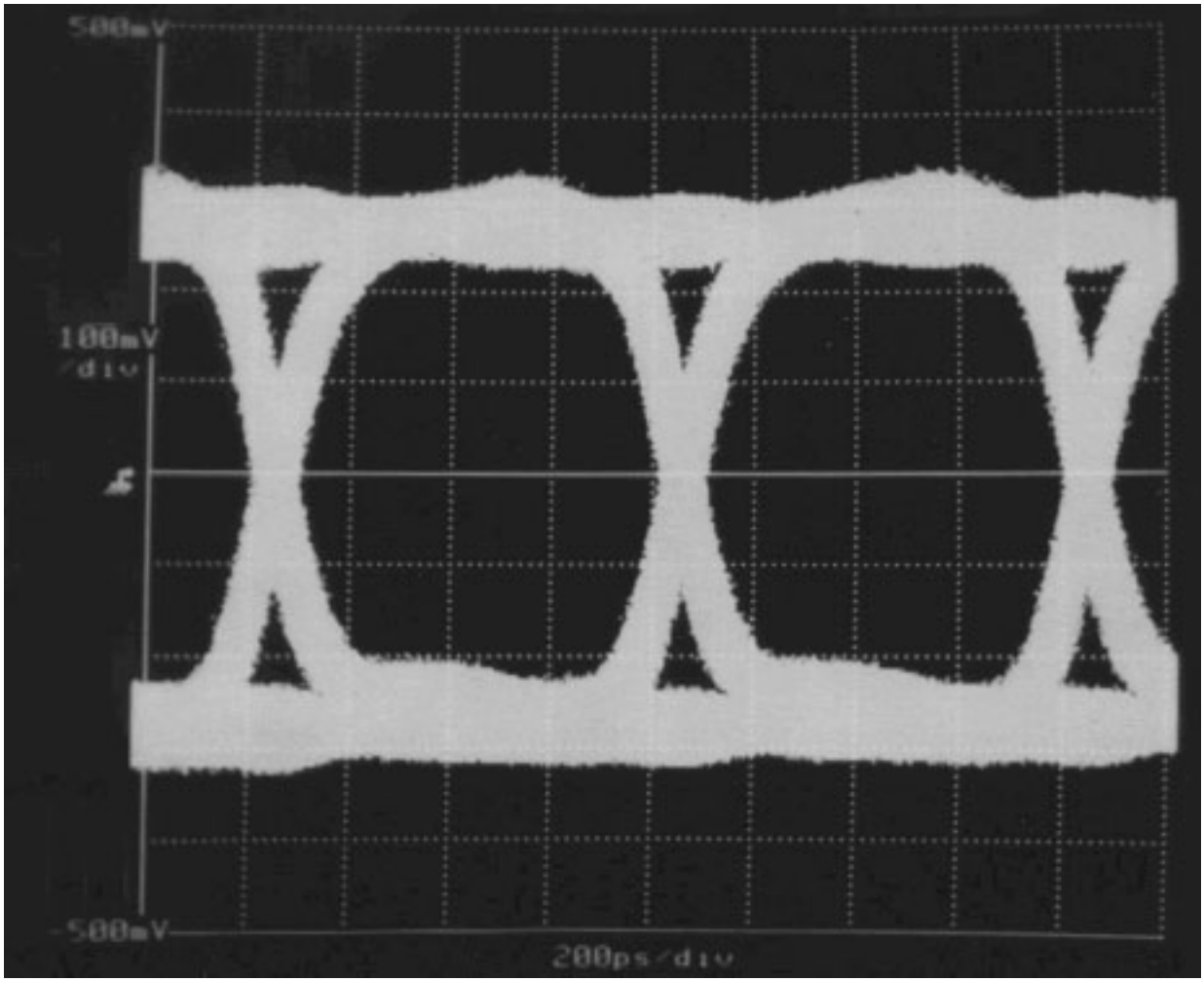

Figure 4-2. MC92600 Data-Eye Using Recommended Setup

4.3 Bit Error Rate Checking

In addition to having an integrated PN generator, the MC92600 also has an integrated bit error rate checker (BERC). The following test procedure will describe how to use this built-in self-test (BIST). For more information concerning the MC92600 BIST, refer to the *MC92600 Quad 1.25 Gbaud SerDes User's Manual*.

4.3.1 Setting Up the BERC Test Equipment

Connect the evaluation board as shown in Figure 4-3. All XMIT_*x*_P serial outputs must be connected to RECV_*x*_P serial inputs. All XMIT_*x*_N serial outputs must be connected to RECV_*x*_N serial inputs.

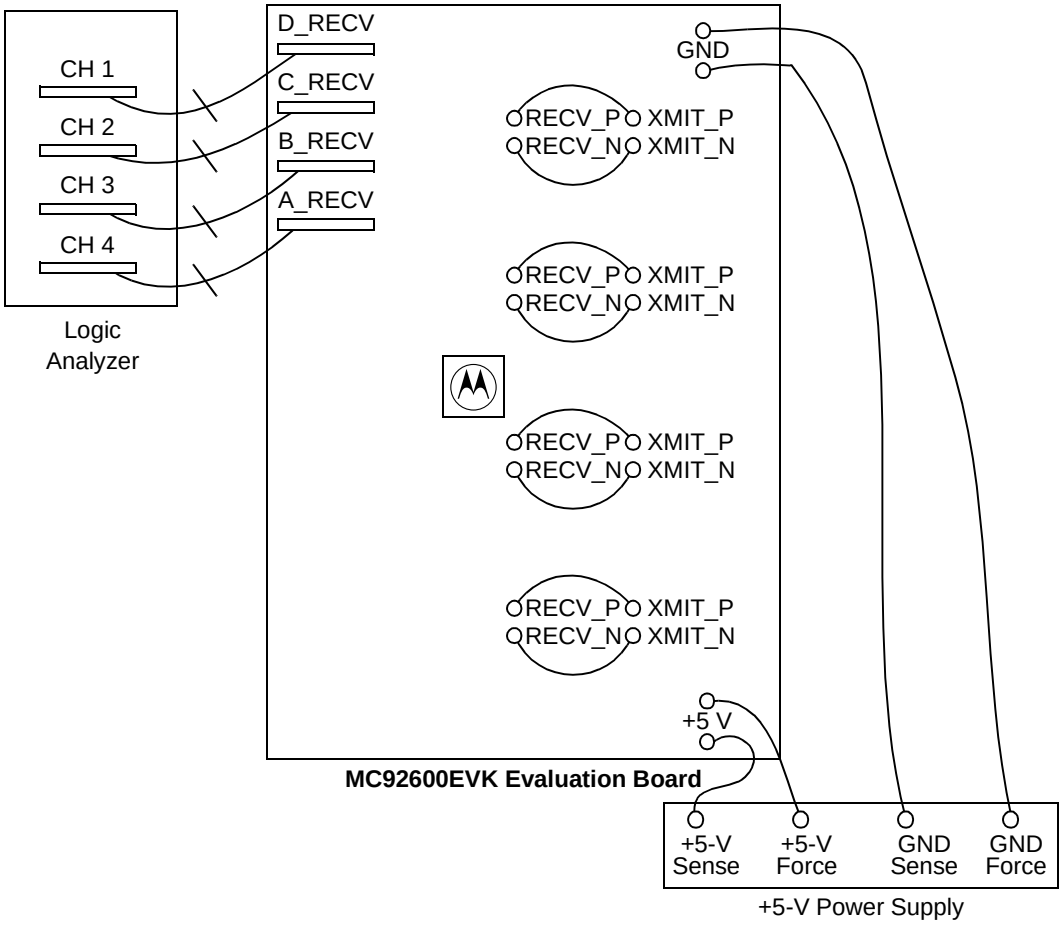

Figure 4-3. Bit Error Rate Check Test Setup

4.3.1.1 Parallel I/O Connections

All parallel inputs are connected as described in Table 4-2. The parallel outputs are connected to some type of digital data analysis system.

4.3.2 BERC Test Procedure

1. Connect the evaluation board and test equipment as described in Section 4.3.1, “Setting Up the BERC Test Equipment,” and Section 4.3.1.1, “Parallel I/O Connections.” This will place the MC92600 in full-speed, PN generation mode with the MC92600 in reset as well as set the receivers to BERC mode using the recovered clock.
2. Apply +5.0 V to the evaluation board. Verify the 3.3 V voltage at the T5 connector and use the R12V potentiometer to adjust the voltage, if necessary. At the T8 connector, verify the 1.8 V voltage but use the R22V potentiometer to adjust the voltage, if necessary.
3. Connect the $\overline{\text{RESET}}$ (connector CTRL_SIG_0, pin 11) to a +3.3 V access connection. This releases the $\overline{\text{RESET}}$ signal.
4. On the logic analyzer, observe the parallel outputs. As described in the *MC92600 Quad 1.25 Gbaud SerDes User’s Manual*, the MC92600 will start and lock its PLL, initialize the receivers and byte alignment, and reset its bit error counter.

   Table 4-3 shows the sequence of operational states with corresponding status bits that occur at each WarpLink receiver as the test procedure runs:

Table 4-3. State Sequence of Receiver

Receiver State		Status Outputs		
		RECV_*x*_ERR	RECV_*x*_K	RECV_*x*_IDLE
1.	Receiver in start-up	1	1	0
2.	Receiver byte/word synchronized, PN analyzer not locked.	1	0	1
3.	BIST running, no PN mismatch this character	0	0	0

5. Once the receiver has initially locked (RECV_*x*_ERR, RECV_*x*_K, RECV_*x*_IDLE) = 3'b000, all receiver data bits, RECV_*x*[7:0], are set to zero. Should an error occur, (RECV_*x*_ERR, RECV_*x*_K, RECV_*x*_IDLE) = 3'b100 for one RECV_*x*_RCLK clock cycle at the time of the error and RECV_*x*[7:0] will increment by one. The value of RECV_*x*[7:0] remains constant until another error is detected or the system is reset. Refer to the *MC92600 Quad 1.25 Gbaud SerDes User’s Manual* for more detail.

See Figure 4-4 for an example of a receiver start-up and error detection sequence.

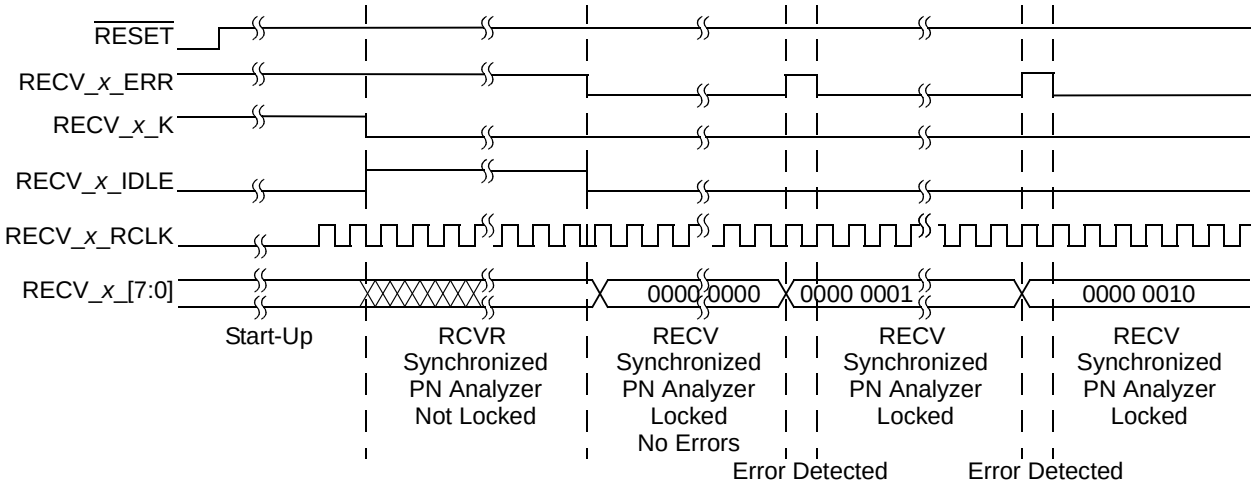

Figure 4-4. Receiver Start-Up and Error Detection Sequence

Appendix A
Connector Signals

The input and output signals of the MC92600EVK evaluation board's connectors are listed in the tables of this appendix.

A.1 Input: 2×10, 0.100" Connectors

The signals of connectors PG1–PG11 are contained in the tables below.

Table A-1 shows the signals for the PG1 connector.

Table A-1. PG1—CTRL_SIG_0, 2×10, 0.100" Connector to MC92600 Map

Connector Pin	MC92600 Pin		Input Signal Name	Description
	196 PBGA	217 BGA		
19	N/C	N/C	GND	Ground connection
17	N/C	N/C	—	—
15	C10	A14	STNDBY	Standby mode enable
13	D10	C14	DDRE	Double data rate enable
11	A11	B14	$\overline{\text{RESET}}$	System reset bar
9	C11	C15	ADIE	Add/drop idle enable
7	A12	B15	HSE	Half-speed mode enable
5	B12	B16	WSE	Word synchronization enable
3	C12	E14	RCCE	Recovered clock enable
1	A13	C16	REPE	Repeater mode enable

Table A-2 shows the signals for the PG2 connector.

Table A-2. PG2—CTRL_SIG_1, 2×10, 0.100" Connector to MC92600 Map

Connector Pin	MC92600 Pin		Input Signal Name	Description
	196 PBGA	217 BGA		
19	N/C	N/C	GND	Ground connection
17	N/C	N/C	—	—
15	N/C	N/C	—	—
13	N/C	N/C	—	—
11	N/C	N/C	—	—
9	N/C	N/C	—	—
7	N12	T15	TBIE	Ten-bit interface enable
5	N13	R16	MEDIA	Media impedance select
3	P13	R14	LBE	Loopback enable
1	P14	P13	LBOE	Loopback output enable

Table A-3 shows the signals for the PG3 connector.

Table A-3. PG3—CTRL_SIG_2, 2×10, 0.100" Connector to MC92600 Map

Connector Pin	MC92600 Pin		Input Signal Name	Description
	196 PBGA	217 BGA		
19	N/C	N/C	GND	Ground connection
17	N/C	N/C	—	—
15	N/C	N/C	—	—
13	N/C	N/C	—	—
11	N/C	N/C	—	—
9	M10	R12	WSE_GEN	Generate word synchronization event
7	N11	U14	TST_0	Test mode—select 0
5	L10	U13	TST_1	Test mode—select 1
3	M12	U15	BSYNC_1	Byte synchronization mode—select 1
1	P12	R13	BSYNC_0	Byte synchronization mode—select 0

Table A-4 shows the signals for the PG5 connector.

Table A-4. PG5—D_XMIT1, 2×10, 0.100" Connector to MC92600 Map

Connector Pin	MC92600 Pin		Input Signal Name	Description
	196 PBGA	217 BGA		
19	N/C	N/C	GND	Ground connection
17	N/C	N/C	—	—
15	N/C	N/C	—	—
13	N/C	N/C	—	—
11	N/C	N/C	—	—
9	N/C	N/C	—	—
7	N/C	N/C	—	—
5	N/C	N/C	—	—
3	E9	D13	$\overline{\text{XMIT\_D\_IDLE}}$	Transmitter D, idle enable bar (data bit 9 for ten-bit mode)
1	B10	B13	XMIT_D_K	Transmitter D, special character (data bit 8 for ten-bit mode)

Table A-5 shows the signals for the PG7 connector.

Table A-5. PG7—C_XMIT1, 2×10, 0.100" Connector to MC92600 Map

Connector Pin	MC92600 Pin		Input Signal Name	Description
	196 PBGA	217 BGA		
19	N/C	N/C	GND	Ground connection
17	N/C	N/C	—	—
15	N/C	N/C	—	—
13	N/C	N/C	—	—
11	N/C	N/C	—	—
9	N/C	N/C	—	—
7	N/C	N/C	—	—
5	N/C	N/C	—	—
3	B5	B6	$\overline{\text{XMIT\_C\_IDLE}}$	Transmitter C, idle enable bar (data bit 9 for ten-bit mode)
1	C6	A6	XMIT_C_K	Transmitter C, special character (data bit 8 for ten-bit mode)

Table A-6 shows the signals for the PG9 connector.

Table A-6. PG9—A_XMIT1, 2×10, 0.100" Connector to MC92600 Map

Connector Pin	MC92600 Pin		Input Signal Name	Description
	196 PBGA	217 BGA		
19	N/C	N/C	GND	Ground connection
17	N/C	N/C	—	—
15	N/C	N/C	—	—
13	N/C	N/C	—	—
11	N/C	N/C	—	—
9	N/C	N/C	—	—
7	N/C	N/C	—	—
5	N/C	N/C	—	—
3	P11	T14	$\overline{\text{XMIT\_A\_IDLE}}$	Transmitter A, idle enable bar (Data bit 9 for ten-bit mode)
1	N10	T13	XMIT_A_K	Transmitter A, special character (Data bit 8 for ten-bit mode)

Table A-7 shows the signals for the PG11 connector.

Table A-7. PG11—B_XMIT1, 2×10, 0.100" Connector to MC92600 Map

Connector Pin	MC92600 Pin		Input Signal Name	Description
	196 PBGA	217 BGA		
19	N/C	N/C	GND	Ground enables pod
17	N/C	N/C	—	—
15	N/C	N/C	—	—
13	N/C	N/C	—	—
11	N/C	N/C	—	—
9	N/C	N/C	—	—
7	N/C	N/C	—	—
5	N/C	N/C	—	—
3	N5	T5	$\overline{\text{XMIT\_B\_IDLE}}$	Transmitter b, idle enable bar (data bit 9 for ten-bit mode)
1	M6	U5	XMIT_B_K	Transmitter B, special character (data bit 8 for ten-bit mode)

Table A-8 shows the signals for the PG4 connector.

Table A-8. PG4—D_XMIT0, 2×10, 0.100" Connector to MC92600 Map

Connector Pin	MC92600 Pin		Input Signal Name	Description
	196 PBGA	217 BGA		
19	N/C	N/C	GND	Ground connection
17	N/C	N/C	—	—
15	A10	A13	XMIT_D_7	Transmitter D, data bit 7
13	B9	C13	XMIT_D_6	Transmitter D, data bit 6
11	A9	B12	XMIT_D_5	Transmitter D, data bit 5
9	D9	A12	XMIT_D_4	Transmitter D, data bit 4
7	B8	B11	XMIT_D_3	Transmitter D, data bit 3
5	A8	A11	XMIT_D_2	Transmitter D, data bit 2
3	C8	C11	XMIT_D_1	Transmitter D, data bit 1
1	D8	C10	XMIT_D_0	Transmitter D, data bit 0

Table A-9 shows the signals for the PG6 connector.

Table A-9. PG6—C_XMIT0, 2×10, 0.100" Connector to MC92600 Map

Connector Pin	MC92600 Ball		Input Signal Name	Description
	196 PBGA	217 BGA		
19	N/C	N/C	GND	Ground connection
17	N/C	N/C	—	—
15	D6	C7	XMIT_C_7	Transmitter C, data bit 7
13	A5	B7	XMIT_C_6	Transmitter C, data bit 6
11	B6	A7	XMIT_C_5	Transmitter C, data bit 5
9	A6	A8	XMIT_C_4	Transmitter C, data bit 4
7	C7	B8	XMIT_C_3	Transmitter C, data bit 3
5	D7	C8	XMIT_C_2	Transmitter C, data bit 2
3	B7	A10	XMIT_C_1	Transmitter C, data bit 1
1	A7	B10	XMIT_C_0	Transmitter C, data bit 0

Table A-10 shows the signals for the PG8 connector.

Table A-10. PG8—A_XMIT0, 2×10, 0.100" Connector to MC92600 Map

Connector Pin	MC92600 Pin		Input Signal Name	Description
	196 PBGA	217 BGA		
19	N/C	N/C	GND	Ground connection
17	N/C	N/C	—	—
15	P10	T12	XMIT_A_7	Transmitter A, data bit 7
13	N9	R11	XMIT_A_6	Transmitter A, data bit 6
11	P9	T11	XMIT_A_5	Transmitter A, data bit 5
9	L9	U11	XMIT_A_4	Transmitter A, data bit 4
7	N8	R10	XMIT_A_3	Transmitter A, data bit 3
5	P8	T10	XMIT_A_2	Transmitter A, data bit 2
3	M8	U10	XMIT_A_1	Transmitter A, data bit 1
1	L8	U8	XMIT_A_0	Transmitter A, data bit 0

Table A-11 shows the signals for the PG10 connector.

Table A-11. PG10—B_XMIT0, 2×10, 0.100" Connector to MC92600 Map

Connector Pin	MC92600 Pin		Input Signal Name	Description
	196 PBGA	217 BGA		
19	N/C	N/C	GND	Ground enables pod
17	N/C	N/C	—	—
15	L6	T6	XMIT_B_7	Transmitter B, data bit 7
13	P5	R6	XMIT_B_6	Transmitter B, data bit 6
11	N6	U6	XMIT_B_5	Transmitter B, data bit 5
9	P6	T7	XMIT_B_4	Transmitter B, data Bit 4
7	M7	U7	XMIT_B_3	Transmitter B, data bit 3
5	L7	R7	XMIT_B_2	Transmitter B, data bit 2
3	N7	T8	XMIT_B_1	Transmitter B, data bit 1
1	P7	R8	XMIT_B_0	Transmitter B, data bit 0

A.2 Output: 2×20, 0.100" Connectors

The signals of connectors LA1–LA4 are contained in Table A-12 through Table A-15.

Table A-12 shows the signals for the LA1 connector and Table A-13 shows the signals for the LA2 connector.

Table A-12. LA1—A_RECV, 2×20, 0.100" Connector to MC92600 Map

Connector Pin	MC92600 Pin		Output Signal Name	Description
	196 PBGA	217 BGA		
39	N/C	N/C	—	—
37	M1	N3	RECV_A_0	Receiver A, data bit 0
35	N1	R1	RECV_A_1	Receiver A, data bit 1
33	M2	T1	RECV_A_2	Receiver A, data bit 2
31	N2	P3	RECV_A_3	Receiver A, data bit 3
29	P1	N4	RECV_A_4	Receiver A, data bit 4
27	M5	R3	RECV_A_5	Receiver A, data bit 5
25	M3	T2	RECV_A_6	Receiver A, data bit 6
23	M4	T3	RECV_A_7	Receiver A, data bit 7
21	P2	U3	RECV_A_K	Receiver A, special character (data bit 8 for TBI mode)
19	N3	T4	RECV_A_9	Receiver A, data bit 9 for TBI mode
17	L5	R4	RECV_A_IDLE	Receiver A, idle detect
15	P4	R5	RECV_A_ERR	Receiver A, error detect
13	N/C	N/C	GND	Ground connection
11	N/C	N/C	GND	Ground connection
9	N/C	N/C	GND	Ground connection
7	N/C	N/C	GND	Ground connection
5	N/C	N/C	—	—
3	P3	U4	RECV_A_RCLK	Receiver A, receive data clock
1	N/C	N/C	—	—

Table A-13. LA2—B_RECV, 2×20, 0.100" Connector to MC92600 Map

Connector Pin	MC92600 Pin		Output Signal Name	Description
	196 PBGA	217 BGA		
39	N/C	N/C	—	—
37	K3	P2	RECV_B_0	Receiver B, data bit 0
35	L4	P1	RECV_B_1	Receiver B, data bit 1
33	L1	M3	RECV_B_2	Receiver B, data bit 2
31	J3	N1	RECV_B_3	Receiver B, data bit 3
29	K4	M2	RECV_B_4	Receiver B, data bit 4
27	K2	L3	RECV_B_5	Receiver B, data bit 5
25	K1	M1	RECV_B_6	Receiver B, data bit 6
23	H3	L2	RECV_B_7	Receiver B, data bit 7
21	J4	L1	RECV_B_K	Receiver B, special character (data bit 8 for TBI mode)
19	J1	J3	RECV_B_9	Receiver B, data bit 9 for TBI mode
17	G3	K1	RECV_B_IDLE	Receiver B, idle detect
15	H2	J2	RECV_B_ERR	Receiver B, error detect
13	N/C	N/C	GND	Ground connection
11	N/C	N/C	GND	Ground connection
9	N/C	N/C	GND	Ground connection
7	N/C	N/C	GND	Ground connection
5	N/C	N/C	—	—
3	H4	K2	RECV_B_RCLK	Receiver B, receive data clock
1	N/C	N/C	—	—

Table A-14 shows the signals for the LA3 connector.

Table A-14. LA3—C_RECV, 2×20, 0.100" Connector to MC92600 Map

Connector Pin	MC92600 Pin		Output Signal Name	Description
	196 PBGA	217 BGA		
39	N/C	N/C	—	—
37	C1	D1	RECV_C_0	Receiver C, data bit 0
35	D2	D3	RECV_C_1	Receiver C, data bit 1
33	D4	E2	RECV_C_2	Receiver C, data bit 2
31	E2	E3	RECV_C_3	Receiver C, data bit 3
29	E3	F2	RECV_C_4	Receiver C, data bit 4
27	F4	F1	RECV_C_5	Receiver C, data bit 5
25	E1	G2	RECV_C_6	Receiver C, data bit 6
23	F2	F3	RECV_C_7	Receiver C, data bit 7
21	F1	G1	RECV_C_K	Receiver C, special character (data bit 8 for TBI mode)
19	F3	H2	RECV_C_9	Receiver C, data bit 9 for TBI mode
17	G2	J1	RECV_C_IDLE	Receiver C, idle detect
15	H1	H3	RECV_C_ERR	Receiver C, error detect
13	N/C	N/C	GND	Ground connection
11	N/C	N/C	GND	Ground connection
9	N/C	N/C	GND	Ground connection
7	N/C	N/C	GND	Ground connection
5	N/C	N/C	—	—
3	G1	H1	RECV_C_RCLK	Receiver C, receive data clock
1	N/C	N/C	—	—

Table A-15 shows the signals for the LA4 connector.

Table A-15. LA4—D_RECV, 2×20, 0.100" Connector to MC92600 Map

Connector Pin	MC92600 Pin		Output Signal Name	Description
	196 PBGA	217 BGA		
39	N/C	N/C	—	—
37	D3	D2	RECV_D_0	Receiver D, data bit 0
35	E4	C3	RECV_D_1	Receiver D, data bit 1
33	B1	C1	RECV_D_2	Receiver D, data bit 2
31	C2	B1	RECV_D_3	Receiver D, data bit 3
29	A1	C2	RECV_D_4	Receiver D, data bit 4
27	C5	B3	RECV_D_5	Receiver D, data bit 5
25	C3	A3	RECV_D_6	Receiver D, data bit 6
23	C4	B4	RECV_D_7	Receiver D, data bit 7
21	A2	C4	RECV_D_K	Receiver D, special character (data bit 8 for TBI mode)
19	B3	C5	RECV_D_9	Receiver D, data bit 9 for TBI mode
17	D5	B5	RECV_D_IDLE	Receiver D, idle detect
15	A4	C6	RECV_D_ERR	Receiver D, error detect
13	N/C	N/C	GND	Ground connection
11	N/C	N/C	GND	Ground connection
9	N/C	N/C	GND	Ground connection
7	N/C	N/C	GND	Ground connection
5	N/C	N/C	—	—
3	A3	A4	RECV_D_RCLK	Receiver D, receive data clock
1	N/C	N/C	—	—

Appendix B
Parts List

B.1 Evaluation Board Parts List

Table B-1 shows the parts used in constructing the MC92600EVK evaluation board.

Table B-1. MC92600EVK Evaluation Board Parts List

Item	Qty	Reference	Value	Manufacturer	Manufacturer's Part No.	Description
1	13	C30–C33, C54–C57, C208–C210, C303–C304	1 µF	Bourns	C1812C105KRACTR	Ceramic chip capacitor, 1 µF, size 1812
2	2	C11, C21	100 µF	Kemet	T495D107K010AS	100 µF solid tantalum chip capacitor, low ESR, 10 V, size 7343
3	4	C13, C12, C22 µC23	10 µF	Kemet	T495X106K035AS	10 µF solid tantalum chip capacitor, low ESR, 35 V, size 7343H
4	1	C305	22 µF	Kemet	T491D226K020A5	22 µF solid tantalum chip capacitor, low ESR, size 7343
5	4	C1, C10, C20, C306	0.1uF	Kemet	C0805C104K5RACTR	Ceramic chip capacitor, 0.1 µF, size 0805
6	30	C2, C34 µC53, C201 µC207 C301 µ302	0.01uF	Kemet	C0805C103K5RACTR	Ceramic chip capacitor, 0.01 µF, size 0805
7	1	Y1	20MHz	Raltron	AS-20.000-18-FUND-SMD	20-MHz surface mount quartz crystal
8	1	SW2	N/A	Omron	A6S-6104	6-pole DIP slide switches, 2 position (open or closed), surface mount
9	1	SW1	N/A	Omron	A6S-7104	7-pole DIP slide switches, 2 position (open or closed), surface mount
10	12	PG1 µPG11	N/A	3M	3428-6002	2×10 keyed header with shroud, 0.1" pin spacing

Table B-1. MC92600EVK Evaluation Board Parts List (continued)

Item	Qty	Reference	Value	Manufacturer	Manufacturer's Part No.	Description
11	4	LA1–LA4	N/A	3M	2540-6002UB	2×20 keyed header with shroud, 0.1" pin spacing, low profile
12	1	D1	N/A	Dialight	551-1307	Green 2 mA LED
13	2	VR18, VR33	N/A	Linear Technology	LT1587CM	Linear voltage regulator, 3 amps, 3-lead DD pak
14	1	U3	N/A	Motorola	MC12429	Frequency synthesizer, 28-pin J lead PLCC
15	1	U2	N/A	Motorola	MPC948	Level shift and clock buffer, 32-pin gull wing TQFP
18	8	T1–T8	N/A	SPC Technology	2304/2303	4-mm screw terminal binding post, red/black
19	3	R5–R6, R23	82 Ω	SPC/ Multicomp	CR16B820JT	82-Ω chip resistor, size 0603
20	3	R1–R2, R8	20 Ω	Newark	CR10-470JT-612935	47-Ω chip resistor, size 0805
21	4	R4, R3, R10, R20	124 Ω	Dale	CRCW08051240FT	124-Ω chip resistor, size 0805
22	2	R13, R11	330 Ω	Welwyn	WCR0805330RG	330-Ω chip resistor, size 0805
23	1	R21	68 Ω	Dale	CRCW0805680JRT1	68-Ω chip resistor, size 0805
24	1	R7	10 Ω	Dale	CRCW1206xxxx	10-Ω chip resistor, size 1206
25	2	R9, R14	470 Ω	Dale	CRCW1206xxxx	470-Ω chip resistor, size 1206
26	1	R33	3.9 Ω	Dale	CRCW12063R9JT	3.9-Ω chip resistor, size 1206
27	1	TPA	N/A	Johnson	129-0701-202	Scope PCB test socket
28	27	CLK_IN, CLK_OUT1–2, SMA1–16, TST1–8	N/A	Amp	221789-1	SMA 50-Ω RF PCB jack socket
29	1	R12V	1 kΩ	BOURNS	3214W-1-102E	Surface mount trimming resistor, J lead
30	1	R22V	500 Ω	BOURNS	3214W-1-501E	Surface mount trimming resistor, J lead
31	1	U4	N/A	Motorola	MC92600	217 PBGA or 196 FBGA
32	50	N/A	N/A	3M	929950-00	0.100” shunts
33	12	N/A	N/A	Pomona	4741-12-0 4741-12-2	Square pin receptacle patch cord
34	1	PG12	N/A	3M	2516-6002UB	2×8 keyed header with shroud, 0.1" pin spacing, low profile

Appendix C
Revision History

This appendix provides a list of the major differences between revisions of the *MC92600 Quad SerDes Evaluation Kit User's Guide* (MC92600EVKUG).

Table C-1 provides a revision history for this document.

Table C-1. MC92602DVB Revision History

Rev. No.	Date	Substantive Change(s)
0.2	12/15/1999	Full document revision.
0.3	12/20/1999	Added WSE_GEN under entry CTRL_SIG2 in Table 18.
1.0	2/9/2000	• Corrected package designations. • Corrected EVB trace impedance range. • Updated Section 3 to demonstrate REF_CLK = 125 MHz. • Updated Section 8 for full-speed testing. • Updated Appendix B for full-speed testing.
1.1	3/2/2000	Updated Section 4.3 to reflect change in connector from 2×10, 0.100″ connector to 2×8, 0.100″ connector. • Updated Table 17 to reflect change in connector. • Updated Appendix B to reflect additional connector. • Added 2 attenuators to Section 7.1 as recommended by DSO manufacturer. • Added 2 attenuators to Figure 5, Section 8.1.1. • Updated Figure 6, Section 8.1.3 to show data-eye with addition of attenuators.
2	4/2004	Removed references to WarpLink and reformatted for new release.

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