MPC5748G Low Cost EVB User Guide (MPC5748G-LCEVB)
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MPC5748G Low Cost EVB User Guide, Rev. 1, 08/2016

NXP Semiconductors
1. Introduction

This user guide details the setup and configuration of the NXP MPC5748G Low Cost Evaluation Board (hereafter referred to as the LCEVB). The LCEVB is intended to provide a mechanism for easy evaluation of the MPC5748G family of microcontrollers, and to facilitate basic hardware and software development.

Note that the LCEVB has a limited feature set compared to the main MPC574xG customer EVB and is intended for evaluation purposes. Customers moving to serious development activities are recommended to purchase the fully functional customer EVB which also has device specific daughter cards.

The LCEVB is intended for bench / laboratory use and has been designed using normal temperature specified components (+70° C).

This product contains components that may be damaged by electrostatic discharge. Observe precautions for handling electrostatic sensitive devices when using the LCEVB.

The user guide is intended to be read alongside the respective MCU documentation available at www.nxp.com and includes:

- Reference Manuals
- Product Data Sheets
- Application notes
- Device Errata

2. LCEVB Features

The LCEVB provides the following key features:

- Single 5 V DC external power supply input with on-board 3.3 V regulator. Power is supplied via a 2.1 mm barrel style power jack.
- Simple jumper less configuration (enhanced configuration is possible via 0 Ohm Resistors and optional jumpers if required).
- Master power switch and regulator status LED.
- USB Serial interface.
- 2 x High Speed CAN transceiver routed to 3-way headers.
- 2 x LIN interfaces routed to 3-way headers.
- Main clock supplied from on board crystal.
- User reset switch with reset status LED’s.
- Ethernet PHY and RJ45 socket (configured for MII mode).
- USB Type A Host interface.
- 2 x FlexRay interfaces with standard 2-pin connectors.
- 14-pin JTAG connector.
• 4 user LED’s wired to MCU ports.
• 2 user pushbutton switches wired to MCU ports.
• Hexadecimal encoded switch wired to 4 MCU ports.
• Simple potentiometer connected to analogue input channel.

2.1. Differences to the Customer EVB

Note that the GPIO pins used for peripherals on the LCEVB are the same as those used on the customer EVB. This ensures maximum code compatibility between the 2 boards, making it easy to migrate from one board to the other.

Table 1. Customer EVB vs LCEVB features

<table>
<thead>
<tr>
<th>Feature</th>
<th>Customer EVB</th>
<th>LCEVB</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCU Support</td>
<td>Custom MCU Daughter cards for multiple devices (socketed)</td>
<td>Soldered 176QFP MPC5748G</td>
</tr>
<tr>
<td>Power Supply</td>
<td>External 12 V</td>
<td><strong>External 5 V (Caution)</strong></td>
</tr>
<tr>
<td>On Board Regulators (and LED’s)</td>
<td>5 V, 3.3 V, 1.25 V (combination of Linear and /or Switching regulators)</td>
<td>3.3 V Switching Regulator</td>
</tr>
<tr>
<td>Master Power Switch</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Reset Control</td>
<td>Reset button with MCU and External Reset LED’s</td>
<td>Reset button with MCU and External Reset LED’s</td>
</tr>
<tr>
<td>USB FTDI Serial Interface</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>CAN Physical Interfaces</td>
<td>2 (routed to 0.1” headers)</td>
<td>2 (routed to 0.1” headers)</td>
</tr>
<tr>
<td>LIN Physical Interfaces</td>
<td>2 (routed to Molex headers)</td>
<td>2 (routed to 0.1” headers)</td>
</tr>
<tr>
<td>FlexRay Physical Interfaces</td>
<td>2 (routed to 0.1” headers)</td>
<td>2 (routed to 0.1” headers)</td>
</tr>
<tr>
<td>Ethernet Physical Interface</td>
<td>1 (MII and RMII Support)</td>
<td>1 (MII only mode)</td>
</tr>
<tr>
<td>USB Physical Interface</td>
<td>2 (USB Host and OTG)</td>
<td>1 (USB Host)</td>
</tr>
<tr>
<td>MLB Daughter card Connector</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>SAI Audio / TWRPI Connectors</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>SDHC Connector</td>
<td>Full Size SDHC Socket</td>
<td>No</td>
</tr>
<tr>
<td>Fast External Osc (FXOSC)</td>
<td>Daughter card Crystal * and SMA input connector</td>
<td>40 MHz Crystal</td>
</tr>
<tr>
<td>Slow External Osc (SXOSC)</td>
<td>Daughter card Crystal *</td>
<td>32.768 KHz Crystal</td>
</tr>
<tr>
<td>CLKOUT signals available</td>
<td>Yes (GPIO Matrix)</td>
<td>Yes (Standalone pads)</td>
</tr>
<tr>
<td>User LEDS</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>User Pushbutton Switches</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>Hex Encoded Switch</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Test Potentiometer for ADC</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>GPIO Matrix</td>
<td>All Available Pins not otherwise used for peripherals</td>
<td>Selection of Pins available from 5 GPIO Ports</td>
</tr>
<tr>
<td>Debug</td>
<td>14 Pin JTAG and 50 pin Nexus</td>
<td>14 Pin JTAG</td>
</tr>
<tr>
<td>Configuration</td>
<td>Highly configurable via jumper shunts</td>
<td>Fixed (limited configuration via 0 ohm resistors)</td>
</tr>
</tbody>
</table>

* Daughter card crystals are typically 40 MHz for FXOSC and 32.768 KHz for SXOSC but may vary between daughter cards.
The figure below shows the customer EVB (left) next to the LCEVB (right).

Figure 1. Customer and LCEVB side by side
3. Configuration Overview

Out of the box, there is no configuration required for the LCEVB to function. Unlike the customer EVB, the LCEVB is primarily designed for a single mode of operation with no requirement for user configuration. If you wish to have a more flexible configuration the recommendation is that the fully configurable customer EVB is purchased.

There are however some jumper footprints and zero ohm resistors populated in positions that would normally have jumper headers fitted (for example on the MCU power supply lines and tracking to the peripheral interfaces). If required these can be de-soldered to modify functionality. Any such modification is done at the full risk of the user and no support or warranty repairs will be provided for a board that has been modified. Modifications should only be attempted by appropriately trained personnel using the correct equipment and Personal Protective Apparel.

The diagram below gives an overview of the functional blocks of the LCEVB.

![Figure 2. EVB Functional Blocks](image-url)
4. Initial Setup

This section details the power, reset, clocks, and debug configuration which is the minimum configuration needed in order to power ON the LCEVB.

4.1. Power Supply Configuration

The LCEVB requires an external power supply voltage of 5 V DC, minimum 1 A. There is a single 3.3 V switching regulator on the LCEVB providing MCU and peripheral power.

**CAUTION**

Connecting a power supply with a voltage greater than 5 V will result in irrecoverable board damage. Check the power supply voltage before connecting the plug to the LCEVB.

4.1.1. Power Input Connector

Power is supplied to the LCEVB via a 2.1 mm connector from the wall-plug mains adapter as shown below. Note – if a replacement or alternative adapter is used, care must be taken to ensure the 2.1 mm plug uses the correct polarization as shown below:

**Figure 3. 2.1 mm Power Connector**

4.1.2. Power Switch

Slide switch SW2 can be used to isolate the power supply input from the EVB voltage regulators if required.

- Moving the slide switch to the right (away from the power connector) will turn the EVB ON.
- Moving the slide switch to the left (towards the power connector) will turn the EVB OFF.
4.1.3. Power Status LED

When power is applied to the LCEVB, two green LED’s adjacent to the regulator and power connector show the presence of the supply voltages as follows:

- LED DS5 – Indicates that the 5.0 V supply voltage is present
- LED DS6 – Indicates that the 3.3 V switching regulator is functioning

If no LED’s are illuminated when power is supplied to the LCEVB and the power switch is in the “ON” position, the power adapter may be faulty or there may be a fault with the LCEVB. If only one LED is illuminated there may be a short in that power supply rail – check there is nothing shorting on the EVB. If you continue to have problems, contact NXP for support.

**CAUTION**

In the event of a short on the regulator output (in which case one of the LED’s would be off or dimly illuminated), the regulator and/or the shorted component will likely be hot.

4.1.4. MCU and Peripheral Voltage Configuration

The following MCU supply rails are connected to the 3.3 V switching regulator:

- VDD_HV_ADC0
- VDD_HV_ADC1
- VDD_HV_ADC1_REF
- VDD_HV_A
- VDD_HV_B
- VDD_HV_FLA
- External Ballast Transistor Supply

Similarly all of the peripheral interfaces (or the I/O power in the peripheral interface) are supplied from 3.3 V as is the reset circuitry and the voltage sense wire on the JTAG connector.

4.2. Reset Control (SW3)

The MCU has a single bi-directional open drain Reset pin. Rather than connect multiple devices to the reset pin directly, a reset-in and reset-out buffering scheme has been implemented on the LCEVB as shown in Figure 4. The reset “in” from the reset switch (SW3) and the debug connectors are logically OR’d together using an AND gate and then connected to the buffer to provide an open-drain output.

The “reset-out” circuitry provides a buffered reset signal that can be used to drive any circuitry requiring a reset control from the MCU.
This scheme is not required if it is guaranteed that anything driving the reset pin has an open drain drive and that there is no significant output load on the MCU reset pin.

**4.2.1. Reset LEDs**

As can be seen above, there are two reset LED’s that can be used to identify the source / cause of a reset:

**RED LED DS8 (titled “MCU”)** will illuminate if:

- The MCU issues a reset (in this condition ONLY this LED will be illuminated and LED DS1 will be off)
- There is a target reset (i.e. from the reset switch or from the debugger in which case LED DS1 will be ON)

**YELLOW LED DS7 (titled “EXT”)** will illuminate when an external hardware device issues a reset to the MCU:

- The reset switch is pressed
- There is a reset being driven from one of the debug connectors

<table>
<thead>
<tr>
<th>LED DS7 (Yellow)</th>
<th>LED DS8 (Red)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFF</td>
<td>OFF</td>
<td>No Reset being issued from MCU or external logic</td>
</tr>
<tr>
<td>OFF</td>
<td>ON</td>
<td>MCU has issued a reset</td>
</tr>
<tr>
<td>ON</td>
<td>OFF</td>
<td>External reset issued from switch or debug BUT not being issued to MCU (check R137 has not been removed)</td>
</tr>
<tr>
<td>ON</td>
<td>ON</td>
<td>External reset issued from reset switch or debug and has been issued to MCU.</td>
</tr>
</tbody>
</table>
4.3. MCU Clock Configuration

There is an external 40MHz crystal connected to the MCU Fast External Oscillator (FXOSC) pins EXTAL and XTAL.

There is also a 32.768 crystal connected to the MCU Slow External Oscillator (SXOSC) pins OSC32K_EXTAL and OSC32K_XTAL. This can be used for accurate time keeping.

There are 2 pads PG6 and PG7 (located just below the MCU) on the LCEVB to facilitate measurement of the CLKOUT1 and CLKOUT0 signals.

Note – there is no external clock input on the LCEVB

4.4. Debug Connector (P1)

The LCEVB has a single 14-pin keyed JTAG connector for connection to an external debugger.

Before attaching or removing the debug cable from the LCEVB remove power from the EVB to prevent damage to the LCEVB or debug hardware.

4.4.1. Debug Connector Pinout

The following tables list the pinout for the JTAG connector used on the LCEVB

<table>
<thead>
<tr>
<th>Pin No</th>
<th>Function</th>
<th>Connection</th>
<th>Pin No</th>
<th>Function</th>
<th>Connection</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>TDI</td>
<td>PC0</td>
<td>2</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>TDO</td>
<td>PC1</td>
<td>4</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>5</td>
<td>TCLK</td>
<td>PH9</td>
<td>6</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>7</td>
<td>EVTI</td>
<td>PL8</td>
<td>8</td>
<td>N/C</td>
<td>---</td>
</tr>
<tr>
<td>9</td>
<td>RESET</td>
<td>JTAG – RSTx</td>
<td>10</td>
<td>TMS</td>
<td>PH10</td>
</tr>
<tr>
<td>11</td>
<td>VREF</td>
<td>PER_HVA</td>
<td>12</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>13</td>
<td>RDY</td>
<td>---</td>
<td>14</td>
<td>JCOMP</td>
<td>10k Pulldown</td>
</tr>
</tbody>
</table>

TDI, TDO and TMS have 10K pullup resistors on the LCEVB. TCLK has a 10K pulldown (R147) to facilitate STANDBY exit without any additional code (at the sacrifice of slightly higher STANDBY current), however this can be changed to a pullup if required by removing R147 and fitting the resistor on R56.
### 5. Communications & Memory Interfaces:

This section details the communication interface and storage peripherals that are implemented on the LCEVB.

#### 5.1. CAN Interfaces (P2, P3)

The LCEVB incorporates two identical CAN interface circuits connected to MCU CAN0 and CAN1 using MC33901 transceivers. Both transceivers are configured for high speed operation by pulling pin 8 to GND via a 4.7 kOhm resistor. There are test points to allow the Select pin to be driven high if desired. The MC33901 is pin compatible with other CAN transceivers supporting full CAN FD data rates.

For flexibility, the CAN transceiver I/O is connected to a 0.1” header (P2 for CAN0 / P3 for CAN1) rather than using non-standard DB9 connectors. The pinout of these headers is shown below.

![Figure 5. CAN Physical Interface Connectors](image-url)
5.2. LIN Interfaces (P6, P7)

The LCEVB incorporates two LIN transceiver circuits connected to MCU LIN0 and LIN1, using an NXP MC33662 transceiver. The MPC5748G LIN0 supports both master and slave modes whereas LIN1 only supports master mode.

On the LCEVB, the LIN0 transceiver is configured as slave mode by default. Master mode operation is possible by either populating a zero ohm resistor (R143) or by fitting a jumper header (J2) – see the schematics for details. The LIN0 transceiver is hard wired for master mode. To save on board space and cost, both LIN transceivers are connected to 0.1” pitch 3x1 headers as shown below rather than the usual LIN Molex header.

![Figure 6. LIN Physical Interface Connector](image)

Note that in order for the LIN transceiver to function, external 12v must be supplied via pin 2 of the connector.

5.3. USB RS232 Serial Interface (P11)

The LCEVB incorporates a USB RS232 serial interface providing RS232 connectivity via a direct USB connection between the PC and the EVB. The circuit contains an FTDI FT2232D USB to Serial interface which should automatically install the drivers for two additional COM ports on your PC. Note that only one of these ports is used so you will need to try both (usually the higher numbered COM port is the active one). For more information on the USB drivers and general fault finding, consult the FTDI website at [http://www.ftdichip.com/](http://www.ftdichip.com/)

The MCU LIN2 signals are routed to the FTDI transceiver (UART TX and RX). No handshaking signals are implemented and no board configuration is required.

5.4. USB HOST Interface (P4)

The LCEVB includes a Type A (Host) USB interface, routed to a USB type A female connector. The USB circuit contains a USB83340 transceiver with a MIC2026-1YM USB power switch. There is no hardware user configuration required to use the USB circuit.
5.5. Ethernet Interface (P5)

The EVB incorporates a single DP83848c Ethernet transceiver with the circuitry configured for MII mode. The transceiver is connected to a pulse J1011F21PNL RJ45 connector which includes a built-in isolation transformer. There is no hardware configuration needed.

If you require RMII mode or access to both Ethernet ports on the MPC5748G, please purchase the MPC5748G customer EVB and appropriate daughter cards.

Note that the MCU Ethernet signals are all in the VDD_HV_B domain. The Ethernet PHY will only function with 3.3 V I/O so if you have made any modifications to the EVB power domain configuration (via the zero ohm resistors), you need to ensure the VDD_HV_B domain is at 3.3 V before attempting to use the Ethernet module. If VDD_HV_B is set to 5 V, the signals routed to the Ethernet PHY (see the EVB schematics) must be left as tristate to prevent damage to the transceiver.

5.6. FlexRay (P8, P9, P10)

The LCEVB incorporates two FlexRay TJA1080TS/N interfaces connected to MCU FlexRay channels A and B and routed to two Molex 1.25 mm pitch Pico Blade shrouded headers (standard on many NXP EVB’s). There is no hardware configuration required to use FlexRay.

Note that the LCEVB is supplied with a 40 MHz crystal by default. If FlexRay is configured to use the external clock source, then the crystal should be left at 40 MHz.
6. User Interface (I/O)

This section details the user I/O available on the LCEVB and includes the GPIO matrix, switches, LED’s and the ADC variable resistor.

6.1. GPIO Matrix

A sub-set of available GPIO pins (available pins being those not already routed to LCEVB peripherals) are available at the GPIO matrix as detailed below. The matrix provides an easy to follow, intuitive, space saving grid of 0.1” header through-hole pads. Users can solder wires, fit headers or simply insert a scope probe into the respective pad.

To use the matrix, simply read the port letter from the top or bottom row of text then the pad number from the columns on the left or right of the matrix. For example, the 1st pad available on Port B is PB5 as outlined below.

If a pad is populated in the matrix, it means this is available for exclusive use as GPIO. The exception to this are the port pins detailed below which are also shared with switches or user LED’s (shaded red in the matrix diagram above).

PD0, PD1, PD2, PD3 – HEX Encoder Switch
PA1, PA2 – User pushbutton Switches

If you require access to all of the available GPIO pads, the customer EVB and daughter card provides this additional functionality.
6.2. User Switches (SW4, SW5)

There are two active high (pulled low, driven to 3.3 V) pushbutton switches on the LCEVB connected directly to MCU GPIO ports. No configuration is required to use the switches.

SW4 is connected to port PA1 (which is also the NMI pin) and SW5 is connected to port PA2

NOTE

The MCU ports used on the user pushbutton switches are also routed to the GPIO matrix.

6.3. Hex Encoded Switch (SW1)

There is a single hex encoded 16 position rotary switch on the LCEVB. This outputs a binary encoded hex value (active high) on four MCU ports (Port D[0..3]).

<table>
<thead>
<tr>
<th>Position</th>
<th>HEX_SW4 (PD3)</th>
<th>HEX_SW3 (PD2)</th>
<th>HEX_SW2 (PD1)</th>
<th>HEX_SW1 (PD0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
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<tr>
<td>7</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>9</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>A</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>B</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>C</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>D</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>E</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>F</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Note that POSN 0 will ensure that no voltage is applied to the pads. This allows the pads to be used as normal GPIO (with 10K pulldown) and accessed at the respective pads on the GPIO matrix area.
6.4. User LED’s (DS1, DS2, DS3, DS4)

There are four **active low** user LED’s, DS1 to DS4, connected directly to 4 MCU ports (PG[2..5]) as shown below. No configuration is required to use the LED’s.

<table>
<thead>
<tr>
<th>User LED</th>
<th>MCU Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>DS1</td>
<td>PG2</td>
</tr>
<tr>
<td>DS2</td>
<td>PG3</td>
</tr>
<tr>
<td>DS3</td>
<td>PG4</td>
</tr>
<tr>
<td>DS4</td>
<td>PG5</td>
</tr>
</tbody>
</table>

6.5. ADC Input Potentiometer (RVAR, RV1)

There is a small variable resistor RV1 on the LCEVB which routes a voltage between 0v and 3.3 V to MCU pin PB4. This is useful for quick ADC testing. Test point RVAR can be used to probe the voltage with a voltmeter.

Note that this circuit provides a very rough way to evaluate the ADC. There is a small current limiting series resistor network to limit the injection current to around 4.4 mA.
# 7. MCU Port Pin LCEVB Functions

The table below shows what each MCU pin is used for on the LCEVB.

## Table 7. LCEVB 176QFP Port Pin Functions

<table>
<thead>
<tr>
<th>No</th>
<th>Port A</th>
<th>Port B</th>
<th>Port C</th>
<th>Port D</th>
<th>Port E</th>
<th>Port F</th>
<th>Port G</th>
<th>Port H</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>GPIO</td>
<td>CAN0</td>
<td>JTAG</td>
<td>GPIO</td>
<td>---</td>
<td>GPIO</td>
<td>Ethernet</td>
<td>Ethernet</td>
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### Key:
- **---** Pin not bonded out on 176QFP package
- **Pin not accessible on LCEVB**

2 Shared with user switches
3 Shared with Hex Encoder Switch
4 Shared with user LED’s
8. Appendix

The MPC5748G LCEVB schematics, Rev B are shown below.
Table Of Contents:

- Power - Main input and 3.3V regulator
- Power - MCU Power
- Power - MCU Decoupling
- Reset and JTAG
- Clocks
- MCU GPIO 1
- MCU GPIO 2
- Comms1 - CAN and LIN
- Comms 2 - FTDI RS232 Interface
- Comms 3 - USB Host Interface (device footprints only)
- Comms 4 - Ethernet (MII Mode)
- Comms 5 - FlexRay
- User - Switches, LED's and Potentiometer
- User - GPIO Pin Matrix

Revised NXP Logos

Caution:
These schematics are provided for reference purposes only. As such, NXP does not make any warranty, implied or otherwise, as to the suitability of circuit design or component selection (type or value) used in these schematics for hardware design using the NXP Calypso family of Microprocessors. Customers using any part of these schematics as a basis for hardware design, do so at their own risk and NXP does not assume any liability for such a hardware design.

Notes:
- All components and board processes are to be ROHS compliant
- All small capacitors are 0402 unless otherwise stated
- All resistors are 0603 5% 0.1w unless otherwise stated. All zero ohm links are 0603
- All connectors and headers are denoted Px and are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
- All switches are denoted SWx
- 2 Pin jumpers generally have the "source" on pin 1.
- Two point Vias (just through hole pads) are denoted TPVx
- User notes are given throughout the schematics.

Specific PCB LAYOUT notes are detailed in ITALICS

Signals (ports) have not been routed via busses as this makes it harder to determine where each signal goes.

User notes are given throughout the schematics.

3 Different test points used in design:
- TPVx - Through Hole Pad small
- TPHx - Through Hole Pad Large (for standard 0.1" header).
- TPX - Surface Mount Wire Loop

User notes are given throughout the schematics.

Specific PCB LAYOUT notes are detailed in ITALICS

Consult the Design Guide, Rev 2.x, for unit pinout examples and footprint guidance.

Notes are given throughout the schematics.
Power Supply Input

Power Control

Jumpers can be fitted to facilitate power measurements

3.3v Switching Regulator

Input Voltage 5V, Output 3.3V at 700mA. Ripple 1.4mV, Approx 90% efficient

Test and reference points

GND Test Points, GND Test Points,
Top Side underside of board
Power Supply Constraints:
- If VDD_HV_A is driven from 3.3V, VDD_HV_FLA must also be supplied from 3.3V
- If VDD_HV_A is driven from 5V, the VDD_HV_FLA pin must be disconnected from 3.3V
- Don't attempt to over drive an analogue pad to 5V when the digital VDD_HV_x supply is set to 3.3V.
  This will trigger the ESD protection on that pad.
  For example if VDD_HV_A is set to 3.3V and the analogue supplies are set to 5V, you cannot drive 5V
  into a pad in the VDD_HV_A domain.

Default Configuration:
- All MCU supply voltages are set to 3.3V
  (ADC0, ADC1, VDD_HV_A, VDD_HV_B, VDD_HV_C, VBallast)
- VDD_HV_FLA = External 3.3V supplied (jumper fitted)

The analogue pins can only be driven to the same voltage as the VDD_HV_x domain they are situated in (i.e., max 3.3V) so makes sense for the analogue supply and reference to be 3.3V.

Notes on signal Grounds:
- The scheme shown has the analogue and digital grounds connected to the same plane.
- This results in better ADC performance than using an analogue ground plane with single entry point (or ferrite) to digital ground plane.
Calypso MCU Decoupling and bulk storage

Capacitor Types:
- 4700pF - Ceramic X7R, 50V 10% 0402 (Kemet C0402C104K0G4K4)
- 0.1uF - Ceramic X7R, 16V 10% 0402 (Kemet C0402C0100K0G100K1)
- 0.68uF - Ceramic X7R, 16V 10% 0805 (Murata GCM218R716M080K)
- 2.2uF - Ceramic X7R, 10V 10% 0603 Low ESR (Taiyo Yuden LMK107B7225T)
- 2.2uF - Ceramic X7R, 10V 10% 0603 Low ESR (Taiyo Yuden LMK107B7225A)

ADC
- ADC0_CAP
- ADC1_CAP
- ADC0REF_CAP

Flash
- HVFLA_CAP

Place small Caps as close as possible to MCU pins.

VDD_HVA
- C112 2.2uF
- C109 1.0uF
- C102 1.0uF
- C100 1.0uF

VDD_HVB
- C99 1.0uF

One 0.1uF cap per VDD_HV_x pin. Place as close as possible to pin.

VDD_LV
- C110 0.1uF
- C111 0.1uF
- C27 0.1uF
- C108 0.1uF
- C116 0.1uF
- C98 0.1uF
- C113 0.1uF

VDD_LV (1.25V) Decoupling. Place one of the 0.1uF caps close to each VDD_LV pin. Place the 0.68uF caps on each side of the package such that there is no cap on the side with the ballast transistor. (For regulator stability the total capacitance should be around 2.2uF).

Ballast Transistor
- B_CAP
- E_CAP
- C_CAP
- LVDEC_CAP

Place close to transistor.

LP Internal Reg Cap
- C119 4.7uF
- C122 2.2uF

Automotive Microcontroller Applications
East Kilbride, Scotland
NXP General Business Use
Reset and External Clock In

Reset is in the VDD_HVA domain.

Connect an external LVI to pad when supplying external 1.25V so that PORST is asserted until external 1.25V supply is at threshold and stable.

Tri-State Buffered RESET signal to reset the MCU.

Active reset drive (high / low) for any peripherals that need to be reset when MCU is in reset.

Note: The Reset pad on Calypso is in the VDD_HV_A domain which can be run from either 3.3V or 5V (selected by the VDD_HV_A and PER_HVA jumpers).

In to maintain brightness on the LED's irrespective of the voltage setting, the LED's are powered from constant 3.3V, grounded via the reset line.

Note: PORST needs to be pulled down to allow exit from STANDBY in some corner cases.
All CAN and LIN signals are in power domain VDD_HV_A. All interfaces will work at 3.3V or 5.0V (PER_HVA).
USB RS232 (serial) Interface

All Signals are in power domain
VDD_HV_A.
FTDI interface will work at 3.3V or 5.0V (PER_HVA)

FTDI USB <-> Serial Interface
- Self Powered mode. No power is taken from USB
- Device defaults to Dual serial (RS232) mode i.e. RS232 on both A and B
- Configurable I/O voltage on CHA / CHB via VDDIOA/B
USB (Type A Host and Type AB OTG)

USB Signals power domain

VDD_RVA The USB interface only supports 3.3V operation. All I/O signals must be 3.3V. If VDD RVA is set to 5V, USB MCU pads must be left as tri-state with no pullups.

5V0_SR 3V3_SR USB Signals

General Layout Note. Recommendation is to keep all tracks between MCU and USB PHI less than 3" See additional SMSC Layout guidelines PDF to the right.

USB Host, Type A
(Available on all packages)

USB Power Switch

Layout Note: Placement of termination resistor close to USB IC

(Layout Note: Route DP and DM with tracks as short as possible)
Ethernet (Configured for MII Mode)

All Ethernet Signals are in power domain VDD_RV_B

The Ethernet interface only supports 3.3V operation. All I/O signals must be 3.3V. If VDD_RVA is set to 5V, Ethernet MCU pads must be left as tri-state with no pullups.

3.3V operation. All I/O signals must be 3.3V. If VDD_RVA is set to 5V, Ethernet MCU pads must be left as tri-state with no pullups.

 Ethernet (Configured for MII Mode)

All Ethernet Signals are in power domain VDD_RV_B

The Ethernet interface only supports 3.3V operation. All I/O signals must be 3.3V. If VDD_RVA is set to 5V, Ethernet MCU pads must be left as tri-state with no pullups.
All Signals are in power domain VDD_HV_A.

FlexRAY interface will work at 3.3V or 5.0V (PER_HVA)

Note on VBAT:
- Operational range is 4.5V to 6.0V
- Undervoltage detection is max 4.1V

On EVB this is supplied from 5V, In theory this should be 60uS delay between applying U1 to VBAT. If necessary, 12V can be externally supplied by removing the resistor and connecting pad to 12V

Components spec'd for 12V operation

Bus voltage +/- 12V (VBAT = 12v)

Components spec'd for 12V operation

Bus voltage +/- 12V (VBAT = 12v)
User Peripherals (Led's, Switches and ADC Pot)

Switches are hard wired to 3.3V rather than 5V so it's not possible to drive 5V into a 3.3V pad (which would cause damage).

Similarly, the LED's are active low with 3.3v supply so can be safely coupled to pads on either 3.3V or 5V domains.

The ADC input is limited to 3.3V, again to prevent driving 5V into a 3.3V pad which would cause damage.

User LED's (Active Low)

PG[2..5] share eMIOS1 UC[11..14] with PMM

functionality

LED's are SMD (1206) Yellow

Note that LED2 and LED4 (PG3 and PG5) can be controlled in LPU RUN mode (and also have pad keepers in LPU_STANDBY)

User Peripherals (Led's, Switches and ADC Pot)
GPIO Pin Matrix

All pads are DNP (Do Not Populate) 0.1" pitch headers placed on a 0.1" grid

Layout Notes:
- Pads must be placed in a 5 (W) x 16(H) matrix pattern, 2.54 mm pitch
- one column for each port
- 16 tall (1 row for each port number from 0 to 15).
- GND pad at bottom of each column
- After production, pads should be through hole (not solder filled)
## 9. Revision History

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<tr>
<td>March 2016</td>
<td>Initial release</td>
</tr>
<tr>
<td>August 2016</td>
<td>Rev. 1: Updated Schematics and Board Pictures</td>
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