

HW Getting Started Guide

MPC8349EA MDS Processor Board

Nov 2006: Rev. A



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About This Document

This document shows how to connect the MPC8349EA MDS processor board and verify its basic operation, in a step by step format. Settings for switches and jumpers are shown, as well as instructions for connecting peripheral devices. In addition, instructions for connecting the MPC8349EA MDS processor board to an Integrated Development Environment (IDE), such as Freescale's *CodeWarrior®* are included, but instructions for working with the IDE are beyond the scope of this document. This version of the board has a faster DDR2 (400MHz), and a flash memory of 32MB.

Required Reading

It is assumed that the reader is familiar with the MPC8349EA chip, and the contents of the *MPC8349EA Reference Manual*.

Definitions, AcroRev. And Abbreviations

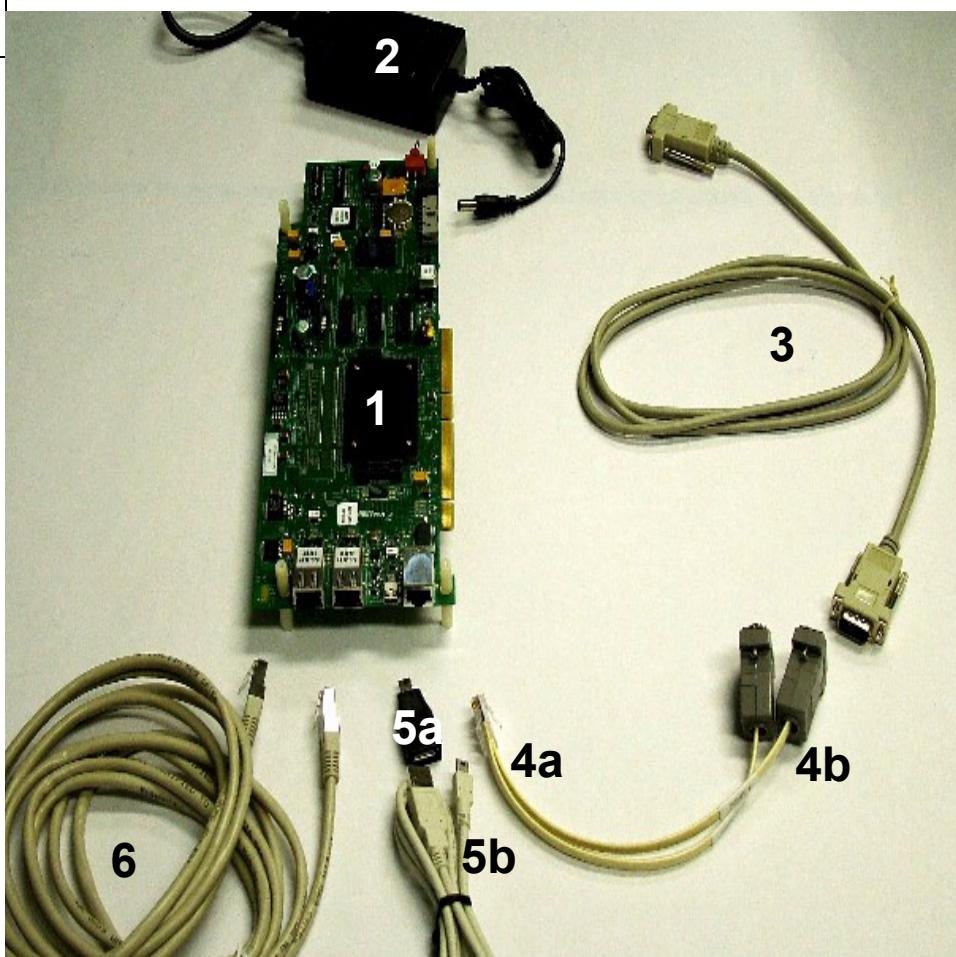
BCSR	board control and status register	LED	light emitting diode
BMS	boot memory space	PCI	peripheral component interconnect
CFG_RS	bit in RCW register	PCI_SYNC_OUT	chip pin
CLKDIV	clock division	PIB	platform I/O board
CLKIN	clock input	PLL	phase lock loop
COP	debug port in PowerPC	RCW	reset configuration words
DDR	double data rate DRAM	ROM	read-only memory
DIP	dual in-line package	SHMOO	sweep test (of frequency and core voltage)
I2C	Philips serial port	TLE	bit in RCW register
JTAG	IEEE standard 1149.1	TSEC	triple speed ethernet controller

MPC8349EA MDS Processor Board

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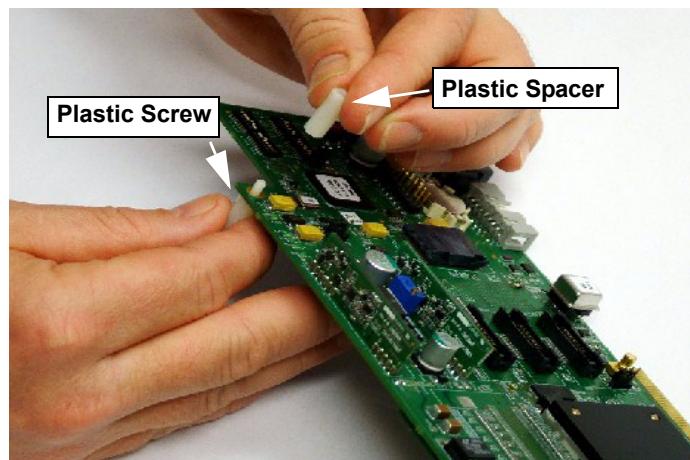
Step 1: Check HW kit contents

1. MPC8349EA MDS Processor Board
2. AC/DC 5V/5A universal power supply kit
3. RS232 standard serial cable with two 9-pin connectors-extends the Freescale adaptor cable
4. Freescale adaptor cable (joined) with one RJ45 and two RS232 connectors:
 - a) RJ45 10-pin plug
 - b) RS232 9-pin D-type connector
5. USB adaptor and connector:
 - a Mini USB adaptor: 5-pin (male) and 4-pin (female)
 - b USB cable with two connectors: standardA and miniB.
6. Ethernet cables (2) with RJ45-8 connectors
Not shown:
7. Four sets of plastic spacers (male/female)
8. One Allen wrench
9. CodeWarrior SW kit (includes JTAG connectivity unit)
10. MPC8349EA MDS Processor Board documentation



Step 2: Connect plastic spacers

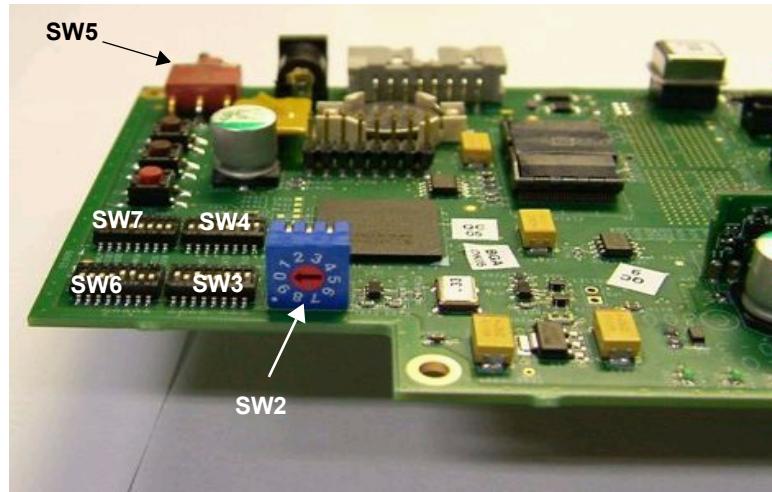
- Four sets of plastic spacers screw into holes located at (approximately) the four corners of the board. The spacers raise and stabilize the board.
1. From under the board, insert a spacer into one of the board's four spacer holes.
 2. Attach a female spacer onto the male spacer.
 3. Repeat for the three remaining pairs of spacers.



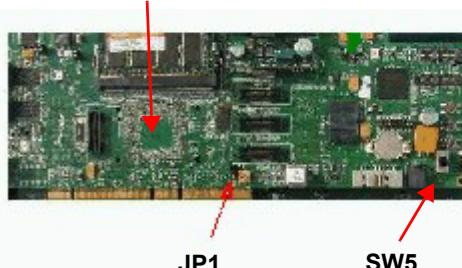
Step 3: Check Switches and Jumpers

The MPC8349EA MDS Processor Board has two rows of Dual-In-Line Package (DIP) switches. The default DIP-switch positions set-up the MPC8349EA MDS Processor Board clock mode as shown in the table below:

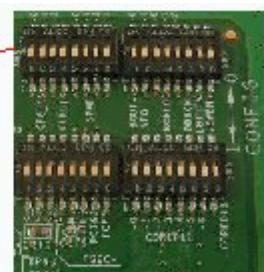
MPC8349EA MDS Processor Board Clock Mode	
e300 Core Frequency	533 MHz
CCB	266 MHz
DDR2 (can be changed to 400MHz)	266 MHz
Local Bus	133 MHz



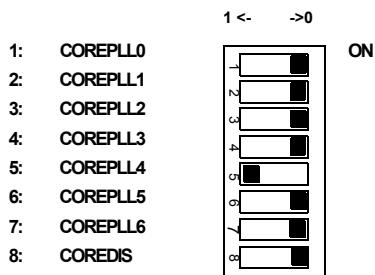
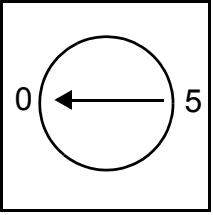
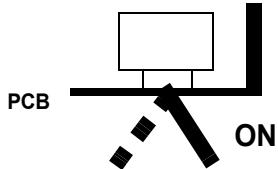
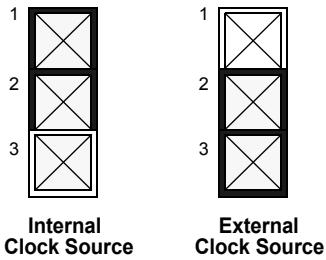
Socket for MPC8349EA



Switches SW3,4,6,7



Step 3.a: SW3 Configuration Set 1 <p>The "On" DIP Switch position corresponds to a signal value of "zero".</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr><td>1: CFG_RS0</td><td>1 <-> 0</td></tr> <tr><td>2: CFG_RS1</td><td>ON</td></tr> <tr><td>3: CFG_RS2</td><td>OFF</td></tr> <tr><td>4: CLKDIV</td><td>OFF</td></tr> <tr><td>5: SPMF0</td><td>OFF</td></tr> <tr><td>6: SPMF1</td><td>OFF</td></tr> <tr><td>7: SPMF2</td><td>OFF</td></tr> <tr><td>8: SPMF3</td><td>OFF</td></tr> </table>	1: CFG_RS0	1 <-> 0	2: CFG_RS1	ON	3: CFG_RS2	OFF	4: CLKDIV	OFF	5: SPMF0	OFF	6: SPMF1	OFF	7: SPMF2	OFF	8: SPMF3	OFF	SW3.1-SW3.3 CFG_RS sets the Reset Configuration Words Source ON: value of zero factory setting: '000' when RCW is fetched from the local bus DIP-switch SW9/3 FCFG: chooses between BCSR or Flash RCW source SW3.4 CLKDIV selects the relationship between CLKIN and PCI_SYNC_OUT if the MPC8349 is configured as a PCI Agent (factory setting) then CLK_DIV is low SW3.5-SW3.8 SPMF selects System PLL Multiplication Factor factory setting: '0100' clock ratio: csb_clk/CLKIN = 4 (csb_clk = 266MHz) or csb_clk/PCI_CLK = 4 Factory default setting: 00000101
1: CFG_RS0	1 <-> 0																
2: CFG_RS1	ON																
3: CFG_RS2	OFF																
4: CLKDIV	OFF																
5: SPMF0	OFF																
6: SPMF1	OFF																
7: SPMF2	OFF																
8: SPMF3	OFF																
Step 3.b: SW4 Configuration Set 2 <table border="1" style="margin-left: auto; margin-right: auto;"> <tr><td>1: TSEC1-0</td><td>1 <-> 0</td></tr> <tr><td>2: TSEC1-1</td><td>ON</td></tr> <tr><td>3: TSEC2-0</td><td>OFF</td></tr> <tr><td>4: TSEC2-1</td><td>OFF</td></tr> <tr><td>5: BMS</td><td>OFF</td></tr> <tr><td>6: TLE</td><td>OFF</td></tr> <tr><td>7: PCI64</td><td>OFF</td></tr> <tr><td>8: FCFG</td><td>OFF</td></tr> </table>	1: TSEC1-0	1 <-> 0	2: TSEC1-1	ON	3: TSEC2-0	OFF	4: TSEC2-1	OFF	5: BMS	OFF	6: TLE	OFF	7: PCI64	OFF	8: FCFG	OFF	SW4.1-SW4.2: TSEC1/TSEC2 Selects the protocol used by the two-port TSEC controller factory setting: enters GMII mode when TSEC1 and TSEC2 initiate similar 2'b10 SW4.5: BMS: Selects boot memory space factory setting is '1' when boot memory resides in upper eight Mbytes at 0xFF80_0000 to 0xFFFF_FFFF SW4.6 TLE: Selects endian mode factory setting: '0'; big endian mode SW4.7: PCI64: Selects PCI width factory setting: '0'; 32-bit width SW4.8: FCFG: Sets RCW source on local bus '0': BCSR source; setting uses values from SW3 and SW6. '1': Flash source - setting is burned in flash memory Factory setting: '0' Factory default setting: 10101000
1: TSEC1-0	1 <-> 0																
2: TSEC1-1	ON																
3: TSEC2-0	OFF																
4: TSEC2-1	OFF																
5: BMS	OFF																
6: TLE	OFF																
7: PCI64	OFF																
8: FCFG	OFF																
Step 3.c: SW6 Configuration Set 3 <table border="1" style="margin-left: auto; margin-right: auto;"> <tr><td>1: BOOTSEQ0</td><td>1 <-> 0</td></tr> <tr><td>2: BOOTSEQ1</td><td>ON</td></tr> <tr><td>3: ROMLOC0</td><td>OFF</td></tr> <tr><td>4: ROMLOC1</td><td>OFF</td></tr> <tr><td>5: ROMLOC2</td><td>OFF</td></tr> <tr><td>6: DDRCM</td><td>OFF</td></tr> <tr><td>7: LBIUCM</td><td>OFF</td></tr> <tr><td>8: SWEN</td><td>OFF</td></tr> </table>	1: BOOTSEQ0	1 <-> 0	2: BOOTSEQ1	ON	3: ROMLOC0	OFF	4: ROMLOC1	OFF	5: ROMLOC2	OFF	6: DDRCM	OFF	7: LBIUCM	OFF	8: SWEN	OFF	SW6.1-SW6.2: Boot sequencer configuration Boot sequencer loads configuration data from the serial ROM. Factory setting: '00'; disables access to I2C ROM. SW6.3-SW6.5: Boot ROM location Factory setting: '110'; provides flash boot on local bus SW6.6 DDR: Clock mode Factory setting: '0'; operates with DDR clock (identical to csb_clk) SW6.7: Local bus clock mode Factory setting: '1'; operates with local bus clock - half of csb_clk SW6.8: Software watchdog Factory setting: '0'; with software watchdog disabled Factory default setting: 00110010
1: BOOTSEQ0	1 <-> 0																
2: BOOTSEQ1	ON																
3: ROMLOC0	OFF																
4: ROMLOC1	OFF																
5: ROMLOC2	OFF																
6: DDRCM	OFF																
7: LBIUCM	OFF																
8: SWEN	OFF																

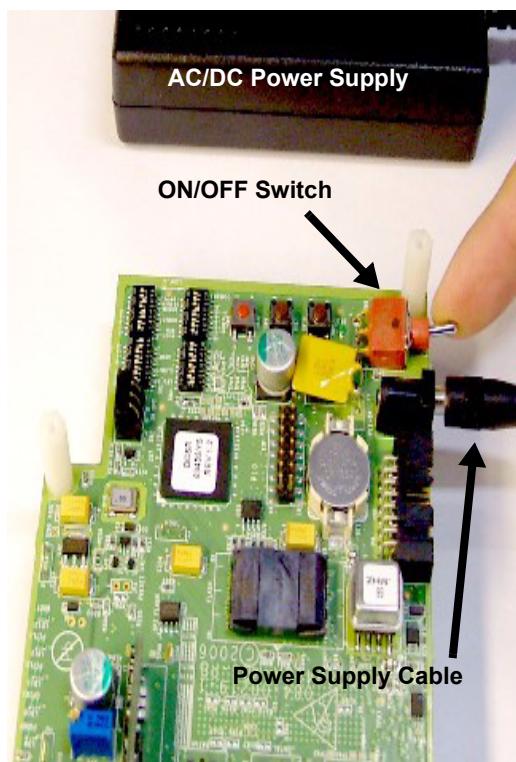
Step 3.d: SW7 Configuration Set 4  <p>1: COREPLL0 2: COREPLL1 3: COREPLL2 4: COREPLL3 5: COREPLL4 6: COREPLL5 7: COREPLL6 8: COREDIS</p>	SW7.1-SW7.7: Core PLL setting Sets the ratio between the e300 core clock and the internal csb_clk Factory setting: '000010000' for core_clk = 533MHz Recommended secondary setting: '00000110' for core_clk = 500MHz SW7.8: Core disable Factory setting: '0'; core enabled for boot operation Factory default setting: 00001000
Step 3.e: SW2 Software Option 	SW2: Software option Software BCS rotary-switch SW2 positions (0-7) enable program flow change Switch status can be seen in BCSR10[2-4] Factory setting: '0'
Step 3.f: SW5 Power Switch 	SW5: power switch ON: power from an external 5V power supply via the P10 power jack combined mode: powered from +5V on PIB power supply through riser connectors (regardless of SW5 position) board plugged as a PCI add-in card: PC internal power supply will provide 5V via PCI edge connector (regardless of SW5 position)
Step 3.g: JP1: Internal/External Clock  <p>Internal Clock Source External Clock Source</p>	JP1 Selects the source for the CLOCKIN signal <ul style="list-style-type: none"> If a jumper is located between JP1 pins 1-2 (factory setting), the processor is clocked from the on-board clock oscillator (U21 socket) If a jumper is located between JP1 pins 2-3, the processor is clocked from an external source (via P5) The SHMOO mode clock source is I2C; manually programmed clock synthesizer residing on PIB

Step 4: Assemble and connect the power supply kit.

Note:
Move power switch to OFF.

Assemble the AC/DC power supply kit:

- power cable with country-specific wall outlet plug
 - power supply unit and cable with jack (for board connection)
1. Connect the AC/DC power supply cable with jack to the board.
 2. Plug the power cable into the wall outlet.



Step 5: Perform initial board power up.

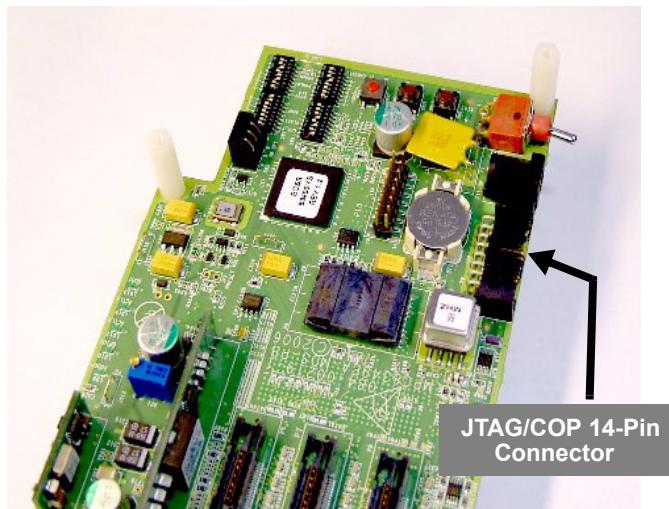
Note:
To prevent damage to the JTAG connectivity unit connect the unit only after initial board reset.

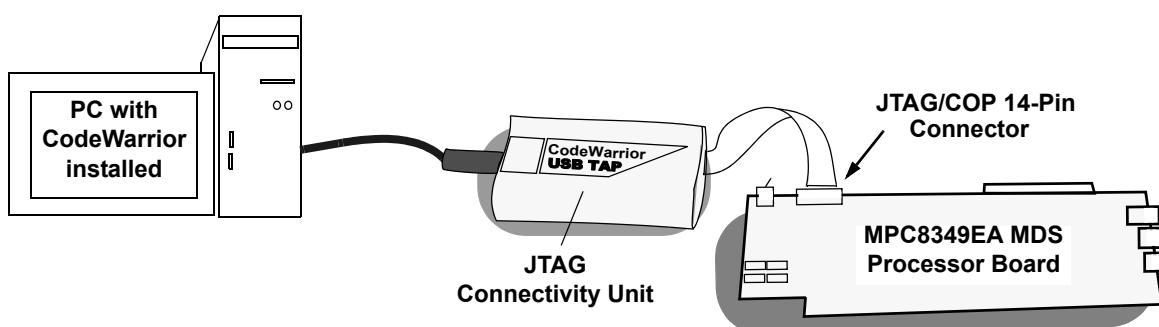
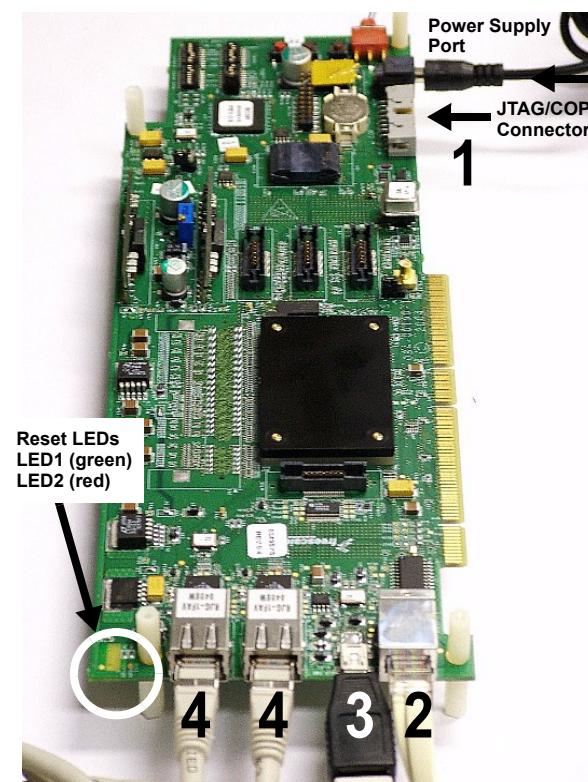
1. Move the power switch to ON. LED1 briefly displays green light.
2. Check for completion of the reset sequence-indicated by a single flash of LED1 (green) and LED2 (red). The location of LED1 and LED2 is marked in the figure of Step 7 on page 7.
3. Shut off the power-move the power switch to OFF.

Step 6: Connect the JTAG connectivity unit to the board.

The JTAG connectivity unit enables CodeWarrior SW work with the board.

1. Connect the JTAG connectivity unit to the JTAG/COP 14-pin connector.
2. Move the power switch to ON.
3. Check for completion of the reset sequence (see Step 5 on page 6).
4. Continue as per the instructions in the Kit Configuration Guide.



	
<p>Step 7: Attach remaining cables to the board according to your development needs.</p> <p>Connect the remaining cables to the board as per user development needs and planned board use:</p> <ol style="list-style-type: none"> 1. JTAG/COP connector for JTAG connectivity unit-included in the CodeWarrior SW kit 2. Serial port for the joined Freescale adaptor cable with one RJ45 and two RS232 connectors: <ul style="list-style-type: none"> a RJ45 10-pin plug-plugs into the serial port b RS232 9-pin D-type connector 3. USB port for USB adaptor and connector: <ul style="list-style-type: none"> a mini USB adaptor: 5-pin (male) and 4-pin (female) b USB cable with two connectors: standardA and miniB. 4. Ethernet ports for the two Ethernet cables with RJ45-8 pin connectors. 	

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