6/97

MPC850FADS Daughter Board Design Specification—Rev 0

PRELIMINARY

MOTOROLA

1 - General Information

1•1 Introduction

This document is the operation guide for the MPC8XXFADS Daughter Board for the MPC850—namely, the MPC850FADSDB.

The daughter board holds the evaluated MPC850 along with some necessary logic, which is required to be in the nearest vicinity of the MPC850 as well as peripherals, that are dedicated to the MPC850 and are not required for any other member of the MPC8XX family.

The daughter board has 2 sets of matching connectors - on the print[A] side and on the component[B] side. Those on the print side, connect to a matching set found on the MPC8XXFADS while those on the component side, are to serve hardware expansion via a dedicated adaptor.

In addition, a set of logic analyzer connector is featured matching the new high density HP16500 logic analyzer adaptors, this to provide fast connection to logic analyzer while saving on board's space and reducing EMI.

1•2 List of Abbreviations

- FADS[C] - the MPC8XXFADS, to which this board connects.
- UPM - User Programmable Machine
- GPCM - General Purpose Chip-select Machine
- GPL - General Purpose Line (associated with the UPM)
- I/R - Infra-Red
- MPCADS - the MPC850FADSDB, the subject of this document.
- BSCR - Board Control & Status Register.
- ZIF - Zero Input Force
- BGA - Ball Grid Array
- DB - The MPC850-FADSDB, the subject of this document.
- Spec - engineering Specification Document.

1•3 Related Documentation

- MPC850 Engineering Specification.
- ADI Board Specification.
- MPC8XXFADS Engineering Specification
- PHILIPS's PDIUSBP11 Data Sheet. May be obtained from http://www.semiconductors.philips.com/acrobat/4417.pdf

1•4 SPECIFICATIONS

The MPC832FADSDB specifications are given in TABLE 1-1.

TABLE 1-1. MPC850FADSDB Specifications

CHARACTERISTICS	*SPECIFICATIONS*
Microprocessor	MPC850 @ 50 MHz

A. Board's bottom.
B. Board's top.
C. Not to be mistaken for the M683XX Family Ads

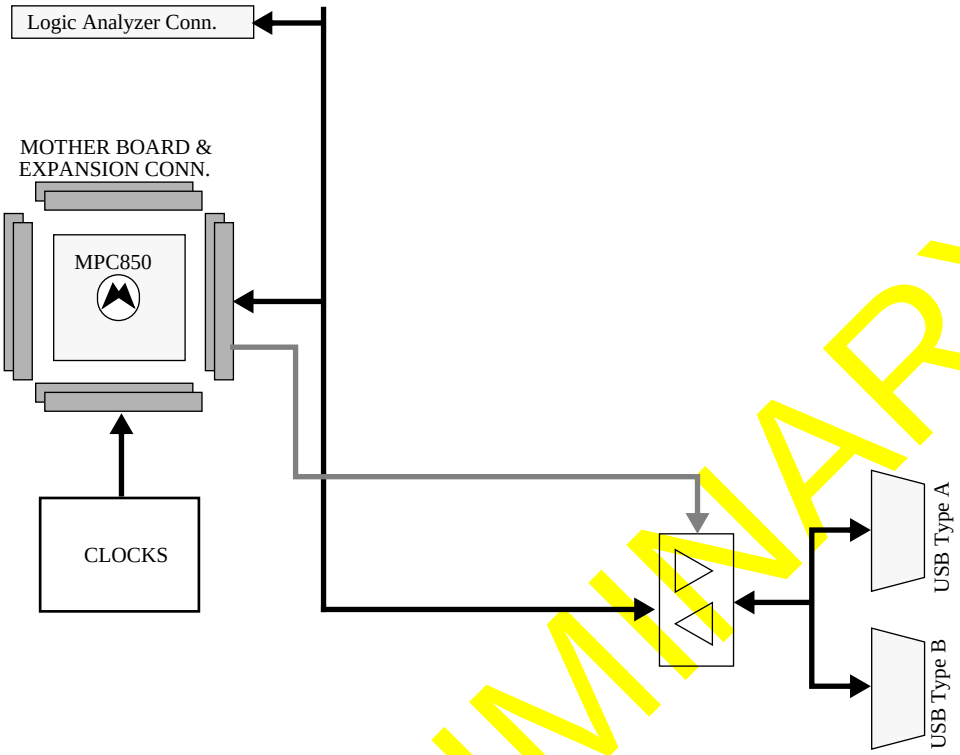
TABLE 1-1. MPC850FADSDB Specifications

CHARACTERISTICS	*SPECIFICATIONS*
Addressing Total address range:	 4 GBytes Internal 64 MByte External
Operating temperature	0°C - 30°C
Storage temperature	-25°C to 85°C
Relative humidity	5% to 90% (non-condensing)
Dimensions: Length Width Thickness	 5.87 " (149 mm) 4.37 " (111 mm) 0.063 " (1.6 mm)

1•5 MPC850-FADSDB Features

- ❑ MPC850 running upto 50 MHz
- ❑ USB Port with shutdown option - BCSR controlled. Support for both type A and Type B USB connectors.
- ❑ USB Port Speed control, BCSR driven.
- ❑ 5V supply for USB port, BCSR controlled.
- ❑ Selectable KAPWR source: 3.3V or externally supplied
- ❑ Selectable VDDL source: 3.3V or 2V
- ❑ Selectable clock source: 32768Hz crystal resonator or 4MHz Clock generator.
- ❑ On-Board Expansion connectors, including all MPC pins and MPC8XXFADS control / status signals.
- ❑ On-Board High Density Logic Analyzer connectors, supporting fast connection to HP 16500 logic analyzer.
- ❑ MPC860 Modem Tool Support.

FIGURE 1-1 MPC850-FADSDB Block Diagram



1•6 Changes From Previous Revision (Draft 0.1)

1) Changed SCC2 port to MPC8XXFADS connection scheme. See 4•5 "Communication Ports" on page 31.
2) Added USB Power control (BCSR controlled) with Power On indication led.
3) Added 3.3V pull-up resistors over USB's D+ and D- lines. Connection scheme of these resistors depends on USB port's speed. See 4•5•1 "USB Port" on page 32.
4) Added support for MPC860 Modem Tool. See 4•8•1 "MPC860 Modem Tool Support" on page 33.
5) The selection of Power-On reset source is moved on-board from the MPC8XXFADS.
6) Part #s are provided for all connectors.

2 - Hardware Preparation and Installation

2•1 INTRODUCTION

This chapter provides unpacking instructions, hardware preparation, and installation instructions for the MPC850FADSDB.

2•2 UNPACKING INSTRUCTIONS

NOTE

If the shipping carton is damaged upon receipt, request carrier's agent to be present during unpacking and inspection of equipment.

Unpack equipment from shipping carton. Refer to packing list and verify that all items are present. Save packing material for storing and reshipping of equipment.

CAUTION

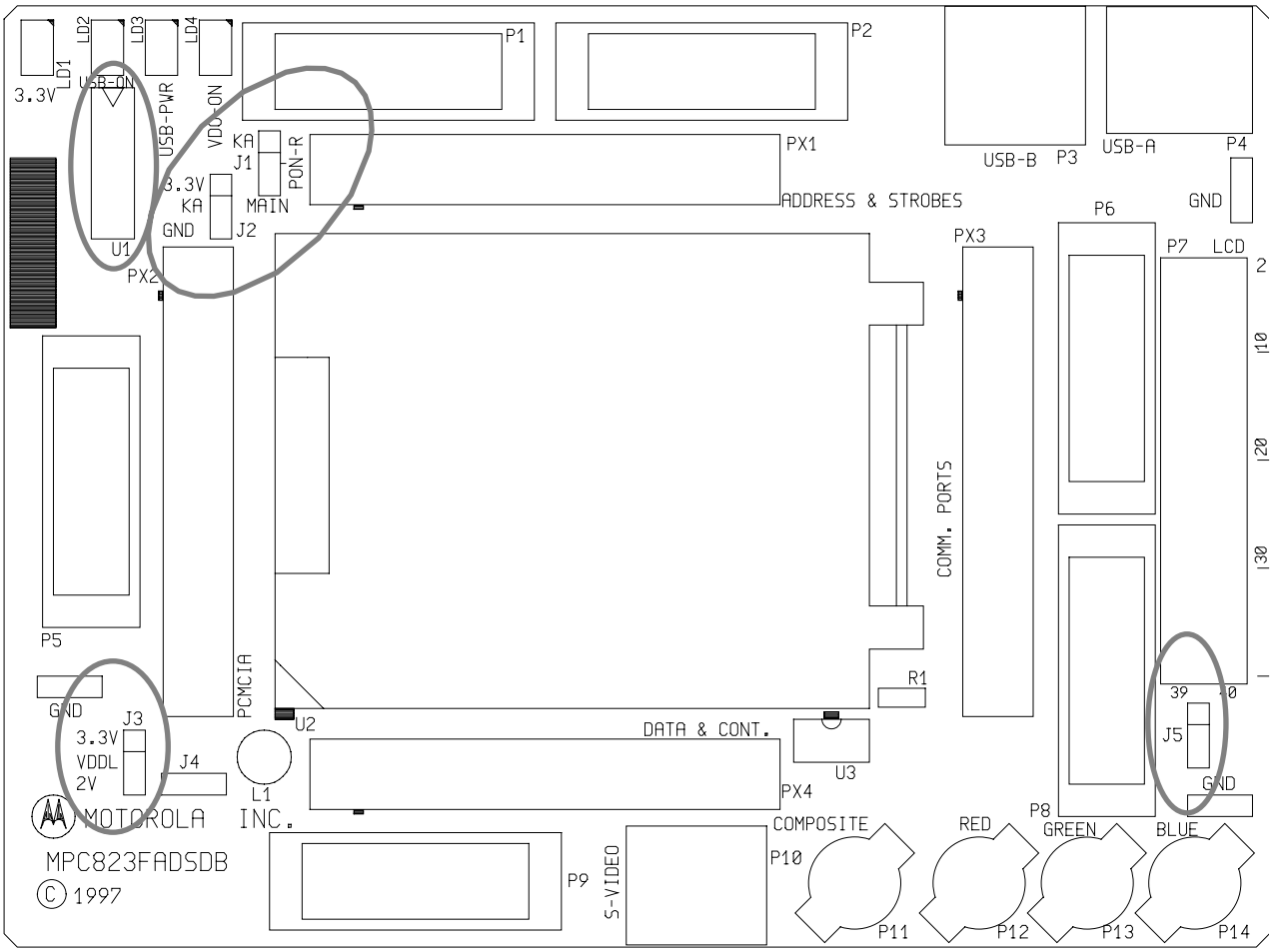
AVOID TOUCHING AREAS OF INTEGRATED CIRCUITRY; STATIC DISCHARGE CAN DAMAGE CIRCUITS.

2•3 HARDWARE PREPARATION

To select the desired configuration and ensure proper operation of the MPC850FADSDB board, changes of the jumpers settings may be required before installation. The location of the switches, LEDs, and connectors is illustrated in FIGURE 2-1 "MPC850FADSDB Top Side Part Location diagram" on page 5. The board has been factory tested and is shipped with Dip-Switch settings as described in the following paragraphs. Parameters can be changed for the following conditions:

- Power-On Reset Source.
- MPC Keep Alive Power Source
- MPC Internal Logic Supply Source

FIGURE 2-1 MPC850FADSDB Top Side Part Location diagram

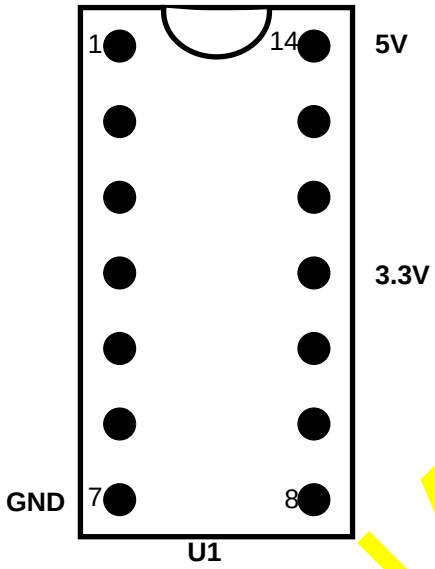


2•3•1 Clock Generator Replacement - U1

When replacing U1 with another clock generator it should be noticed that there are 2 supply level available at U1:

1) 5V supply at pin 14.
2) 3.3V supply available at pin 11.

FIGURE 2-2 U1 Power Sources



From looking at FIGURE 2-2 "U1 Power Sources" above, we see that 5V oscillator may be used with 14 pins only form-factor while 3.3V oscillators may be used with 8 pins only form-factor.

WARNING

IF A 14 Pin Form-Factor, 3.3V Clock Generator is inserted to U17, PERMANENT DAMAGE Might Be Inflicted To The Device.

WARNING

Since the MPC clock input is NOT 5V FRIENDLY, any clock generator inserted to U17, MUST BE 3.3V compatible. If a 5V output clock generator is inserted to U17, PERMANENT DAMAGE might be inflicted to the MPC.

2•3•2 Power-On Reset Source Selection

As there are differences between MPC revisions regarding the functionality of the Power-On Reset logic, it is therefore necessary to select different sources for Power-ON reset generation.

J1 on the ADS is used to select Power-On Reset source: when a jumper is placed between positions 1 - 2 of J1, Power-On reset to the MPC is generated by the Keep-Alive power rail. I.e., When KAPWR goes below 2.005V - Power-On reset is generated. When a jumper is place between position 2 - 3 of J1, Power-On reset to the MPC is generated from the MAIN 3.3V power rail. I.e, when the MAIN 3.3V power rail goes below 2.805V Power-On reset is generated.

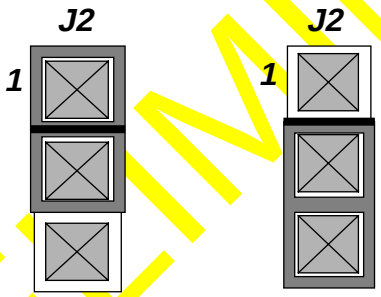
FIGURE 2-3 Power-On Reset Source Selection

KA Power Rail MAIN Power Rail

2•3•3 VDDL Source Selection

J2 serves as a selector for VDDL - MPC internal logic supply. When a jumper is placed between positions 1 - 2 of J2, VDDL is supplied with 3.3V. When a jumper is placed between positions 2 - 3 of J2, VDDL is supplied by 2V power source. The jumper on J2 is factory set between positions 1 - 2 to supply 3.3 to VDDL.

FIGURE 2-4 VDDL Source Selection



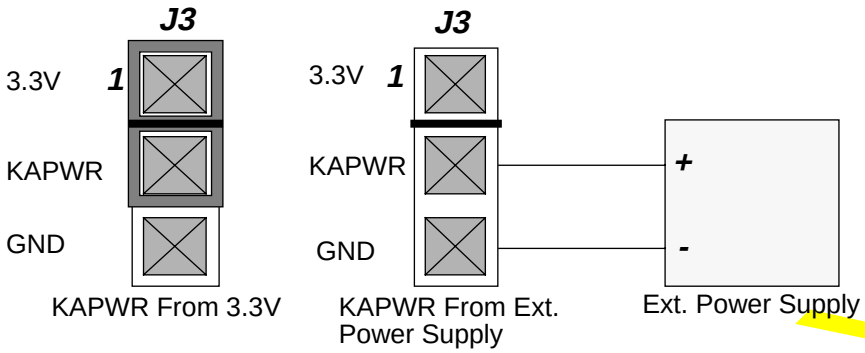
VDDL - 3.3V VDDL - 2V

2•3•4 Keep Alive Power Source Selection

J3 selects the Keep Alive power source of the MPC. When a jumper is placed between positions 1 - 2 of J3, the Keep Alive power is fed from the main 3.3V bus. When an external power source[A] is to be connected to the Keep Alive power rail, it should be connected between positions 2 (the positive pole) and position 3 (GND) of J3.

A. E.g., a battery.

FIGURE 2-5 Keep Alive Power Source Selection



2•4 INSTALLATION INSTRUCTIONS

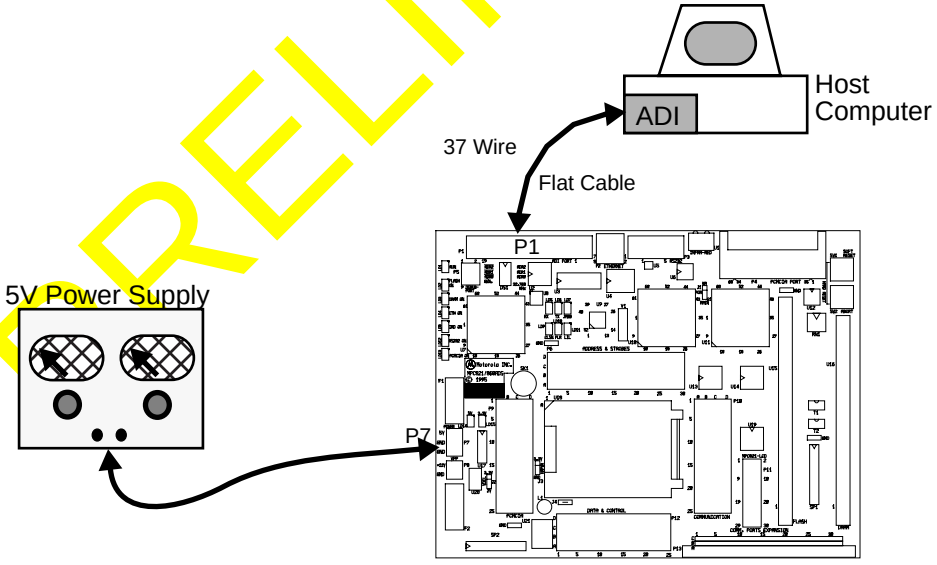
When the MPC850FADSDB has been configured as desired by the user, it can be installed according to the required working environment as follows:

- Host Controlled Operation
- Debug Port Controller for Target System
- Stand-Alone

2•4•1 Host Controlled Operation

In this configuration the MPC850FADSDB is controlled by a host computer via the ADI through the debug port. This configuration allows for extensive debugging using on-host debugger.

FIGURE 2-6 Host Controlled Operation Scheme



2•4•2 Debug Port Controller For Target System

This configuration resembles the previous, but here the local MPC is removed from its socket while the ADS is connected via a 10 lead Flat-Cable between P5 and a matching connector on a target system.

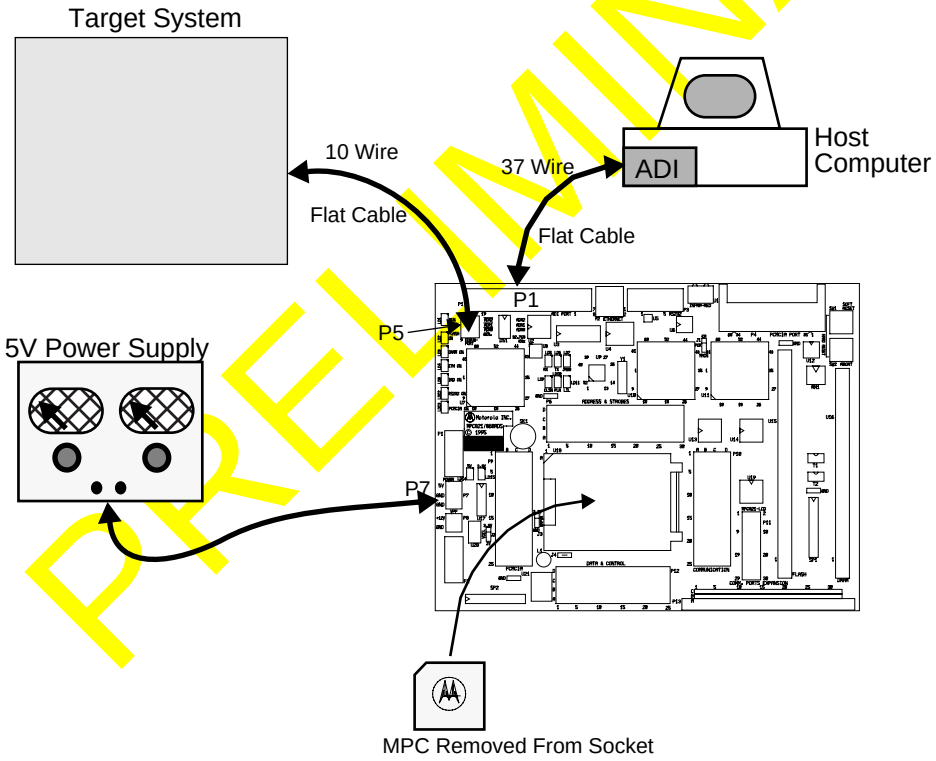
WARNING

When connecting the ADS to a target system via P5 and a 10 lead flat-cable, the MPC MUST be REMOVED from its SOCKET (U18). Otherwise, PERMANENT DAMAGE might be inflicted to either the Local MPC or to the Target MPC.

With this mode of operation, all on-board modules are disabled and can not be accessed in anyway, except for the debug port controller. Also, all indications except for 5V power, 3.3V power and RUN are darkened.

All debugger commands and debugging features are available in this mode, including s/w download, breakpoints, etc‘... The target system may be reset or interrupted by the debug port or reset by the ADS’s RESET switches. It is the responsibility of the target system designer, to provide Power-On-Reset and HARD-Reset configurations, while SOFT-Reset configuration is provided by the debug-port controller. See also 4•15•1 "MPC821/860ADS As Debug Port Controller For Target System" on page 57.

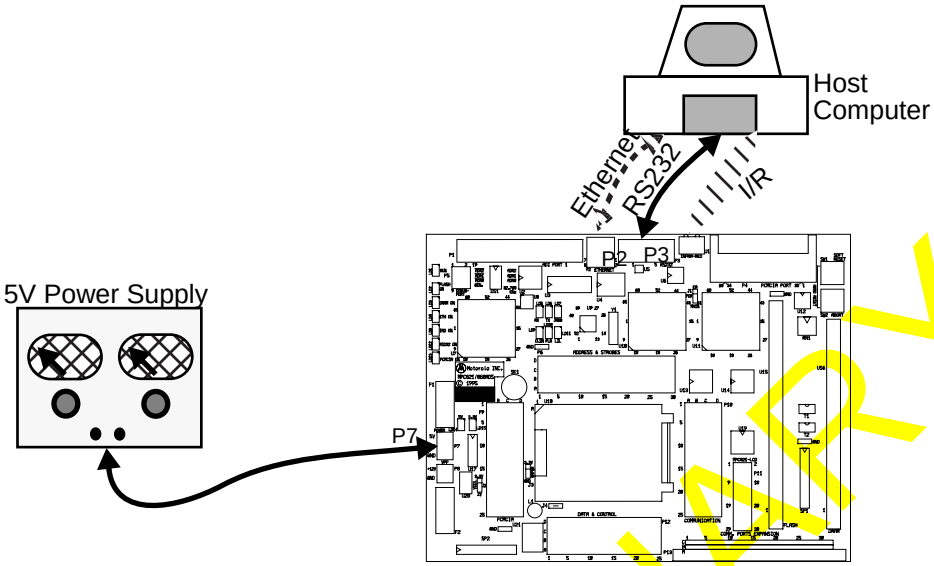
FIGURE 2-7 Debug Port Controller For Target System Operation Scheme



2•4•3 Stand Alone Operation

In this mode, the board is not controlled by the host via the ADI/Debug port. It may connect to host via one of its other ports, e.g., RS232 port, I/R port, Ethernet port, etc‘. Operating in this mode requires an application program to be programmed into the board‘s Flash memory (while with the host controlled operation, no memory is required at all).

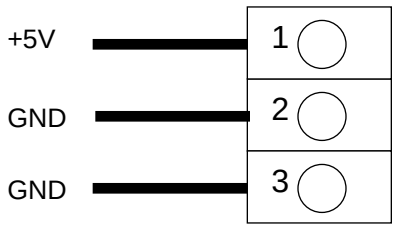
FIGURE 2-8 Stand Alone Configuration



2•4•4 +5V Power Supply Connection

The MPC850FADSDB requires +5 Vdc @ 5 A max, power supply for operation. Connect the +5V power supply to connector P7 as shown below:

FIGURE 2-9 P7: +5V Power Connector



P7 is a 3 terminal block power connector with power plug. The plug is designed to accept 14 to 22 AWG wires. It is recommended to use 14 to 18 AWG wires. To provide solid ground, two Gnd terminals are supplied. It is recommended to connect both Gnd wires to the common of the power supply, while VCC is connected with a single wire.

NOTE

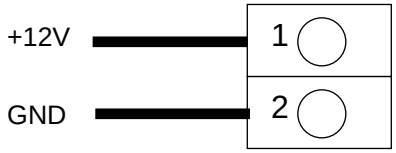
Since hardware applications may be connected to the MPC850FADSDB using the expansion connectors P6, P9, P10, P12 or P13, the additional power consumption should be taken into consideration when a power supply is connected to the MPC850FADSDB.

2•4•5 P8: +12V Power Supply Connection

The MPC850FADSDB requires +12 Vdc @ 1 A max, power supply for the PCMCIA channel Flash programming capability. The MPC850FADSDB can work properly without the +12V power supply, if there is no need to program a 12V programmable PCMCIA flash card.

Connect the +12V power supply to connector P6 as shown below:

FIGURE 2-10 P8: +12V Power Connector



P8 is a 2 terminal block power connector with power plug. The plug is designed to accept 14 to 22 AWG wires. It is recommended to use 14 to 18 AWG wires.

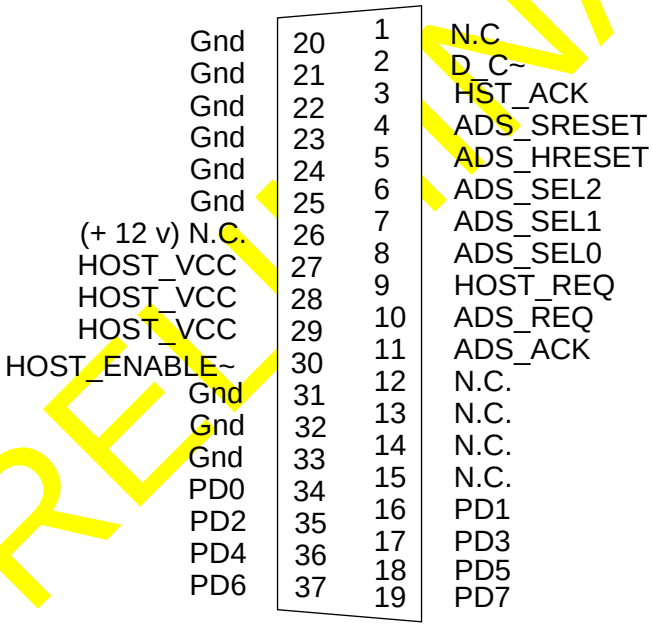
2•4•6 ADI Installation

For ADI installation on various host computers, refer to APPENDIX C - "ADI Installation" on page 182.

2•4•7 Host computer to MPC850FADSDB Connection

The MPC850FADSDB ADI interface connector, P1, is a 37 pin, male, D type connector. The connection between the MPC850FADSDB and the host computer is by a 37 line flat cable, supplied with the ADI board. FIGURE 2-11 below shows the pin configuration of the connector.

FIGURE 2-11 P1 - ADI Port Connector



NOTE: Pin 26 on the ADI is connected to +12 v power supply, but it is not used in the MPC850FADSDB.

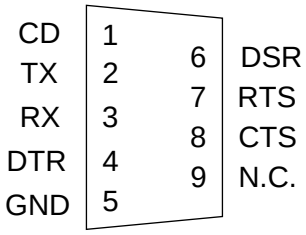
2•4•8 Terminal to MPC850FADSDB RS-232 Connection

A serial (RS232) terminal or any other RS232 equipment, may be connected to the RS-232 connector P3. The RS-232 connector is a 9 pin, female, D-type connector as shown in FIGURE 2-12.

The connector is arranged in a manner that allows for 1:1 connection with the serial port of an IBM-AT[A] or compatibles, i.e. via a flat cable.

A. IBM-AT is a trademark of International Business Machines Inc.

FIGURE 2-12 P3 - RS-232 Serial Port Connector



NOTE: The RTS line (pin 7) is not connected on the MPC850FADSDB.

2•4•9 Memory Installation

The MPC850FADSDB is supplied with two types of memory SIMM:

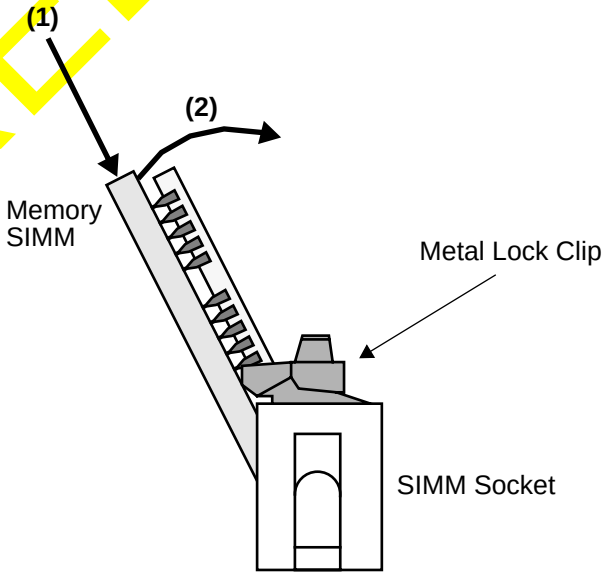
- EDO DRAM SIMM
- Flash Memory SIMM.

To avoid shipment damage, these memories are packed aside rather than being installed in their sockets. Therefore, they should be installed on site. To install a memory SIMM, it should be taken out of its package, put diagonally in its socket (no error can be made here, since the Flash socket has 80 contacts, while the DRAM socket has 72) and then twisted to a vertical position until the metal lock clips are locked. See FIGURE 2-13 "Memory SIMM Installation" below.

CAUTION

The memory SIMMs have alignment nibble near their # 1 pin. It is important to align the memory correctly before it is twisted, otherwise damage might be inflicted to both the memory SIMM and its socket.

FIGURE 2-13 Memory SIMM Installation



3 - OPERATING INSTRUCTIONS

3•1 INTRODUCTION

This chapter provides necessary information to use the MPC850FADSDB in host-controlled and stand-alone configurations. This includes controls and indicators, memory map details, and software initialization of the board.

3•2 CONTROLS AND INDICATORS

The MPC850FADSDB has the following switches and indicators.

3•2•1 SOFT RESET Switch SW1

The SOFT RESET switch SW1 performs Soft reset to the MPC internal modules, maintaining MPC's configuration (clocks & chip-selects) and dram contents. The switch signal is debounced, and it is not possible to disable it by software. At the end of the Soft Reset Sequence, the Soft Reset Configuration is sampled and becomes valid.

3•2•2 ABORT Switch SW2

The ABORT switch is normally used to abort program execution, this by issuing a level 0 interrupt to the MPC. If the ADS is in stand alone mode[A], it is the responsibility of the user to provide means of handling the interrupt, since there is no resident debugger with the MPC850FADSDB. The ABORT switch signal is debounced, and can not be disabled by software.

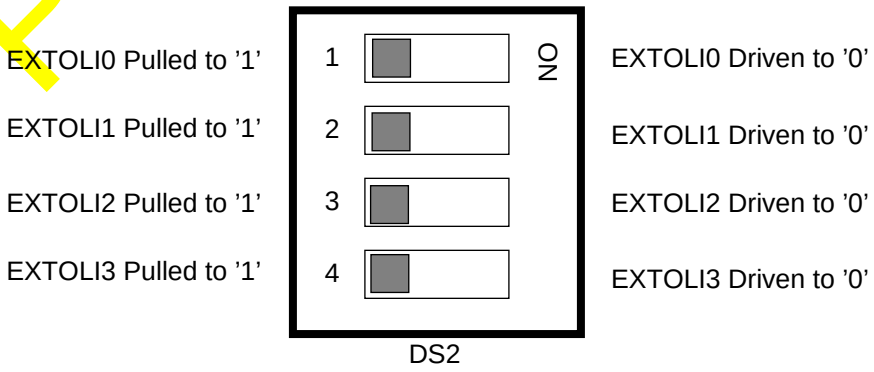
3•2•3 HARD RESET - Switches SW1 & SW2

When BOTH switches - SW1 and SW2 are depressed simultaneously, HARD reset is generated to the MPC. When the MPC is HARD reset, all its configuration is lost, including data stored in the DRAM and the MPC has to be re-initialized. At the end of the Hard Reset sequence, the Hard Reset Configuration stored in BCSR0 becomes valid.

3•2•4 DS2 - Software Options Switch

DS2 is a 4-switches Dip-Switch, mounted over SP2. This switch is connected over EXTOLI(0:3) lines, and since EXTOLI(0:3) lines are available at BCSR, S/W options may be manually selected, according to DS2 state.

FIGURE 3-1 DS2 - Description



A. I.e., detached from a debug station.

3•2•5 J4 Power Bridge

J4 is a soldered jumper, which is in series with the 3.3V power bus. This jumper may be removed[A] if current measurements on the 3.3V bus are to be held.

Warning

There are also GND bridges on board, which physically resemble J4. Do not mistake J4 to be a GND jumper, otherwise, permanent damage might be inflicted to the MPC850FADSDB.

3•2•6 GND Bridges

There are 4 GND bridges on the MPC850FADSDB. They are meant to assist general measurements and logic-analyzer connection.

Warning

When connecting to a GND bridge, use only INSULATED GND clips. Failure in doing so, might result in permanent damage to the MPC850FADSDB.

3•2•7 RUN Indicator - LD1

When the green RUN led - LD1 is lit, it indicates that the MPC is not in debug mode, i.e., VFLS0 & VFLS1 == 0. It is important to remember, that if the VFLS(0:1) pins are programmed for alternative use rather than function as VFLS lines, this indication is meaningless.

3•2•8 FLASH ON - LD2

When the yellow FLASH ON led is lit, it indicates that the FLASH module is enabled in the BCSR1 register. I.e., any access done to the CS0~ address space will hit the flash memory. When it is dark, the flash is disabled and CS0~ may be used off-board via the expansion connectors.

3•2•9 DRAM ON - LD3

When the yellow DRAM ON led is lit, it indicates the DRAM is enabled in BCSR1. Therefore, any access made to CS1~ (or CS2~) will hit on the DRAM. When it is dark, it indicates that either the DRAM is disabled in BCSR1, enabling the use of CS1~ and CS2~ off-board via the expansion connectors.

3•2•10 ETH ON - LD4

When the yellow ETH ON led is lit, it indicates that the ethernet port transceiver - the MC68160 EEST, connected to SCC1 is active. When it is dark, it indicates that the EEST is in power down mode, enabling the use of SCC1 pins off-board via the expansion connectors.

3•2•11 Ethernet RX Indicator - LD5

The green Ethernet Receive LED indicator blinks whenever the EEST is receiving data from one of the Ethernet port.

3•2•12 Ethernet TX Indicator - LD6

The green Ethernet Receive LED indicator blinks whenever the EEST is transmitting data via the Ethernet port.

3•2•13 Ethernet JABB Indicator - LD7

The red Ethernet TP Jabber LED indicator - JABB, lights whenever a jabber condition is detected on the TP ethernet port.

3•2•14 IRD ON - LD8

A. By a skilled technician only.

When the yellow IRD ON led is lit, it indicates that the Infra-Red transceiver - the TFDS3000, connected to SCC2, is active and enables communication via that medium. When it is dark, the I/R transceiver is in shutdown mode, enabling the use of SCC2 pins off-board via the expansion connectors.

3•2•15 Ethernet CLSN Indicator LD9

The red Ethernet Collision LED indicator CLSN, blinks whenever a collision condition is detected on the ethernet port, i.e., simultaneous receive and transmit.

3•2•16 Ethernet PLR Indicator - LD10

The red Ethernet TP Polarity LED indicator - PLR, lights whenever the wires connected to the receiver input of the ethernet port are reversed. The LED is lit by the EEST, and remains on while the EEST has automatically corrected for the reversed wires.

3•2•17 Ethernet LIL Indicator - LD11

The yellow Ethernet Twisted Pair Link Integrity LED indicator - LIL, lights to indicate good link integrity on the TP port. The LED is off when the link integrity fails.

3•2•18 RS232 Port 1 ON - LD12

When the yellow RS232 ON led is lit, it designates that the RS232 transceiver connected to SMC1, is active and communication via that medium (through PA3) is allowed. When dark, it designates that the transceiver is in shutdown mode, so SMC1 pins may be used off-board via the expansion connectors.

3•2•19 PCMCIA ON - LD13

When the yellow PCMCIA ON led is lit, it indicates the following:

1) Address & strobe buffers are driven towards the PCMCIA card
2) Data buffers may be driven to / from the PCMCIA card depending on the CE1A~ and CE2A~ signals and transfer direction.
3) Card status lines are driven towards the MPC from the PCMCIA card.

When it is dark, it indicates that all the above buffers are tri-stated and the pins associated with PCMCIA channel A, may be used off-board via the expansion connectors.

3•2•20 RS232 Port 2 ON - LD14

When the yellow RS232 Port 2 ON led is lit, it designates that the RS232 transceiver connected to SMC2, is active and communication via that medium (through PB3) is allowed. When dark, it designates that the transceiver is in shutdown mode, so SMC2 pins may be used off-board via the expansion connectors.

3•2•21 5V Indicator - LD15

The yellow 5V led, indicates the presence of the +5V supply at P7.

3•2•22 3.3V Indicator - LD16

The yellow 3.3V led indicates that the 3.3V power bus is powered

3•3 MEMORY MAP

All accesses to MPC850FADSDB's memory slaves are controlled by the MPC's memory controller. Therefore, the memory map is reprogrammable to the desire of the user. After Hard Reset is performed by the debug station, the debugger checks to see the size, delay and type of the DRAM and FLASH memory mounted on board and initializes the chip-selects accordingly. The DRAM and the FLASH memory respond to all types of memory access i.e., user / supervisory, program / data and DMA.

TABLE 3-1. MPC860/860ADS Main Memory Map

ADDESS RANGE	*Memory Type*	*Device Type*				*Port Size*
00000000 - 003FFFFF	DRAM SIMM	MCM36100	MCM36200	MCM36400	MCM36800	32
00400000 - 007FFFFF	DRAM SIMM		MCM36200	MCM36400	MCM36800	32
00800000 - 00FFFFFF	DRAM SIMM			MCM36400	MCM36800	32
01000000 - 01FFFFFF	DRAM SIMM				MCM36800	32
02000000 - 020FFFFF	Empty Space					
02100000 - 02103FFF	BCSR(0:3)[a]					32[b]
02104000 - 021FFFFF	Empty Space					
02200000 - 02207FFF	MPC Internal MAP[c]					32
02208000 - 027FFFFF	Empty Space					
02800000 - 029FFFFF	Flash SIMM	MCM29F020	MCM29F040 SM732A1000A	MCM29F080 SM732A2000		32
02A00000 - 02BFFFFF			MCM29F040 SM732A1000A	MCM29F080 SM732A2000		32
02C00000 - 02FFFFFF				MCM29F080 SM732A2000		32

a. The device appears repeatedly in multiples of its size. E.g., BCSR0 appears at memory locations 2100000, 2100010, 2100020..., while BCSR1 appears at 2100004, 2100014, 2100024... and so on.
b. Only upper 16 bit are in fact used.
c. Refer to the MPC860 User's Manual or to the MPC860 User's Manual for complete description of the MPC internal memory map.

3•4 Programming The MPC Registers

The MPC provides the following functions on the MPC850FADSDB:

1) DRAM Controller
2) Chip Select generator.
3) UART for terminal or host computer connection.
4) Ethernet controller.
5) Infra-Red Port Controller

6) General Purpose I/O signals.

The internal registers of the MPC must be programmed after Hard reset as described in the following paragraphs. The addresses and programming values are in hexadecimal base.

For better understanding the of the following initializations refer to the MPC860 or to the MPC860 User's Manual for more information.

TABLE 3-2. SIU REGISTERS' PROGRAMMING

Register	*Init Value[hex]*	*Description*
SIUMCR	01632440	Internal arbitration, External master arbitration priority - 0, External arbitration priority - 0, PCMCIA channel II pins - debug pins, Debug Port on JTAG port pins, FRZ/IRQ6~ - IRQ6~, debug register - locked, No parity for non-CS regions, DP(0:3)/IRQ(3:6)~ pins - DP(0:3), reservation disabled, SPKROUT - Tri-stated, BS_A(0:3)~ and WE(0:3)~ are driven just on their dedicated pins, GPL_B5~ enabled, GPL_A/B(2:3)~ function as GPLs.
SYPCR	FFFFFF88	Software watchdog timer count - FFFF, Bus-monitor timing FF, Bus-monitor - Enabled, S/W watch-dog - Freeze, S/W watch-dog - disabled, S/W watch-dog (if enabled) causes NMI, S/W (if enabled) not prescaled.
TBSCR	00C2	No interrupt level, reference match indications cleared, interrupts disabled, no freeze, time-base disabled.
RTCSC	01C2	Interrupt request level - 1, 32768 Hz source, second interrupt disabled, Alarm interrupt disabled, Real-time clock - FREEZE, Real-time clock disabled.
PISCR	0082	No level for interrupt request, Periodic interrupt disabled, clear status, interrupt disabled, FREEZE, periodic timer disabled.

3•4•1 Memory Controller Registers Programming

The memory controller on the MPC850FADSDB is initialized to 50 MHz operation. I.e., registers' programming is based on 50 MHZ timing calculation except for refresh timer which is initialized to 16.67Mhz, the lowest frequency at which the ADS may wake up. Since the ADS may be made to wake-up at 25MHz[A] as well, the initializations are not efficient, since there are too many wait-states inserted. Therefore, additional set of initialization is provided to support efficient 25MHz operation.

The reason for initializing the ADS for 50Mhz is to allow proper (although not efficient) ADS operation through all available ADS clock operation frequencies.

A. The only parameter which is initialized to the start-up frequency, is the refresh rate, which would have been inadequate if initialized to 50Mhz while board is running at a lower frequency. Therefore, for best bus bandwidth availability, refresh rate should be adapted to the current system clock frequency.

Warning

Due to availability problems with few of the supported memory components, the below initializations were not tested with all parts. Therefore, the below initializations are liable to CHANGE, throughout the testing period.

TABLE 3-3. Memory Controller Initializations For 50Mhz

Register	*Device Type*	*Init Value [hex]*	*Description*
BR0	All Flash SIMMs supported.	02200001	Base at 2200000, 32 bit port size, no parity, GPCM
OR0	MCM29F020-90	FFE00D34	2MByte block size, all types access, CS early negate, 6 w.s., Timing relax
	MCM29F040-90 SM732A1000A-9	FFC00D34	4MByte block size, all types access, CS early negate, 6 w.s., Timing relax
	MCM29F080-90 SM732A2000-9	FF800D34	8MByte block size, all types access, CS early negate, 6 w.s., Timing relax
	MCM29F020-12	FFE00D44	2MByte block size, all types access, CS early negate, 8 w.s., Timing relax
	MCM29F040-12 SM732A1000A-12	FFC00D44	4MByte block size, all types access, CS early negate, 8 w.s., Timing relax
	MCM29F080-12 SM732A2000-12	FF800D44	8MByte block size, all types access, CS early negate, 8 w.s., Timing relax
BR1	BCSR	02100001	Base at 2100000, 32 bit port size, no parity, GPCM
OR1	BCSR	FFFF8110	32 KByte block size, all types access, CS early negate, 1 w.s.
BR2	All Dram SIMMs Supported	00000081	Base at 0, 32 bit port size, no parity, UPMA
OR2	MCM36100/200-60/70	FFC00800	4MByte block size, all types access, initial address multiplexing according to AMA.
	MCM36400/800-60/70 MT8/16D432/832X-6/7	FF000800	16MByte block size, all types access, initial address multiplexing according to AMA.
BR3	MCM36200-60/70	00400081	Base at 400000, 32 bit port size, no parity, UPMA
	MCM36800-60/70 MT16D832X-6/7	01000081	Base at 1000000, 32 bit port size, no parity, UPMA
OR3	MCM36200-60/70	FFC00800	4MByte block size, all types access, initial address multiplexing according to AMA
	MCM36800-60/70 MT16D832X-6/7	FF000800	16MByte block size, all types access, initial address multiplexing according to AMA.
MPTPR	All Dram SIMMs Supported	0400	Divide by 16 (decimal)

TABLE 3-3. Memory Controller Initializations For 50Mhz

Register	*Device Type*	*Init Value [hex]*	*Description*
MAMR	MCM36100-60/70	40A21114[a] 60A21114[b] C0A21114[c]	refresh clock divided by 40[a] or 60[b] or C0[c], periodic timer enabled, type 2 address multiplexing scheme, 1 cycle disable timer, GPL4 disabled for data sampling edge flexibility, 1 loop read, 1 loop write, 4 beats refresh burst.
	MCM36200-60/70	20A21114[a] 30A21114[b] 60A21114[c]	refresh clock divided by 20[a] or 30[b] or 60[c], periodic timer enabled, type 2 address multiplexing scheme, 1 cycle disable timer, GPL4 disabled for data sampling edge flexibility, 1 loop read, 1 loop write, 4 beats refresh burst.
	MCM36400-60/70 MT8D432X-6/7	40B21114[a] 60B21114[b] C0B21114[c]	refresh clock divided by 40[a] or 60[b] or C0[c], periodic timer enabled, type 3 address multiplexing scheme, 1 cycle disable timer, GPL4 disabled for data sampling edge flexibility, 1 loop read, 1 loop write, 4 beats refresh burst.
	MCM36800-60/70 MT16D832-6/7	20B21114[a] 30B21114[b] 60B21114[c]	refresh clock divided by 20[a] or 30[b] or 60[c], periodic timer enabled, type 3 address multiplexing scheme, 1 cycle disable timer, GPL4 disabled for data sampling edge flexibility, 1 loop read, 1 loop write, 4 beats refresh burst.

a. Assuming 16.67 MHz BRGCLK.
b. Assuming 25MHz BRGCLK
c. For 50MHz BRGCLK

TABLE 3-4. UPMA Initializations for 60nsec DRAMs @ 50MHz

Cycle Type		Single Read	Burst Read	Single Write	Burst Write	Refresh	Exception
Offset in UPM		0	8	18	20	30	3C
Contents @ Offset +	0	8FFFEC24	8FFFEC24	8FAFCC24	8FAFCC24	C0FFCC84	33FFCC07
	1	0FFFEC04	0FFFEC04	0FAFCC04	0FAFCC04	00FFCC04	X
	2	0CFFEC04	08FFEC04	0CAFCC00	0CAFCC00	07FFCC04	X
	3	00FFEC04	00FFEC0C	11BFCC47	03AFCC4C	3FFFCC06	X
	4	00FFEC00	03FFEC00	X	0CAFCC00	FFFFCC85	
	5	37FFEC47	00FFEC44	X	03AFCC4C	FFFFCC05	
	6	X	00FFCC08	X	0CAFCC00	X	
	7	X	0CFFCC44	X	03AFCC4C	X	
	8		00FFEC0C		0CAFCC00	X	
	9		03FFEC00		33BFCC4F	X	
	A		00FFEC44		X	X	
	B		00FFCC00		X	X	
	C		3FFFC847		X		
	D		X		X		
	E		X		X		
	F		X		X		

TABLE 3-5. UPMA Initializations for 70nsec DRAMs @ 50MHz

Cycle Type		Single Read	Burst Read	Single Write	Burst Write	Refresh	Exception
Offset In UPM		0	8	18	20	30	3C
Contents @ Offset +	0	8FFFCC24	8FFFCC24	8FAFCC24	8FAFCC24	E0FFCC84	33FFCC07
	1	0FFFCC04	0FFFCC04	0FAFCC04	0FAFCC04	00FFCC04	X
	2	0CFFCC04	0CFFCC04	0CAFCC00	0CAFCC00	00FFCC04	X
	3	00FFCC04	00FFCC04	11BFCC47	03AFCC4C	0FFFCC04	X
	4	00FFCC00	00FFCC08	X	0CAFCC00	7FFFCC06	
	5	37FFCC47	0CFFCC44	X	03AFCC4C	FFFFCC85	
	6	X	00FFEC0C	X	0CAFCC00	FFFFCC05	
	7	X	03FFEC00	X	03AFCC4C	X	
	8		00FFEC44		0CAFCC00	X	
	9		00FFCC08		33BFCC47	X	
	A		0CFFCC44		X	X	
	B		00FFEC04		X	X	
	C		00FFEC00		X		
	D		3FFFEC47		X		
	E		X		X		
	F		X		X		

TABLE 3-6. UPMA Initializations for 60nsec EDO DRAMs @ 50MHz

Cycle Type		Single Read	Burst Read	Single Write	Burst Write	Refresh	Exception
Offset in UPM		0	8	18	20	30	3C
Contents @ Offset +	0	8FFBEC24	8FFFEC24	8FFFCC24	8FFFCC24	C0FFCC84	33FFCC07
	1	0FF3EC04	0FFBEC04	0FEFCC04	0FEFCC04	00FFCC04	X
	2	0CF3EC04	0CF3EC04	0CAFCC00	0CAFCC00	07FFCC04	X
	3	00F3EC04	00F3EC0C	11BFCC47	03AFCC4C	3FFFCC06	X
	4	00F3EC00	0CF3EC00	X	0CAFCC00	FFFFCC85	
	5	37F7EC47	00F3EC4C	X	03AFCC4C	FFFFCC05	
	6	X	0CF3EC00	X	0CAFCC00	X	
	7	X	00F3EC4C	X	03AFCC4C	X	
	8		0CF3EC00		0CAFCC00	X	
	9		00F3EC44		33BFCC4F	X	
	A		03F3EC00		X	X	
	B		3FF7EC47		X	X	
	C		X		X		
	D		X		X		
	E		X		X		
	F		X		X		

TABLE 3-7. UPMA Initializations for 70nsec EDO DRAMs @ 50MHz

Cycle Type		Single Read	Burst Read	Single Write	Burst Write	Refresh	Exception
Offset In UPM		0	8	18	20	30	3C
Contents @ Offset +	0	8FFBCC24	8FFFCC24	8FFFCC24	8FFFCC24	E0FFCC84	33FFCC07
	1	0FF3CC04	0FFBCC04	0FEFCC04	0FEFCC04	00FFCC04	X
	2	0CF3CC04	0CF3CC04	0CAFCC00	0CAFCC00	00FFCC04	X
	3	00F3CC04	00F3CC0C	11BFCC47	03AFCC4C	0FFFCC04	X
	4	00F3CC00	03F3CC00	X	0CAFCC00	7FFFCC04	
	5	37F7CC47	00F3CC44	X	03AFCC4C	FFFFCC86	
	6	X	00F3EC0C	X	0CAFCC00	FFFFCC05	
	7	X	0CF3EC00	X	03AFCC4C	X	
	8		00F3EC4C		0CAFCC00	X	
	9		03F3EC00		33BFCC47	X	
	A		00F3EC44		X	X	
	B		00F3CC00		X	X	
	C		33F7CC47		X		
	D		X		X		
	E		X		X		
	F		X		X		

TABLE 3-8. Memory Controller Initializations For 25Mhz

Register	*Device Type*	*Init Value [hex]*	*Description*
BR0	All Flash SIMMs supported.	02200001	Base at 2200000, 32 bit port size, no parity, GPCM

TABLE 3-8. Memory Controller Initializations For 25Mhz

Register	*Device Type*	*Init Value [hex]*	*Description*
OR0	MCM29F020-90	FFE00D20	2MByte block size, all types access, CS early negate, 2 w.s.
	MCM29F040-90 SM732A1000A-9	FFC00D20	4MByte block size, all types access, CS early negate, 2 w.s.
	MCM29F080-90 SM732A2000-9	FF800920	8MByte block size, all types access, CS early negate, 2 w.s., Timing relax
	MCM29F020-12	FFE00D30	2MByte block size, all types access, CS early negate, 3 w.s.
	MCM29F040-12 SM732A1000A-12	FFC00D30	4MByte block size, all types access, CS early negate, 3 w.s.
	MCM29F080-12 SM732A2000-12	FF800930	8MByte block size, all types access, CS early negate, 3 w.s.
BR1	BCSR	02100001	Base at 2100000, 32 bit port size, no parity, GPCM
OR1	BCSR	FFFF8110	32 KByte block size, all types access, CS early negate, 1 w.s.
BR2	All Dram SIMMs Supported	00000081	Base at 0, 32 bit port size, no parity, UPMA
OR2	MCM36100/200-60/70	FFC00800	4MByte block size, all types access, initial address multiplexing according to AMA.
	MCM36400/800-60/70 MT8/16D432/832X-6/7	FF000800	16MByte block size, all types access, initial address multiplexing according to AMA.
BR3[a]	MCM36200-60/70	00400081	Base at 400000, 32 bit port size, no parity, UPMA
	MCM36800-60/70 MT16D832X-6/7	01000081	Base at 1000000, 32 bit port size, no parity, UPMA
OR3	MCM36200-60/70	FFC00800	4MByte block size, all types access, initial address multiplexing according to AMA
	MCM36800-60/70 MT16D832X-6/7	FF000800	16MByte block size, all types access, initial address multiplexing according to AMA.
MPTPR	All Dram SIMMs Supported	0400	Divide by 16 (decimal)

TABLE 3-8. Memory Controller Initializations For 25Mhz

Register	*Device Type*	*Init Value [hex]*	*Description*
MAMR	MCM36100-60/70	60A21114	refresh clock divided by 60, periodic timer enabled, type 2 address multiplexing scheme, 1 cycle disable timer, GPL4 disabled for data sampling edge flexibility, 1 loop read, 1 loop write, 4 beats refresh burst.
	MCM36200-60/70	30A21114	refresh clock divided by 30, periodic timer enabled, type 2 address multiplexing scheme, 1 cycle disable timer, GPL4 disabled for data sampling edge flexibility, 1 loop read, 1 loop write, 4 beats refresh burst.
	MCM36400-60/70 MT8D432X-6/7	60B21114	refresh clock divided by 60, periodic timer enabled, type 3 address multiplexing scheme, 1 cycle disable timer, GPL4 disabled for data sampling edge flexibility, 1 loop read, 1 loop write, 4 beats refresh burst.
	MCM36800-60/70 MT16D832-6/7	30B21114	refresh clock divided by 30, periodic timer enabled, type 3 address multiplexing scheme, 1 cycle disable timer, GPL4 disabled for data sampling edge flexibility, 1 loop read, 1 loop write, 4 beats refresh burst.

a. BR3 is not initialized for 36100 or 36400 DRAM SIMMs.

TABLE 3-9. UPMA Initializations for 60nsec DRAMs @ 25MHz

Cycle Type		Single Read	Burst Read	Single Write	Burst Write	Refresh	Exception
Offset in UPM		0	8	18	20	30	3C
Contents @ Offset +	0	0FFFCC04	0FFFCC24	0FAFCC24	0FAFCC04	80FFCC84	33FFCC07
	1	08FFCC00	08FFCC00	08AFCC00	08AFCC00	13FFCC04	X
	2	33FFCC47	03FFCC4C	3FBFCC47	01AFCC48	FFFFCC87	X
	3	X	08FFCC00	X	08AFCC44	FFFFCC05	X
	4	X	03FFCC4C	X	0FAFCC08	X	
	5	X	08FFCC00	X	08AFCC44	X	
	6	X	03FFCC4C	X	0CAFCC08	X	
	7	X	08FFCC00	X	38BFCC46	X	
	8		33FFCC47		FFFFCC45	X	
	9		X		X	X	
	A		X		X	X	
	B		X		X	X	
	C		X		X		
	D		X		X		
	E		X		X		
	F		X		X		

TABLE 3-10. UPMA Initializations for 70nsec DRAMs @ 25MHz

Cycle Type		Single Read	Burst Read	Single Write	Burst Write	Refresh	Exception
Offset In UPM		0	8	18	20	30	3C
Contents @ Offset +	0	0FFFEC04	0FFFCC24	0FAFCC04	0FAFCC04	C0FFCC84	33FFCC07
	1	08FFEC04	0FFFCC04	08AFCC00	0CAFCC00	01FFCC04	X
	2	00FFEC00	08FFCC00	3FBFCC47	01AFCC4C	7FFFCC86	X
	3	3FFFEC47	03FFCC4C	X	0CAFCC00	FFFFCC05	X
	4	X	08FFCC00	X	01AFCC4C	X	
	5	X	03FFCC4C	X	0CAFCC00	X	
	6	X	08FFCC00	X	01AFCC4C	X	
	7	X	03FFCC4C	X	0CAFCC00	X	
	8		08FFCC00		31BFCC43	X	
	9		33FFCC47		X	X	
	A		X		X	X	
	B		X		X	X	
	C		X		X		
	D		X		X		
	E		X		X		
	F		X		X		

TABLE 3-11. UPMA Initializations for 60nsec EDO DRAMs @ 25MHz

Cycle Type		Single Read	Burst Read	Single Write	Burst Write	Refresh	Exception
Offset in UPM		0	8	18	20	30	3C
Contents @ Offset +	0	0FFBCC04	0FFBCC04	0FEFCC04	0FEFCC04	80FFCC84	33FFCC07
	1	0CF3CC04	09F3CC0C	08AFCC04	08AFCC00	13FFCC04	X
	2	00F3CC00	09F3CC0C	00AFCC00	07AFCC48	FFFFCC87	X
	3	33F7CC47	09F3CC0C	0FBFCC47	08AFCC48	FFFFCC05	X
	4	X	08F3CC00	X	08AFCC48	X	
	5	X	3FF7CC47	X	39BFCC47	X	
	6	X	X	X		X	
	7	X	X	X		X	
	8		X			X	
	9		X			X	
	A		X		X	X	
	B		X		X	X	
	C		X		X		
	D		X		X		
	E		X		X		
	F		X		X		

TABLE 3-12. UPMA Initializations for 70nsec EDO DRAMs @ 25MHz

Cycle Type		Single Read	Burst Read	Single Write	Burst Write	Refresh	Exception
Offset In UPM		0	8	18	20	30	3C
Contents @ Offset +	0	0FFBCC04	0FFBEC04	0FEFCC04	0FEFCC04	C0FFCC84	33FFCC07
	1	0CF3CC04	08F3EC04	08AFCC04	08AFCC00	01FFCC04	X
	2	00F3CC00	03F3EC48	00AFCC00	07AFCC4C	7FFFCC86	X
	3	33F7CC47	08F3CC00	0FBFCC47	08AFCC00	FFFFCC05	X
	4	X	0FF3CC4C	X	07AFCC4C	X	
	5	X	08F3CC00	X	08AFCC00	X	
	6	X	0FF3CC4C	X	07AFCC4C	X	
	7	X	08F3CC00	X	08AFCC00	X	
	8		3FF7CC47		37BFCC47	X	
	9		X		X	X	
	A		X		X	X	
	B		X		X	X	
	C		X		X		
	D		X		X		
	E		X		X		
	F		X		X		

4 - Functional Description

In this chapter the various modules combining the MPC850FADSDB are described to their design details.

4•1 Reset & Reset - Configuration

There are 3 reset sources for the MPC:

1) Power-On Reset[A]
2) Hard Reset
3) Soft Reset

4•1•1 Power-On Reset

The Power - On Reset on the MPC850-FADSB is generated out of 2 alternative power buses:

1) The keep alive power bus
2) The MAIN power bus.

Selection between the 2 options is done by means of jumper.

When option (1) above is selected, the power-on reset is generated by a dedicated voltage detector made by Seiko the S-8051HN-CD-X with detection voltage range of 1.795 to 2.005V. During keep alive power-on or when there is a voltage drop of that input into the above range Power-On Reset is generated, i.e., PORESET* input of the MPC is asserted for a period of approximately 4 sec.

When option (2) above is selected, the power-on reset is generated by a dedicated voltage detector made
by Seiko the S-8052ANY-NH-X with detection voltage range of 2.595V to 2.805V. During MAIN 3.3V bus power-on or when there is a voltage drop of that input into the above range Power-On Reset is generated, i.e., PORESET* input of the MPC is asserted for a period of approximately 4 sec. The MAIN power on reset also generates power-on reset to all logic located on the motherboard.

When PORESET* is asserted to the MPC, the Power-On reset configuration is made available to MPC. See 2•1•6•1 "Power - On Reset Configuration" on page 7 of MPC8XXFADS spec.

4•1•2 Hard Reset

Hard Reset is generated to the MPC850 by the following sources:

1) The MAIN power-on reset
2) Manual Hard Reset generated on the mother board
3) The debug port Hard reset
4) and by MPC850's internal sources.

When the open-drain signal Hard Reset is asserted, Hard reset configuration is driven on the data bus by logic on the motherboard. See 2•1•6•2 "Hard Reset Configuration" on page 7 on MPC8XXFADS spec.

4•1•3 Soft Reset

Soft Reset is generated to the MPC850 by the following sources:

1) The debug port controller located on the motherboard
2) Manual Soft Reset generated on the motherboard

A. In fact generated on the daughter board.

3) and by MPC850 internal sources.

When Soft reset is generated to the MPC850, Soft Reset configuration is made available to the MPC by logic residing over the motherboard. See 2•1•6•3 "Soft Reset Configuration" on page 7 on MPC8XXFADS spec.

4•2 Interrupts

The only external interrupt which is applied to the MPC via its interrupt controller is the ABORT (NMI), which is generated by a push-button & logic residing over the motherboard.

4•3 Clock Generator

Although most of clock generator logic is found on this board, it is documented within the motherboard spec, since, it is common to all daughter boards. See 2•3 "Clock Generator" on page 8 of the MPC8XXFADS spec.

4•4 PCMCIA Port

The MPC850 has only one PCMCIA port which resides on PCMCIA port B[A] pins. It is routed to the PCMCIA port on the MPC8XXFADS. Since the default Hard Reset Configuration of the FADS, sets these pins as debug support pins, their functionality should be changed via SIUMCR to PCMCIA pins prior to this port being used.

For further information see 2•10 "PCMCIA Port" on page 20 in MPC8XXFADS spec.

4•5 Communication Ports

The MPC850 has the following communication ports:

1) USB Port which is connected on board to a USB transceiver.
2) SCC2 which may be operated either as an Ethernet port or as an Infra/Red port or as RS232 Port #2.
3) SMC1 which is connected to RS232 Port #1 of the MPC8XXFADS.
4) SMC2 which supports TDM only and will not be used on board.
5) I^2C
6) SPI, which is not used on-board.

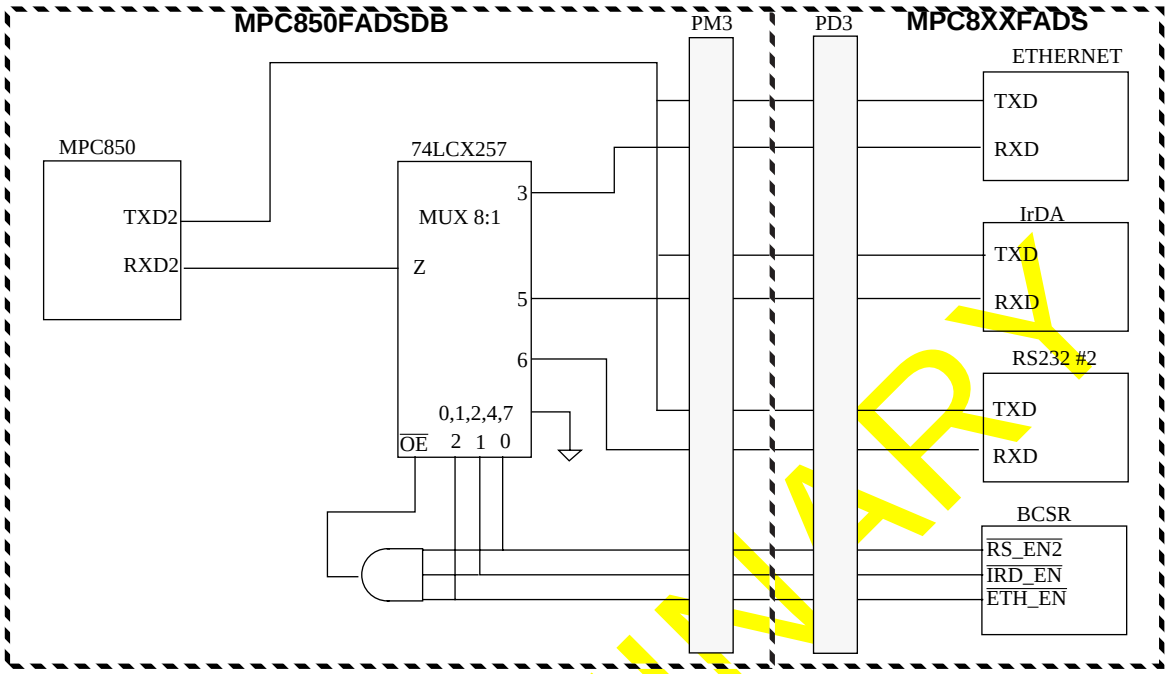
All communication ports may be enabled / disabled by S/W via BCSR1 or BCSR4. See TABLE 2-10. "BCSR1 Description" on page 26 and TABLE 2-23. "BCSR4 Description" on page 34 - both in MPC8XXFADS spec.

To protect against possible contention, the RxD lines of the Ethernet port, IrDA port and RS232 Port #2 of the MPC8XXFADS, are multiplexed to RXD2 input. The selection between the 3 RxD lines is done according to their respective enable bits in BCSR1. When ETH_EN~, IRD_EN~ or RS_EN2~ bits in BCSR1 are mutually exclusive enabled, their respective comm. port RxD line is driven to RXD2 of the MPC. If 2 or more of these lines are simultaneously enabled, '0' is driven to RXD2. When neither of them is asserted, the output of the mux is tri-stated, and RXD2 line of the MPC may be used for any alternate function.

The connection scheme of the Ethernet, IrDA and Serial Port #2 to SCC2 is shown in FIGURE 2-1 "SCC2 Connection Scheme" below:

A. In MPC860 Terms.

FIGURE 2-1 SCC2 Connection Scheme



4•5•1 USB Port

The USB port resides on the MPC850FADSDB and is driven by the USB port of the MPC. A dedicated USB transceiver - the PDIUSBP11 by PHILIPS is provided, along with a tri-state buffer, separating this port from the MPC's USB port, this to allow Port disable option and off-board use of MPC USB pins.

To correctly support the 2 speed modes of the usb, detachable pull-up resistors (3.3V) are provided over D+ and D- lines of the USB, controlled by the USB_SPD bit of BCSR4. When USB_SPD is in low-speed level (low) D- is pulled-up while D+ remains floating. When USB_SPD bit is in high-speed level, D+ is being pulled-up and D- floats.

Also, 5V power is optionally provided for the USB connector, controlled by USB_VCC0 in BCSR4. When USB_VCC0 is driven low, a 5V supply is connected to pin 1 of the USB connectors.

To support both physical connection types, two USB connectors are provided one of Type A and the other of Type B.

4•5•2 Ethernet Port

SCC2 of the MPC may be operated as an Ethernet port. Its may be connected to the ethernet transceiver on the MPC8XXFADS, provided that the ETH_EN bit in BCSR1 is asserted and both IRD_EN and RS_EN2 bits in the same register are inactive. See 2•9•1 "Ethernet Port" on page 18 and TABLE 2-10. "BCSR1 Description" on page 26 of MPC8XXFADS spec.

4•5•3 Infra-Red Port

SCC2 of the MPC may be operated as Fast IrDA port. Its may be connected to the Fast IrDA transceiver
on the MPC8XXFADS, provided that the IRD_EN bit in BCSR1 is asserted and both ETH_EN and RS_EN2
bits in the same register are inactive. See 2•9•2 "Infra-Red Port" on page 19 and TABLE 2-10. "BCSR1 Description" on page 26 of MPC8XXFADS spec.

4•5•4 RS232 Ports

There may be 2 RS232 ports with this application - RS232 Port #1 of the MPC8XXFADS is connected to SMC1 of the MPC850 while RS232 Port #2 of the FADS is optionally connected to SCC2 of the MPC850, this, when the RS_EN2 bit in BCSR1 is asserted and both ETH_EN and IRD_EN bits in the same register are inactive.

Both ports may be enabled / disabled at any time via BCSR1. See 2•9•3 "RS232 Ports" on page 19 and TABLE 2-10. "BCSR1 Description" on page 26 of the MPC8XXFADS.

4•6 Board Control & Status Register - BCSR

Most BCSR control signals and some of BCSR's status signals are available on the motherboard connectors and on the expansion connectors.

See 2•11 "Board Control & Status Register - BCSR" on page 22 of MPC8XXFADS spec.

4•7 Debug Port

The MPC850 is connected to the FADS's debug port controller through the inter-board connectors. See 2•12 "Debug Port Controller" on page 35 of the MPC8XXFADS spec.

The debug Port on the DB resides over the MPC850 JTAG port. No support is given for debug port to reside over PCMCIA port B pins.

Since VFLS(0:1) that are usually required by the debug port controller, to monitor for Run / Debug Mode status, are being used for PCMCIA port B, use is done with the FRZ signal which is connected to debug port controller on the MPC8XXFADS.

4•8 Communication Ports Expansion

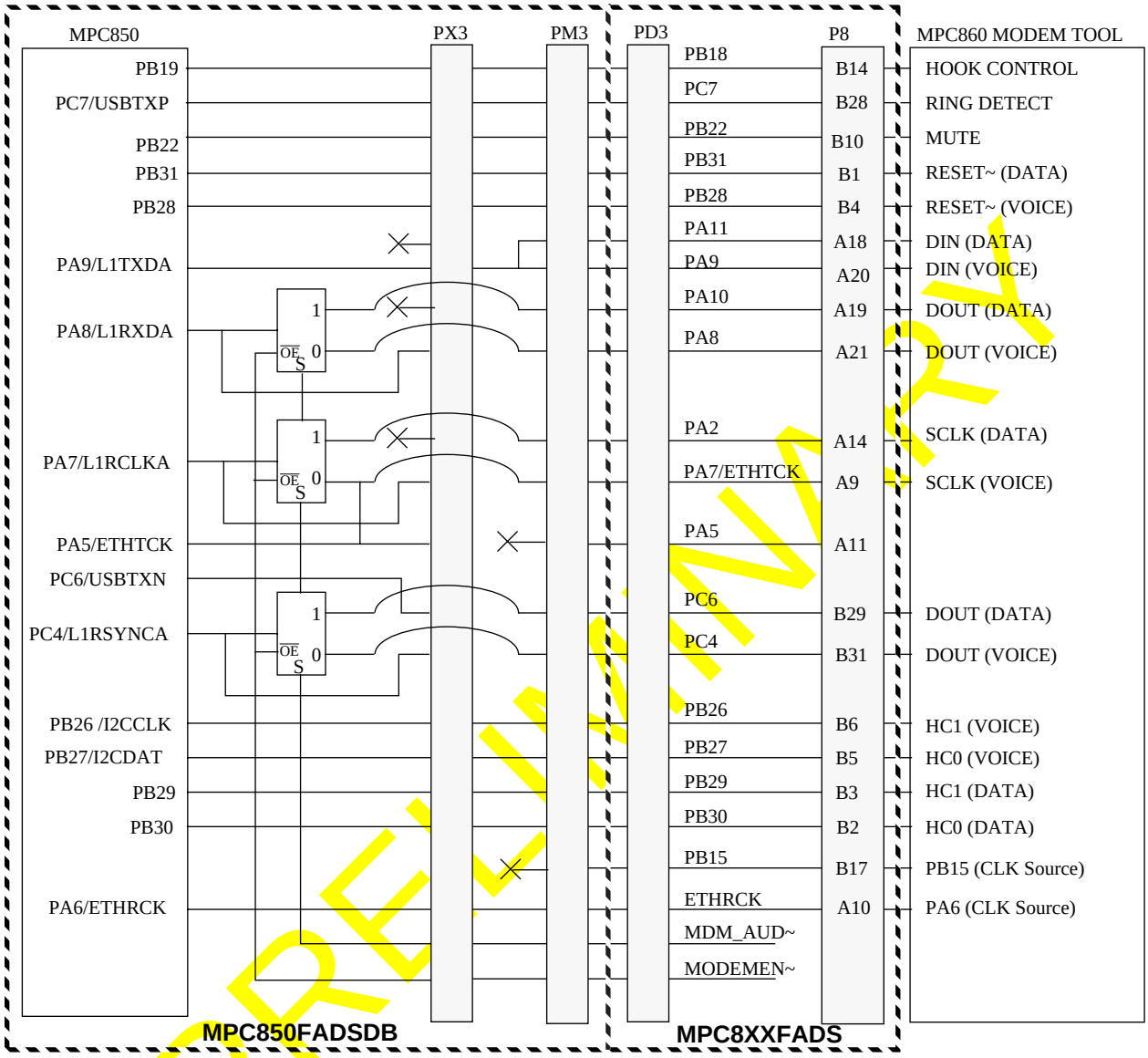
On the MPC8XXFADS, all MPC821 or MPC860 communication ports' pins were available at a 96 pins DIN 41612 connector - designated as P8. This connectors is compatible with P13 of the MPC850FADSDB. With the MPC850, which has different and partial comm. ports the pin assignment of this different and any tool made for this connector, should be examined carefully prior to being connected to the MPC8XXFADS, having the MPC850AFDSDB connected to it.

4•8•1 MPC860 Modem Tool Support

The MPC860 modem tool used the MPC860's TSA port A and port B. The MPC850 has only one TSA port. Therefore, in order to the support that tool, the data portion of the tool, which originally used TSA port B is now multiplexed with the voice part, so, both, reside on TSA port A of the MPC850. To support this multiplexing two additional signals are introduced from the FADS: MODEM_EN which enables the mux and MDM_AUD~ which selects between the data and voice codecs of the modem tool.

The modem tool support logic is described in FIGURE 2-2 "Modem Tool Support Logic Description" below.

FIGURE 2-2 Modem Tool Support Logic Description



As can be seen from FIGURE 2-2 "Modem Tool Support Logic Description" above, the following should be noticed prior to modem tool may be operated:

1) The Ethernet and USB ports need to be disabled[A] since they use few lines that are common to the modem application.
2) Hook control is done by PB19 instead of PB18 with MPC860.
3) MODEM_EN bit in BCSR4 should be asserted. See TABLE 2-23. "BCSR4 Description" on page 34 in MPC8XXFADS spec.
4) One of the optional clock sources for the modem, with the MPC860, was PB15 which does not exist with the MPC850. Since with the working application it was not used at all, no replacement was provided for this signal and it remains un-connected.

A. i.e., their respective enable bits in BCSR1 and BCSR4 should be negated.

5) To select between the voice and data portions of the modem the MDM_AUD~ bit in BCSR4 (See TABLE 2-23. "BCSR4 Description" on page 34 of the FADS spec) should be set correctly.

4•9 Switches, Jumpers and Indicators

The switches and jumpers on the MPC850FADSDB include the following:

1) Keep Alive Power Source Selection
2) VDDL Power Source Selection
3) MPC Current Measurement Jumper[A]
4) Power-On Reset Source Selection.

Since most of the board's logic is controlled via the BCSR and it is not visible whether a module is enabled or disabled as if control was done by a switch. Therefore each module has its own visible enable indicator. The following indicators will be on the MPC850FADSDB:

1) 3.3V Power - On
2) USB Port Enabled
3) USB Port Power On.

A. Soldered on-board.

5 - Memory Map

See TABLE 3-1. "MPC8XXADS Main Memory Map" on page 41 of the MPC8XXFADS spec.

6 - Physical

6•1 Power

See 4•1 "Power" on page 42 of the MPC8XXFADS Spec.

6•2 Connectors

The MPC850FADSDB has connectors attached, to serve the following functions:

1) Keep Alive Power input
2) Mother Board connection
3) H/W Expansion
4) Logic Analyzer connection
5) USB Type A and B

6•2•1 Keep Alive Power Connector

To allow connection of an external keep alive power source (e.g.: a battery) a 3 pin jumper is provided. On its factory setup, it is connected to the 3.3V power bus. Once the fabricated jumper is removed, external keep alive power may be applied through pins 2 (+) and 3 (-) of that jumper.

6•2•2 Mother Board Connectors

To provide a solid connection between the MPC850FADSDB daughter board to the MPC8XXFADS motherboard, a set of four 140 pins, 0.635mm pitch, dual row SMT connectors - Molex 53481-1409, is provided. These connectors carry all necessary MPC signals, Power buses and other control / status signals.

Since the system is to function at high operation frequencies, the connectors surround the MPC socket on the daughter board in a quadratic shape, so that short routs between the MPC and FADS's bus slaves are achieved. To avoid cross-talk interferences between connectors' signals, heavy grounding will be provided over these connectors.

6•2•3 H/W Expansion Connectors

To facilitate H/W expansion from the DB, a set of connectors matching the daughter boards connectors of the mother board (See 4•2•3 "Daughter Board Connectors" on page 44 of MPC8XXFADS spec), is provided on top of the DB.

6•2•4 Logic Analyzer Connector

To provide fast connection option to HP 165XX logic analyzers, a set of 6 high density 38 pin MICTOR connectors, Amp - 2-767004-2, is furnished, carrying all MPC850 functional signals.

6•2•5 USB Port Connector

Two connectors are provided one USB Type A and the other USB type B. Amp 787616-1 and Amp 787780-1.