



PowerPC™

Errata to MPC860T (Rev. D) Fast Ethernet Controller Supplement

This errata describes corrections to revision 0.8 of the *MPC860T (Rev. D) Fast Ethernet Controller Supplement to the MPC860 PowerQUICC User's Manual*. The section and page number of new errata items added since the last errata addendum (10/1999) are boldfaced.

- 2.1, 2-2 Table 2-1. FEC Signal Descriptions. RTS3 and RTS4 should be $\overline{\text{RTS3}}$ and $\overline{\text{RTS4}}$, indicating they are active low.
- 3.2, 3-3 FEC Frame Transmission. First sentence says there is no truncation when a transmit frame exceeds the set value. This should be changed to say that truncation will occur if the frame exceeds 2,048 bytes.
- 3.6, 3-5 Figure 3-1, Ethernet Address Recognition Flowchart. At “Promiscuous Mode?” the indication for a False condition should be (R_CNTRL[PROM] = 0.)
- 4.1, 4-1 Port D Pin Functions—There is a typographical error in the first sentence of the third paragraph of this section. It should begin as follows:

‘PD[11:8] peripheral functions...’
- 4.1, 4-2 Table 4-1. Port D Pin Assignment. RTS3, RTS4, REJECT2, REJECT3, and REJECT4 should be $\overline{\text{RTS3}}$, $\overline{\text{RTS4}}$, $\overline{\text{REJECT2}}$, $\overline{\text{REJECT3}}$, and $\overline{\text{REJECT4}}$, indicating they are active low.
- 4.1.2, 4-2 Enabling MII Mode. Add the following:

3. Set ECNTRL[FEC_PINMUX]; see 6.2.8.
- 6.2.19, 6-19 DMA Function Code Register (FUN_CODE)—The FEC does not support PowerPC little-endian byte ordering. Replace Table 6-21 with the following:

Table 6–21. FUN_CODE Field Descriptions

Bits	Name	Description
0	—	Reserved. This bit reads as zero.
1–2	DATA_BO	Byte order. Supplied to the SDMA interface during receive and transmit data DMA transfers. 0x Reserved 1x Big-endian (Motorola) or true little-endian (DEC or Intel) byte ordering. Considering each word in the buffer, data bytes are received or transmitted from address 0b00 to 0b11. This is because communication is byte-oriented, and byte reads and writes are identical in big- and little-endian modes
3–4	DESC_BO	The byte order field supplied to the SDMA interface during receive and transmit open descriptor DMA transfers, and during close descriptor DMA transfers. 0x Reserved 1x Big-endian (Motorola) or true little-endian (DEC or Intel) byte ordering. Considering each word in the buffer, data bytes are received or transmitted from address 0b00 to 0b11. This is because reception or transmission in communications is byte-oriented and byte reads and writes are identical in big-endian and little-endian modes.
5–7	FC	The function code field supplied to the SDMA interface during all DMA transfers.
8–31	—	Reserved. These bits read as zero.

Freescale Semiconductor, Inc.**Section #/Page #****Changes****6.2.20, 6-19**

Receive Control Register (R_CNTRL). Figure 6-20. R_CNTRL Register. The address of this register is incorrect in the figure. The initial location is 0xF44, and the second word is at 0xF46.

6.3.2.2. 6-23

User Initialization. Title says (after Asserting ECNTRL[ETHER_EN]). It should be (after Setting ECNTRL[ETHER_EN]).

6.4.2, 6-27

Table 6-29. Transmit Buffer Descriptor (TXBD) Field Descriptions. The entry for Data Length should be as follows:

Data length, written by user and never by the FEC. Indicates the number of octets the FEC should send from this BD's buffer, up to a maximum of 2,048 bytes. The DMA engine uses bits 5-15. Bits 0-4 are ignored

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