PTKIT8101UG
Rev. 1, 9/2005

MSC8101 Packet Telephony Farm Card (MSC8101PFC)

The MSC8101 DSP subsystem on the MSC8101 packet telephony farm card (MSC8101PFC) performs the signal processing functions for voice, fax, and modem data applications. The heart of the DSP subsystem is the Freescale StarCore™-based MCS8101 DSP device. Typical functions performedon the farm card include voice compression, DTMF detection, voice activity detection, echo cancellation, silence suppression, as well as modem and fax data modulation and demodulation.

Figure 1 shows the major devices on the MSC8101PFC card.

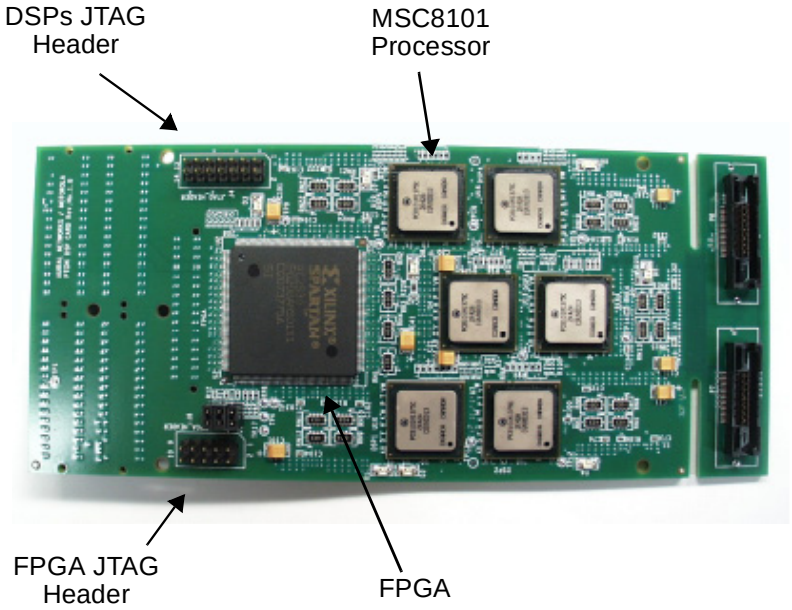


Figure 1. MSC8101PFC Card

CONTENTS

1 Packet Telephony Development Kit

The Packet Telephony Development Kit (PDK) is a platform for evaluating and developing voiceover packet applications. The PDK has an MPC8260 host network processor that runs Linus, StarCore™ DSP resource cards that run DSP code, and a Public Switched Telephone Network (PSTN) card with interfaces such as E1/T1 and analog telephone lines (see **Figure 2**).

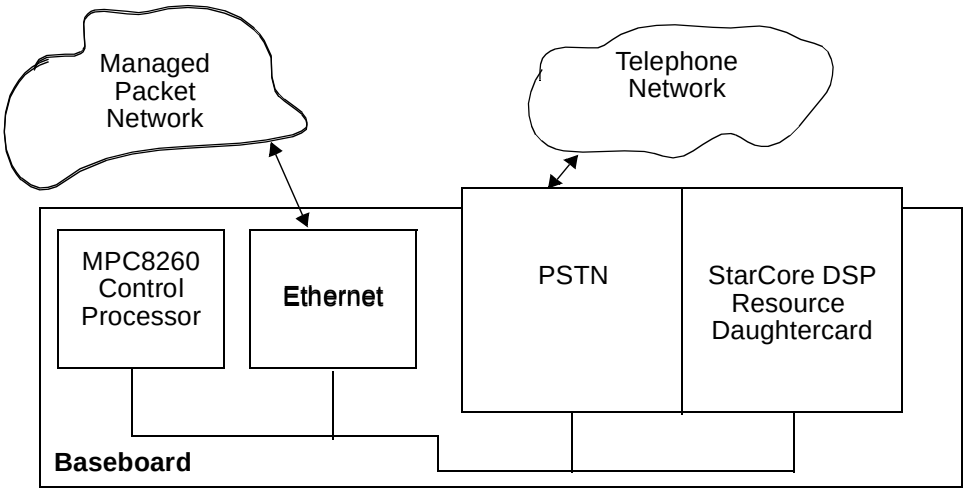


Figure 2. Components of the Packet Telephony Development Kit (PTK)

The documentation for the kit components is listed in **Table 1**.

Table 1. PTK Components and Their Associated Documents

Component	Document	Document ID
Baseboard	Packet Development Kit Baseboard Hardware User's Guide	PTKITBASEUG
MPC8260 Control Processor	*MPC8260 PowerQUICC II™ Family Reference Manual* (Available at the website listed on the back page of this document.)	MPC8260UM
PSTN Card	*Packet Development Kit PSTN Card User's Guide*	PTKITPSTNUG
StarCore DSP Resource Daughtercard	• *MSC8102 Packet Telephony Farm Card (MSC8102PFC) User's Guide* • *MSC8101 Packet Telephony Farm Card (MSC8101PFC) User's Guide*	PTKIT8101UG PTKIT8102UG
MSC8101 Processor	*MSC8101 Reference Manual* and other MSC8101 documentation are located at the web site listed on the back page of this user's guide.	MSC8101RM
Software	*Packet Telephony Development Kit Software User's Guide*	PTKITSOFTUG

CAUTION: The Packet Telephony Development Kit includes open-construction printed circuit boards that contain static-sensitive components. These boards are subject to damage from electrostatic discharge (ESD). To prevent such damage, you must use static-safe work surfaces and grounding straps, as defined in ANSI/EOS/ESD S6.1 and ANSI/EOS/ESD S4.1. All handling of these boards must be in accordance with ANSI/EAI 625.

2 Getting Started With the MSC8101PFC

First, unpack the equipment from the shipping carton. Refer to the packing list and verify that all items are present. Save the packing material for storing and reshipping the equipment. If the shipping carton is damaged upon receipt, request the carrier's agent to be present during unpacking and inspection of equipment.

CAUTION: Avoid touching areas of integrated circuitry; static discharge can damage circuits.

Most systems have an MSC8101PFC card already attached to the baseboard. If you have purchased an MSC8101PFC card separately, you must plug it in. The MSC8101PFC card cannot operate as a stand-alone unit.

The procedure for bringing up the MSC8101PFC is as follows:

1. Ensure that the PDK baseboard power supply is turned OFF.
2. Ensure that the stands off are connected to the MSC8101PFC card.
3. Gently connect the MSC8101PFC card PTMC connectors to the PDK baseboard.
4. Twist and tighten the MSC8101PFC card stands off to baseboard.
5. Ensure that the MSC8101PFC card is properly placed on top of the PDK baseboard.
6. Ensure that the PDK baseboard T3 is populated to supply 1.6V to the MSC8101PFC card.
7. The power supply can now be turned ON.

3 MSC8101PFC Hardware Components

The main hardware components of the MSC8101PFC are an MSC8101 processor, a field-programmable gate array (FPGA), an SDRAM, JTAG, clocks, and a DSP card connector.

3.1 MSC8101 Processor

The MSC8101 processor integrates on a single device the high-performance StarCore™ SC140 four-ALU DSP core along with 512 KB of internal memory, a communications processor module (CPM), a 64-bit 60x-compatible system bus and many other features (see **Figure 3**). The MSC8101 processor can execute up to four multiply-accumulate (MAC) operations in a single clock cycle. The MSC8101 CPM is a 32-bit RISC-based communications protocol engine that can network to Time-Division Multiplexed (TDM) highways, Ethernet, and Asynchronous Transfer Mode (ATM) backbones. The large internal memory, 512 KB, reduces the need for external program and data memories. The MSC8101 device offers 1500 MMACS performance using an internal 300 MHz clock with a 1.6 V core and independent 3.3 V input/output (I/O).

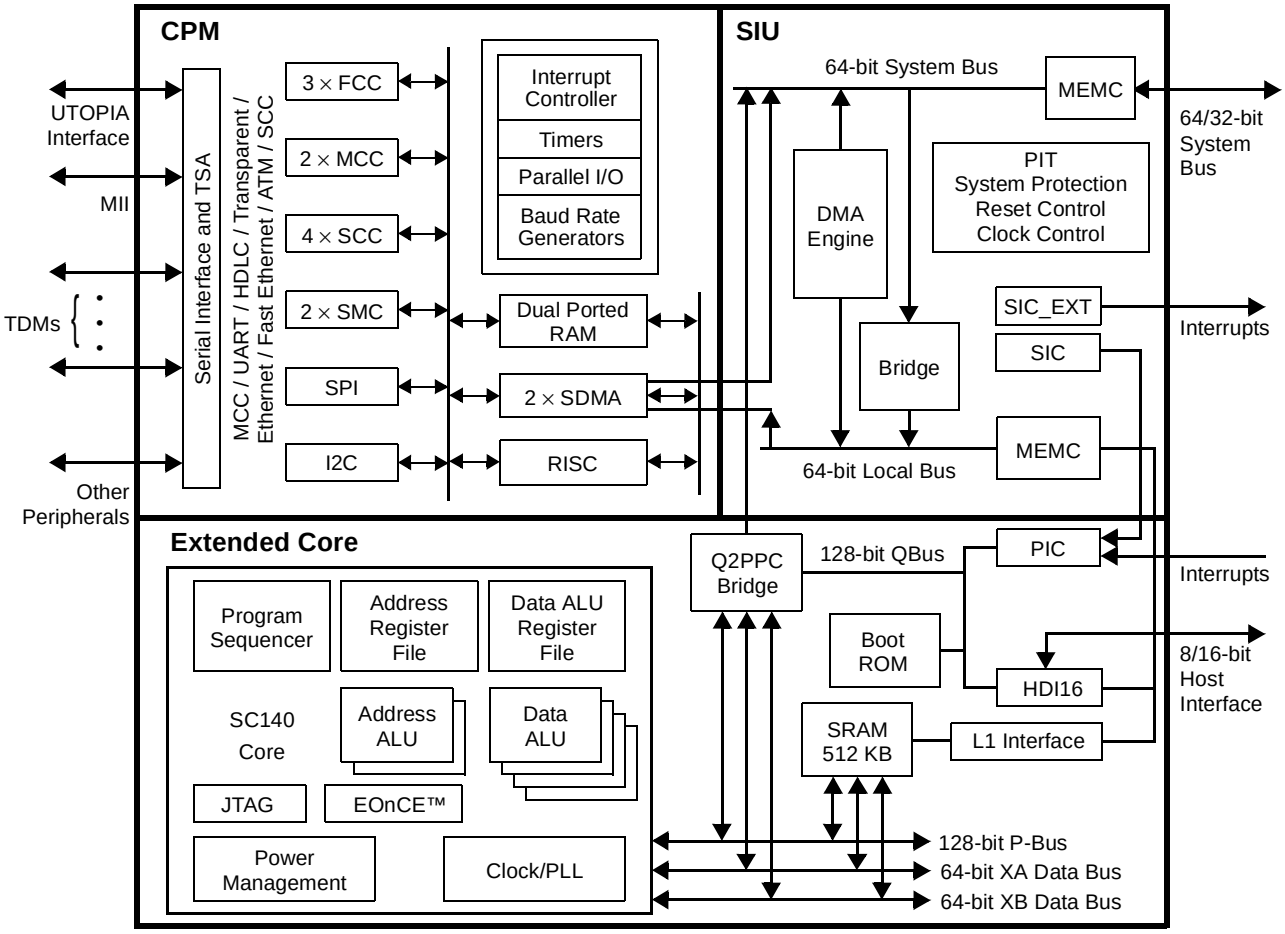


Figure 3. MSC8101 Block diagram

3.2 FPGA

The FPGA (XC2S30-PQ208) handles bus transactions between the host (MPC8260) and the DSP farm, buffers the host interface, implements the logic needed to select between DSPs, and controls DSP reset. FPGA software is available as part of the PDK software suite.[1] **Figure 4** shows an overview of all signals and devices that connect to the FPGA.

1. For a description of FPGA firmware, see the Packet Telephony Development Kit (PDK) Software User's Guide.

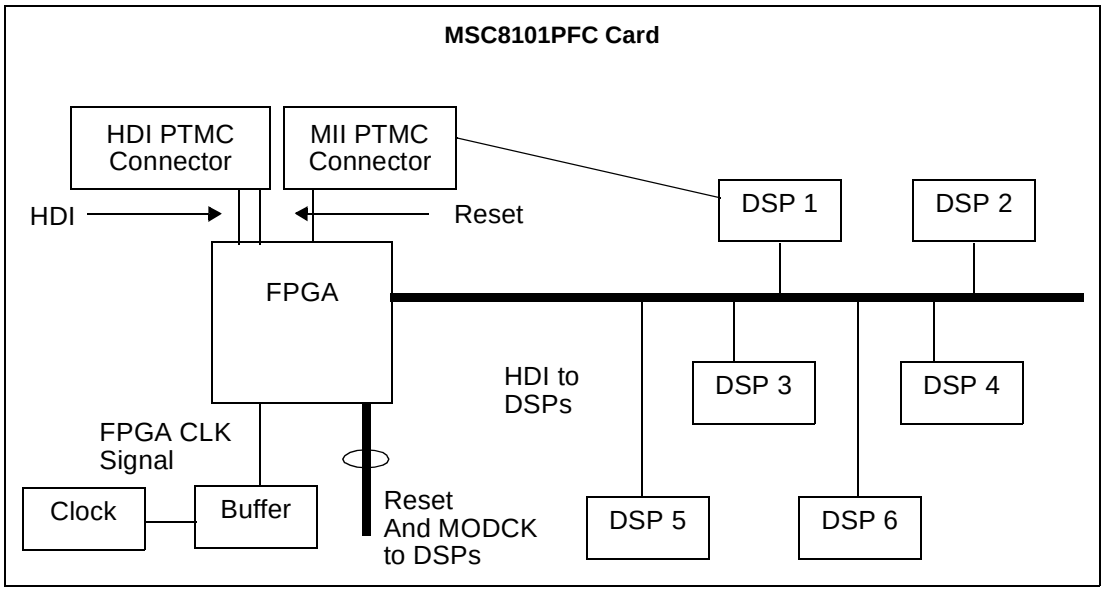


Figure 4. Device and Signals that Connect to FPGA

3.3 SDRAM

The KM432S2030C is an 8 MB Samsung SDRAM that resides on the system bus of each MSC8101. There are six identical SDRAMs, and each is programmed via its affiliate MSC8101 SDRAM memory controller. **Table 2** shows the SDRAM signals on the MSC8101 side and SDRAM side. **Table 3** lists the SDRAM Base and Option Register settings.

Table 2. SDRAM Signals

MSC8101 Signals	KM432S2030C Signals
$\overline{\text{CS}}$ [2]	$\overline{\text{CS}}$
$\overline{\text{PSDRAS}}$	$\overline{\text{RAS}}$
$\overline{\text{PSDCAS}}$	$\overline{\text{CAS}}$
D[0–31]	DQ[0–31]
A[29–20]	A[0–9]
$\overline{\text{PSDWE}}$	$\overline{\text{WE}}$
PSDA10	A10/AP
$\overline{\text{PSDDQM}}$[0–3]	DQM[0–3]
BNKSEL2	BA0
BNKSEL1	BA1
DSP_SDRAM_CLK	CLK

Table 3. SDRAM Option and Base Registers

Register	Value
SDRAM Base Register (BR2)	0x20001841
SDRAM Option Register (OR2)	0xFF803280

Perform the following steps to initialize each of the six identical SDRAMs:

1. Program the Base register (BR2) and the option register(OR2) as well MPTPR and LSRT with the following values:

   LSRT = 0x13

   MPTPR = 0x2100

   BR2 = 0x20001841

   OR2 = 0xFF803280

2. Program the SDRAM PSDMR register to precharge all banks:

   PSDMR = 0xC2849312

3. Write to a byte of memory in SDRAM
4. Program the SDRAM PSDMR registers to issue eight refreshes:

   PSDMR = 0xAA849312

5. Write to a byte of memory in SDRAM for every refresh:

   0x20000020 = 0x0

6. Program the PSDRM register to Program mode register:

   PSDMR = 0x8A849312

7. Write eight bytes of memory in SDRAM:

   0x20000000 = 0x0
   0x20000000 = 0x0
   0x20000000 = 0x0
   0x20000000 = 0x0
   0x20000000 = 0x0
   0x20000000 = 0x0
   0x20000000 = 0x0
   0x20000000 = 0x0

8. Program the LSDRAM register to operate in Normal mode:

   PSDMR = 0x9A849312

9. Write to a byte of memory in SDRAM:

   0x2000008C = 0x0

10. Finish Initialization:

    PSDMR = 0xC2849312
    OR2 = 0xFF803280
    BR2 = 0x20001841
    PSDMR = 0xC2849312
    PSRT = 0x13

3.4 Power

The MSC8101PFC card gets power from the baseboard. The baseboard provides 3.3 V for I/O power, 1.6 V for the MSC8101 DSP core supply, and 2.5 V for the FPGA core supply. Ensure that T3 on the PDK baseboard is populated to supply 1.6 V to the MSC8101PFC card and that J32 on the baseboard has no shunt.

3.5 JTAG Test Access Port (TAP)

This section discusses the configurations for both the DSP and the FPGA JTAG signals.

3.5.1 DSP JTAG TAP Signals

All DSP devices share a common JTAG TAP header (J4) on the MSC8101PFC card. The header JTAG signals can be used in various configurations. **Table 4** shows the configurations for two groups of signals that can be configured for the J4 (JTAG header).

Table 4. JTAG Signals

Header JTAG Signals	DSP JTAG Signals (Default Configuration)	Unified DSP JTAG Signals (Optional Configuration)
Local $\overline{\text{TRST}}$	$\overline{\text{DSP\_TRST}}$	$\overline{\text{PMC\_TRST}}$
Local TCK	DSP_TCK	PMC_TCK
Local TMS	DSP_TMS	PMC_TMS
Local TDO	DSP_TDO	PMC_TDO
Local TDI	DSP_TDI	PMC_TDI

Currently, the unify JTAG chain is not configured for operation, but you can unify the MSC8101PFC DSP JTAG chain and baseboard JTAG chain by populating the R229, R230, R232, R234, and R236 resistors on the MSC8101PFC card. These resistors are currently depopulated. To unify the JTAG chain between the MSC8101PFC card and the baseboard, the configuration settings in the MSC8101PFC card must match the MSC8101 JTAG chain in **Figure 5** and the hardware connections in **Figure 6**. You are advised to adjust J6 (baseboard JTAG chain) to include the DSP card in the baseboard JTAG chain. The schematics also show resistors that can be populated and depopulated to cut DSPs out of the scan chain.

Note: The baseboard JTAG chain must be configured to add the PSTN JTAG with the baseboard JTAG chain. Refer to the baseboard user's manual for details on the JTAG chain configuration.

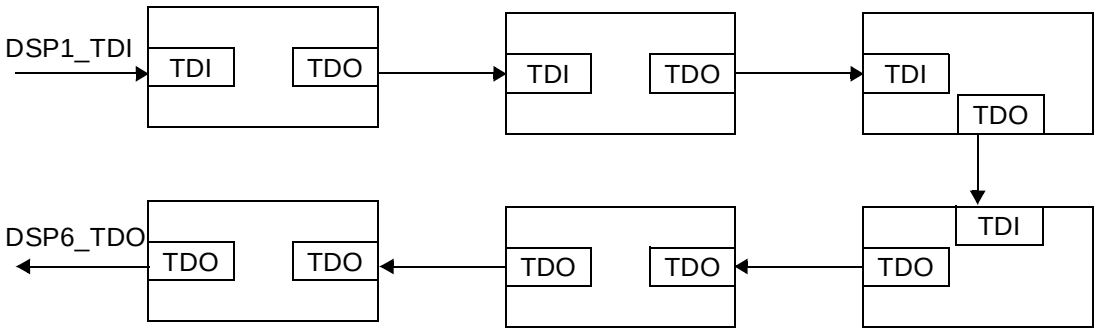


Figure 5. MSC8101PFC JTAG Chain

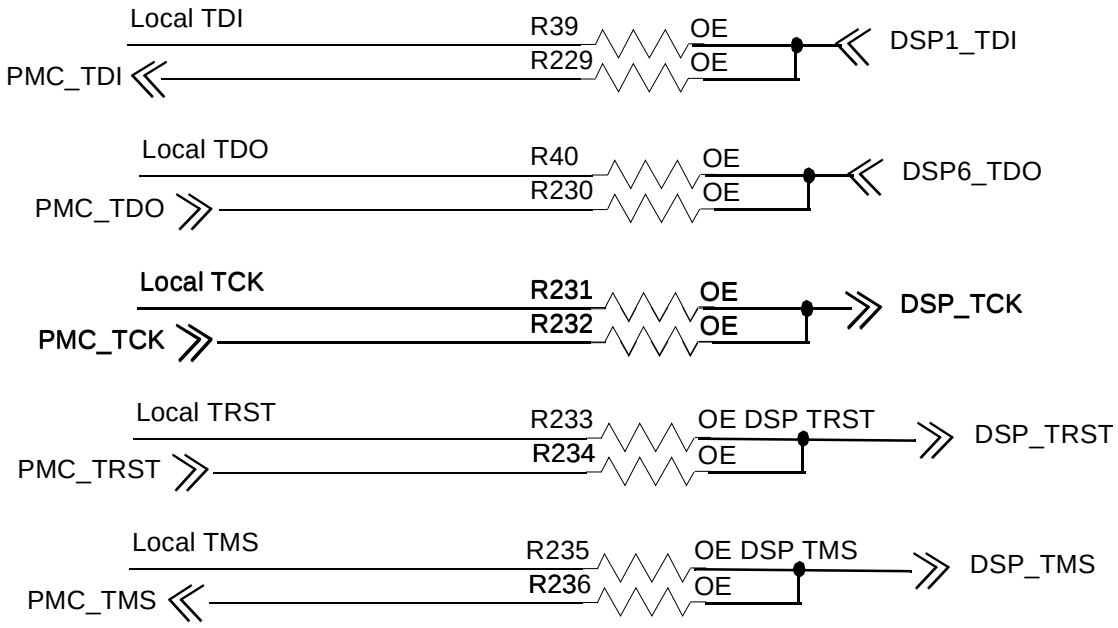


Figure 6. Unifying MSC8101PFC and Baseboard JTAG Chain

3.5.2 FPGA JTAG Signals

The JTAG signals are listed in **Table 5**. These signals to the header J6 (FPGA JTAG header) can be used to program and debug the PFGA with the Xilinx wiggler. Under normal operation, the host processor programs the FPGA.

Table 5. FPGA Programming Header Signals

FPGA Header Signals	FPGA Signals
FPGA_TCK	TCK
FPGA_TMS	TMS
FPGA_TDO	TDO
FPGA_TDI	TDI
FPGA_CCLK	CCLK
FPGA_DONE	I/O, DIN, DO
FPGA_DIN	PROGRAM
FPAG_PROGRAM	DONE

3.6 Clocks

All DSP devices and FPGA on the MSC8101PFC card have one clock source. A crystal oscillator is fed into IDTCSPF2510C (a buffer device) that generates six output clocks. **Table 6** summarizes the input and output clocks of the MSC8101PFC card.

Table 6. FPGA Programming Header Signals

Input Source	Output Source
55 MHz Source	DSP1_CLK
	DSP2_CLK
	DSP3_CLK
	DSP4_CLK
	DSP5_CLK
	DSP6_CLK
	FPGA_CLK

All SDRAM clocks are fed from their affiliate MSC8101 CLKOUT. The MSC8101 processor has input and output clock sources. The MSC8101 clock source is fed from the IDTCSPF2510C (clock buffer) and the MSC8101 output CLK is fed into SDRAM input CLK. See **Figure 7**.

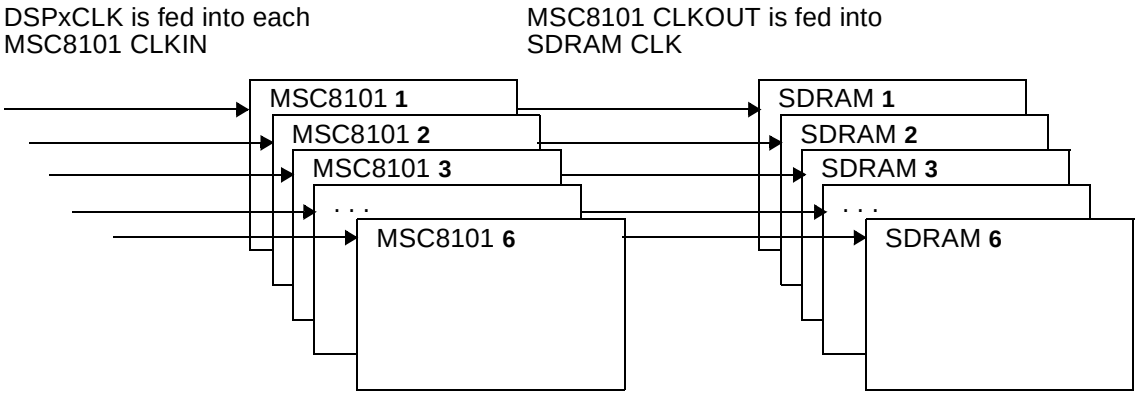


Figure 7. MSC8101 CLKIN and CLKOUT

3.7 DSP Card Connector

There are five PTMC connectors on the MSC8101PFC card. Each PTMC connector enables services between the baseboard and the MSC8101PFC card. PTMC P2 carries HDI signals, P3 carries TDM signals, P4 carries UTOPIA signals, P5 carries MII signals, and P1 carries FPGA signals. Refer to **Figure 8** for the locations of the PTMC connectors on the MSC8101PFC card.

Note: The 8101PFC card must be connected to the baseboard PTMC connectors so that these signals can be carried to/from the baseboard. The power to the baseboard must be turned ON.

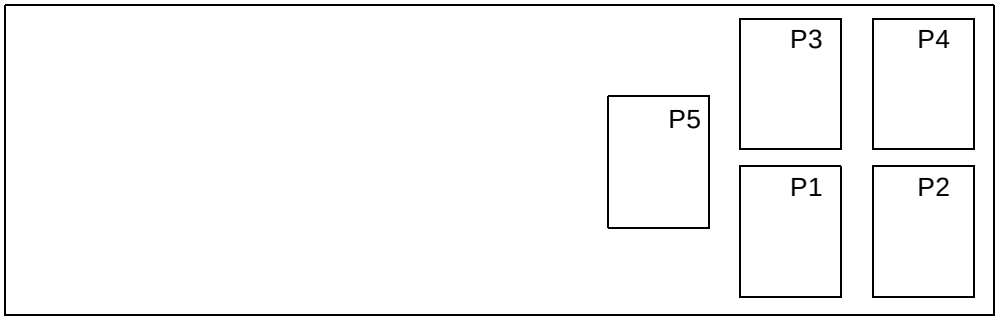


Figure 8. Baseboard PTMC Connector

3.7.1 HDI Signals

The PTMC P2 connector carries and enables HDI16 traffic between the MPC8260 and the MSC8101 DSPs. These HDI16 signals are fed into the FPGA on the MSC8101PFC card, and the FPGA is programmed to handle these signals and perform such operations as feeding MSC8101 with their HRCW from their host (MPC8260), for example. **Figure 9** shows the HDI16 path between the MPC8260 and the MSC8101PFC card. **Table 7** lists the PTMC P2 connector signals.

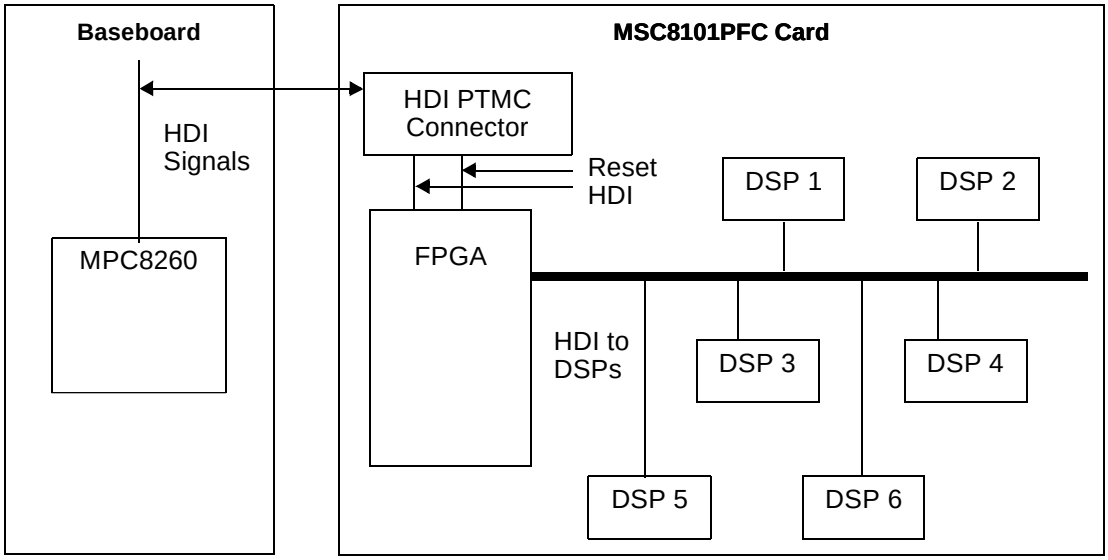


Figure 9. HDI16 Signals Path

Table 7. PTMC P2 Header

Pin	Signal	Pin	Signal
1	PMC_HRESET	2	PMC_TRST
3	PMC_TMS	4	PMC_TDO
5	PMC_TDI	6	GND
7	GND	8	PMC_TCK
9	PMC_HD0	10	PMC_HA1

Table 7. PTMC P2 Header (Continued)

Pin	Signal	Pin	Signal
11	PMC_HD1	12	V_{CC} (3.3 V)
13	DSP_RESET	14	PMC_HA2
15	V_{CC} (3.3 V)	16	PMC_HA3
17	PMC_HD2	18	GND
19	PMC_HD3	20	PMC_HRW
21	GND	22	PMC_HDS
23	PMC_HD4	24	V_{CC} (3.3 V)
25	PMC_HD5	26	PMC_HDREQ0
27	V_{CC} (3.3 V)	28	PMC_HDREQ1
29	PMC_HD6	30	GND
31	PMC_HD7	32	PMC_DSP_INT1
33	GND	34	PMC_HCS
35	PMC_HD8	36	V_{CC} (3.3 V)
37	GND	38	TP1 (Test Point 1)
39	PMC_HD9	40	GND
41	V_{CC} (3.3 V)	42	PMC_HOST_INT1
43	PMC_HD10	44	GND
45	PMC_HD11	46	PMC_HOST_INT2
47	GND	48	PMC_HA_DSP0
49	PMC_HD12	50	V_{CC} (3.3 V)
51	PMC_HD13	52	PMC_HA_DSP1
53	V_{CC} (3.3 V)	54	PMC_HA_DSP2
55	PMC_HD14	56	GND
57	PMC_HD15	58	PMC_DONE_1
59	GND	60	PMC_DONE_2
61	PMC_HA0	62	V_{CC} (3.3 V)
63	GND	64	PMC_BUS_CLK

All DSPs and the FPGA register are part of the PDK memory map. The MPC8260 (which resides on the PDK baseboard) can access these modules of the MSC8101PFC card using MPC8260 chip select 7. **Table 8** shows the HDI16 Base and Option Register settings, and **Table 9** shows the UPM programming.

Table 8. HDI16 Option and Base Registers

Registers	Values
BR7 (HDI16 Base Register)	0xF9001081
OR7 (HDI16 Option Register)	0xFFE00104

Table 9. HDI16 UPM Programming

Operations	Instructions
Single Read	MBMR = 0x90000000 MDR = 0x0FFFBC00 MDR = 0x0FFF7C00 MDR = 0x1FFFFC05
Single Write	MBMR = 0x90000018 MDR = 0xCFFFF000 MDR = 0x0FFF3000 MDR = 0x0FFF0000 MDR = 0x1FFFF005
Run	MBMR = 0x80000000

Note: You are not required to program the HDI16 since it is already programmed before it is shipped to customers.

3.7.2 TDM Signals

PTMC P3 carries TDM signals to DSP 3 and DSP 6. This PTMC connector is very important because it enables data streams to be processed in the MSC8101PFC card and then sent either to the outside world via the H.100 connector in the baseboard or to the PSTN card (if it is connected). The DSP TDM ports are bused as shown in **Table 10**.

Table 10. PTMC P3 Header

DSP	DSP TDMA	DSP TDMB
1	TDM1	TDM2
2	TDM1	TDM2
3	TDM1	TDM2
4	TDM2	TDM1
5	TDM2	TDM1
6	TDM2	TDM1

Refer to **Figure 10** for the TDM path between the baseboard and the MSC8101PFC card. **Table 11** lists the PTMC P3 signals.

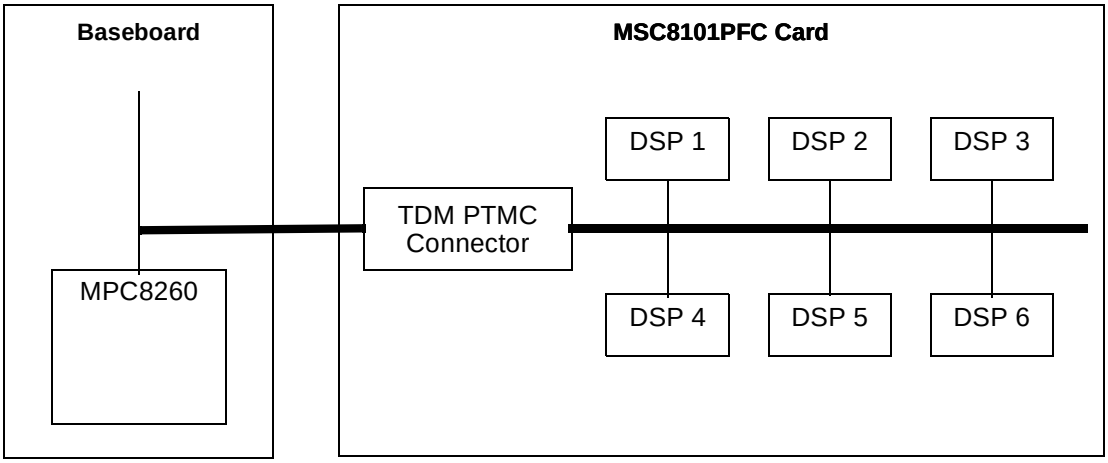


Figure 10. TDM Signal Path

Table 11. PTMC P3 Header

Pin	Signal	Pin	Signal
1	NC	2	GND
3	GND	4	NC
5	NC	6	NC
7	NC	8	GND
9	NC	10	NC
11	NC	12	NC
13	NC	14	GND
15	GND	16	NC
17	CT_FRAM_A	18	NC
19	NC	20	GND
21	NC	22	NC
23	NC	24	NC
25	CT_C8_A	26	GND
27	GND	28	NC
29	NC	30	NC
31	NC	32	GND
33	GND	34	NC
35	NC	36	NC
37	NC	38	GND
39	NC	40	NC
41	NC	42	NC

Table 11. PTMC P3 Header (Continued)

Pin	Signal	Pin	Signal
43	NC	44	GND
45	GND	46	NC
47	NC	48	NC
49	NC	50	NC
51	GND	52	NC
53	NC	54	NC
55	NC	56	GND
57	NC	58	NC
59	TDM1_TX_DATA	60	TDM1_RX_DATA
61	TDM0_TX_DATA	62	GND
63	GND	64	TDM0_RX_DATA

3.7.3 UTOPIA Signals

The PTMC P4 connector carries UTOPIA signals to all DSPs on the MSC8101PFC card. The PTMC P4 does not connect to the FPGA. **Table 12** lists the PTMC P4 connector signals. **Figure 11** shows the UTOPIA path between the MSC8101PFC card and baseboard.

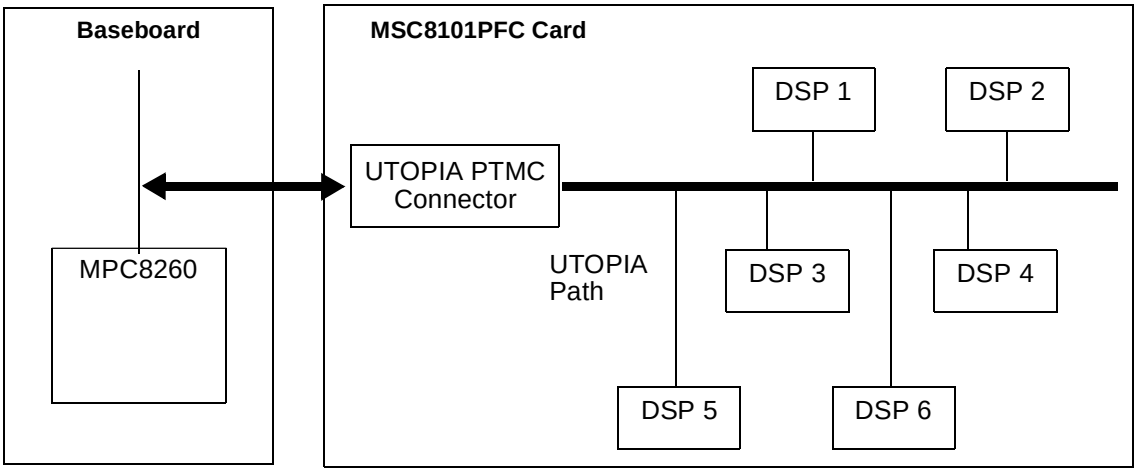


Figure 11. UTOPIA Path Between the Baseboard and MSC8101PFC Card

Table 12. PTMC P4 Header

Pin	Signal	Pin	Signal
1	UTP_TXSOC	2	GND
3	GND	4	UTP_RXADR4
5	UTP_TXCLAV	6	UTP_TXADR4

Table 12. PTMC P4 Header (Continued)

Pin	Signal	Pin	Signal
7	UTP_RXADR3	8	GND
9	NC	10	GND
11	GND	12	NC
13	NC	14	GND
15	GND	16	UTP_RXENB
17	UTP_TXADR3	18	UTP_RXCLAV
19	UTP_TXADR2	20	GND
21	NC	22	UTP_TXENB
23	GND	24	UTP_RXADR2
25	UTP_TXCLK	26	GND
27	GND	28	UTP_RXADR1
29	UTP_TXADR0	30	UTP_TXADR1
31	UTP_TXPRTY	32	GND
33	GND	34	UTP_RXADR0
35	UTP_TXD7	36	UTP_RXPRTY
37	UTP_RXD6	38	GND
39	NC	40	UTP_RXD7
41	GND	42	UTP_RXD6
43	UTP_RXCLK	44	GND
45	GND	46	UTP_RXD5
47	UTP_TXD5	48	UTP_RXD4
49	UTP_RXD4	50	GND
51	GND	52	UTP_RXD3
53	UTP_TXD3	54	UTP_RXD2
55	UTP_RXD2	56	GND
57	PQ2_I2C_SDA	58	UTP_RXD1
59	UTP_TXD1	60	UTP_RXD0
61	UTP_RXD0	62	GND
63	GND	64	UTP_RXSOC

3.7.4 Ethernet MII Signals

The PTMC P5 connector carries Ethernet Media-Independent Interface (MII) signals to DSP 1 and the FPGA on the MSC8101PFC card. DSP1 can use MII signals to receive and transmit Ethernet packets using the Ethernet PHY in the baseboard, for example. **Figure 12** shows the data path between the MSC8101PFC and the baseboard. **Table 13** lists the PTMC P5 connector signals.

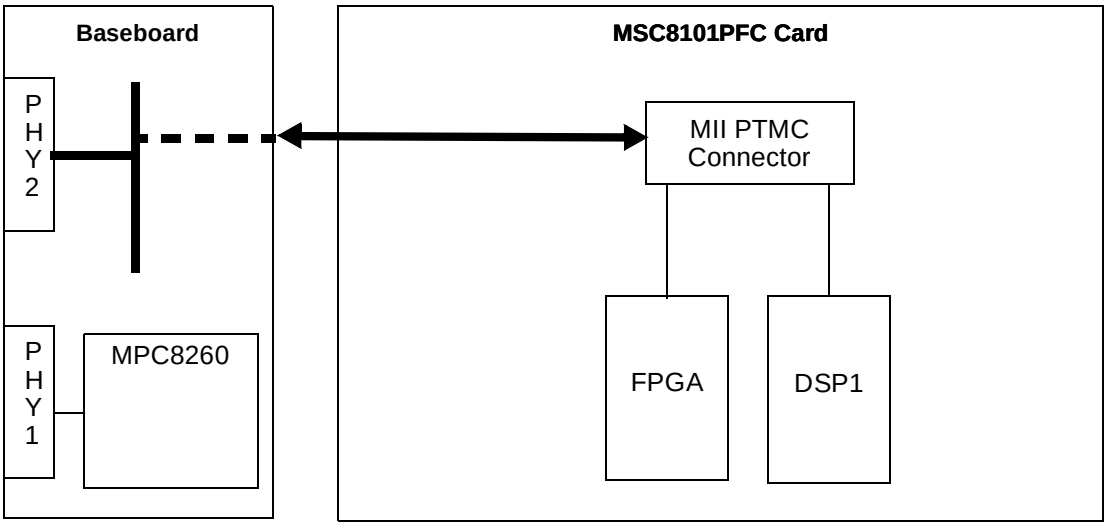


Figure 12. MII Path Between the MSC8101PFC Card PHY and the Baseboard

Table 13. PTMC P5 Header

Pin	Signal	Pin	Signal
1	NC	2	V_{CC} (1.6 V)
3	NC	4	NC
5	NC	6	NC
7	NC	8	NC
9	V_{CC} (1.6 V)	10	NC
11	V_{CC} (1.6 V)	12	GND
13	NC	14	NC
15	NC	16	NC
17	NC	18	NC
19	GND	20	FPG_TCLK
21	FPG_TXD0	22	V_{CC} (1.6 V)
23	FPG_TXD1	24	DSP_RXDV
25	FPG_TXD2	26	DSP_RXD0
27	FPG_TXD3	28	DSP_RXD1
29	V_{CC} (1.6 V)	30	DSP_RXD2

Table 13. PTMC P5 Header (Continued)

Pin	Signal	Pin	Signal
31	V_{CC} (1.6 V)	32	GND
33	FPG_TXEN	34	DSP_RXD3
35	FPG_TXER	36	DSP_RXER
37	FPG_COL	38	DSP_CRS
39	GND	40	DSP_RCLK
41	DSP_TXD0	42	V_{CC} (1.6 V)
43	DSP_TXD1	44	DSP_RXDV
45	DSP_TXD2	46	DSP_RXD0
47	DSP_TXD3	48	DSP_RXD1
49	V_{CC} (1.6 V)	50	DSP_RXD2
51	V_{CC} (1.6 V)	52	GND
53	DSP_TXEN	54	DSP_RXD3
55	DSP_TXER	56	DSP_RXER
57	DSP_COL	58	DSP_CRS
59	GND	60	DSP_RCLK
61	V_{CC} (1.6 V)	62	GND
63	V_{CC} (1.6 V)	64	DSP_TCLK

3.7.5 FPGA Signals

The PTMC P1 connector carries FPGA signals between the baseboard and the MSC8101PFC card. **Table 14** lists the PTMC P1 signals.

Table 14. PTMC P1 Header

Pin	Signal	Pin	Signal
1	V_{CC} (2.5 V)	2	FPGA_CCLK
3	GND	4	FPGA_DONE
5	V_{CC} (2.5 V)	6	FPGA_DIN
7	V_{CC} (2.5 V)	8	V_{CC} (5.0 V)
9	V_{CC} (2.5 V)	10	FPGA_PROGRAM
11	GND	12	V_{CC} (2.5 V)
13	NC	14	GND
15	GND	16	NC
17	V_{CC} (2.5 V)	18	V_{CC} (5.0 V)
19	V_{CC} (3.3 V)	20	V_{CC} (2.5 V)

Table 14. PTMC P1 Header (Continued)

Pin	Signal	Pin	Signal
21	V_{CC} (2.5 V)	22	NC
23	NC	24	GND
25	GND	26	NC
27	NC	28	NC
29	NC	30	V_{CC} (5.0 V)
31	NC	32	NC
33	NC	34	GND
35	GND	36	NC
37	NC	38	V_{CC} (5.0 V)
39	GND	40	NC
41	NC	42	NC
43	NC	44	GND
45	V_{CC} (3.3 V)	46	NC
47	NC	48	NC
49	NC	50	V_{CC} (5.0 V)
51	GND	52	NC
53	NC	54	NC
55	NC	56	GND
57	V_{CC} (3.3 V)	58	NC
59	NC	60	NC
61	NC	62	V_{CC} (5.0 V)
63	GND	64	NC

4 MSC8101PFC LEDs

Table 15 lists all the LEDs in MSC8101PFC card.

Table 15. LEDs in the MSC8101PFC Card

LED	DSP	Description
DSP1_LED1	DSP 1	LED illuminate green
DSP1_LED2		LED illuminate red
DSP2_LED	DSP2	LED illuminate green
DSP3_LED	DSP3	LED illuminate green
DSP4_LED	DSP4	LED illuminate green
DSP5_LED	DSP5	LED illuminate green

Table 15. LEDs in the MSC8101PFC Card (Continued)

LED	DSP	Description
DSP6_LED	DSP6	LED illuminate green
CPLD_LED	CPLD	LED illuminate green

5 Software Instructions

This section covers both the firmware implementation and the MSC8101 Hardware Reset Configuration Word (HRCW).

5.1 Firmware Implementation

The memory map of the MSC8101PFC card is re-programmable as desired. Since it is a soft map, device address can be moved about the map, as convenient. **Table 16** lists the details of the memory map.

Table 16. MSC8101 Memory Map

Address Range	Device Name	Port Size
These addresses can be accessed through the SC140 core.		
00000000–0007FFFF	Internal SRAM	64
00080000–00EFFDFF	Empty Space	
00EFFE00–00EFFEFF	EOnCE Registers	16
00EFFF00–00EFFFFF	Empty Space	
00F00000–00F0FFFF	SP Peripherals (QBus Bank 0)	64
00F10000–00F7FFFF	Empty Space	
00F80000–00F807FF	Boot ROM (QBus Bank 1)	64
00F80800–01EFFFF	Empty Space	
01F00000–01F0FFFF	DSP Peripherals (CS11)	64
01F10000–01FFFFFF	Empty Space	
02000000–0207FFFF	Internal SRAM (CS10)	64
02080000–146FFFFF	Empty Space	
These addresses can be accessed through the memory map.		
F9000000–F913FFFF	MSC8101 System Bus Memory and CPM5	32
F9140000–1FFFFFFF	Empty Space	
20000000–207FFFFF	SDRAM	32
20800000–FFFFFFFF		

5.2 MSC8101 HRCW

After reset, the MSC8101 processor must fetch its Hardware Reset Configuration Word (HRCW) to configure its bus, clocks, and so on. All MSC8101 devices fetch their Hard Reset Configuration Word (HRCW) from the host MPC8260. All MSC8101 devices on the MSC8101PFC card have the same HRCW. The HRCW value for MSC8101 rev A.2 silicon is 0x2580023E.

5.3 System Memory Map

The system memory map, shown in **Table 17**, is determined by the FPGA, which the baseboard programs when it initializes the card. This system memory map is based on the default jumper settings of the MSC8101PFC and baseboard. For details, see the *Packet Telephony Development Kit Software User's Guide* (PTKITSOFTUG/D).

Table 17. System Memory Map Based on Default Jumper Settings

Register	Offset	Description
DSP1	**0x00000**	**First Digital Signal Processor**
ICR	0x00000	HDI16 Interface Control Register
CVR	0x00002	HDI16 Command Vector Register
ISR	0x00004	HDI16 Interface Status Register
TX/RX[0–3]	0x02000	HDI16 Transmit/Receive Data Registers
RSCFG[0–3]	0x04000	HDI16 Reset Configuration Registers
DSP2	**0x08000**	**Second Digital Signal Processor**
ICR	0x08000	HDI16 Interface Control Register
CVR	0x08002	HDI16 Command Vector Register
ISR	0x08004	HDI16 Interface Status Register
RX/TX[0–3]	0x0A000	HDI16 Transmit/Receive Data Registers
RSCFG[0–3]	0x0C000	HDI16 Reset Configuration Registers
DSP3	**0x10000**	**Third Digital Signal Processor**
ICR	0x10000	HDI16 Interface Control Register
CVR	0x10002	HDI16 Command Vector Register
ISR	0x10004	HDI16 Interface Status Register
RX/TX[0–3]	0x12000	HDI16 Transmit/Receive Data Registers
RSCFG[0–3]	0x14000	HDI16 Reset Configuration Registers
DSP4	**0x18000**	**Fourth Digital Signal Processor**
ICR	0x18000	HDI16 Interface Control Register
CVR	0x18002	HDI16 Command Vector Register
ISR	0x18004	HDI16 Interface Status Register
RX/TX[0–3]	0x1A000	HDI16 Transmit/Receive Data Registers
RSCFG[0–3]	0x1C000	HDI16 Reset Configuration Registers
DSP5	**0x20000**	**Fifth Digital Signal Processor**
ICR	0x20000	HDI16 Interface Control Register
CVR	0x20002	HDI16 Command Vector Register
ISR	0x20004	HDI16 Interface Status Register
RX/TX[0–3]	0x22000	HDI16 Transmit/Receive Data Registers
RSCFG[0–3]	0x24000	HDI16 Reset Configuration Registers
DSP6	**0x28000**	**Sixth Digital Signal Processor**
ICR	0x28000	HDI16 Interface Control Register
CVR	0x28002	HDI16 Command Vector Register
ISR	0x28004	HDI16 Interface Status Register
RX/TX[0–3]	0x2A000	HDI16 Transmit/Receive Data Registers
RSCFG[0–3]	0x2C000	HDI16 Reset Configuration Registers

Table 17. System Memory Map Based on Default Jumper Settings (Continued)

Register	Offset	Description
DSP_DMA	**0x30000**	**Mapped DSP Configured for DMA**
ICR	0x30000	HDI16 Interface Control Register
CVR	0x30002	HDI16 Command Vector Register
ISR	0x30004	HDI16 Interface Status Register
RX/TX[0–3]	0x32000	HDI16 Transmit/Receive Data Registers
RSCFG[0–3]	0x34000	HDI16 Reset Configuration Registers
FPGA REGS	**0x38000**	**FPGA Control and Status Registers**
FPGA GCR	0x38000	FPGA General Control Register
FPGA RCR	0x38002	FPGA Reset Control Register
FPGA ICSR	0x38004	FPGA Interrupt Control and Status Register
FPGA IMR	0x38006	FPGA Interrupt Mask Register
FPGA RQSR	0x3A000	FPGA Request Status Register
FPGA TDAR	0x3A002	FPGA Transmit DMA Address Register
FPGA RDAR	0x3A004	FPGA Receive DMA Address Register
Unused	0x3A006	Unused address available in FPGA registers

5.4 FPGA Registers

The FPGA registers control FPGA functionality and signal routing. The unused bits control nothing, and attempts to write to the unused bits are ignored. It is good programming practice to avoid setting unused bits because future versions may apply meaning. Also, writes to read-only bits are ignored.

When the FPGA is first configured or reset, all register bits are cleared, except for the RCR, where every bit is set, and the GCR[MCK] field. Also, the bits that report status continue to report the values provided by the DSP farm.

GCR General Control Register

Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	DHE	GDE	LED	DFE	MCK1	MCK2	MCK3	DDS	—	—	DHM6	DHM5	DHM4	DHM3	DHM2	DHM1
TYPE	R/W															
RESET	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0

GCR controls the FPGA DMA hunt functionality and other special features.

Table 18. GCR Bit Descriptions

Name	Reset	Description
DHE 0	0	**DMA Hunt Enable** Enables the DMA hunt machine that performs round-robin polling of the individual HRRQ signals seeking a DSP that is ready to transfer data to the host. Set this bit to enable DMA hunt. When a DSP is selected, the HRRQ signal is routed to the host receive DREQ, the DONE signal is connected, and the DSP HDI16 registers are mapped into the DSP_DMA address space for read cycles. The DMA hunt state machine then snoops the DONE signal from the DSP to determine whether the DMA access is complete. When the data transfer completes, the DMA hunt state machine writes the address of the DSP into the RDAR before returning to the polling process.
GDE 1	0	**GPIO DREQ Enable** Older versions of firmware for the MSC8101PFC override HTRQ and HRRQ using general-purpose I/O. Setting GDE supports this override. When this bit is set, GPIO0 and GPIO1 are OR-ed with HTRQ and HRRQ, respectively, for all DSP devices. Also, GPIO2, which is normally used as DONE, is rerouted to the ICSR[IFD] field, replacing GPIO0. DONE is continuously deasserted, regardless of the DMA hunt enable status.
LED 2	0	**FPGA LED On/Off** Turns on the green light emitting diode (LED) next to the FPGA. When this bit is cleared, the light is off.
DFE 3	0	**DREQ Flip Enable** After the FPGA is configured or reset, DREQ1 is used for transmit and DREQ2 is used for receive. When this bit is set, the host transmit and receive DREQ input signals are reversed.
MCK[1–3] 4–6	1	DSP MODCK Value Sets the MODCK value for the DSP farm. This value controls the DSP clocking mode and is set to 0b001 after the FPGA is configured or reset.
DDS 7	0	DSP Dual Strobe Sets the bus strobe mode to the DSP farm. The host always uses single-strobe bus mode, but the FPGA converts the single-strobe bus mode to dual-strobe bus mode if this bit is set. When DDS is cleared, the bus strobe signals pass through the FPGA without conversion.
DHM[1–6] 10–15	0	DMA Hunt Mask When DMA hunt is enabled, individual DSP devices can be excluded from the polling process by clearing the bit for the DSP.

RCR Reset Control Register

Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	—										RST6	RST5	RST4	RST3	RST2	RST1
TYPE													R/W			
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

RCR controls the $\overline{\text{HRESET}}$ input to each DSP. When a bit is cleared in this register, the corresponding DSP is put into $\overline{\text{HRESET}}$. Setting a bit releases the $\overline{\text{HRESET}}$ for the DSP device unless the $\overline{\text{LOCAL\_HRESET}}$ input to the FPGA is asserted, in which case all DSP devices are placed into $\overline{\text{HRESET}}$. Reading from this register provides the $\overline{\text{HRESET}}$ status of each DSP. A cleared bit means that the corresponding DSP is in $\overline{\text{HRESET}}$.

ICSR Interrupt Control and Status Register

Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	—	—	IFD6	IFD5	IFD4	IFD3	IFD2	IFD1	—	—	ITD6	ITD5	ITD4	ITD3	ITD2	ITD1
TYPE	R										R/W					
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ICSR reports the interrupt status from the DSP devices and can control interrupt commands to individual DSP devices.

Table 19. ICSR Bit Descriptions

Name	Reset	Description
IFD[1–6] 2–7	0	**Interrupt From DSP** Shows the interrupt status from each DSP device. Normally, GPIO0 from each DSP device signals interrupts to the host. When the GCR[GDE] is set, GPIO2 signals interrupts from the DSP farm. A global interrupt is issued to the host if any bits of the IFD field are set. The global interrupt to the host is assigned to PMC host INT1. These interrupts can be masked by the Interrupt Mask Register (IMR).
ITD[1–6] 10–15	0	**Interrupt to DSP** Controls interrupts to each DSP device. When a bit in this field is set, an interrupt is issued to the corresponding DSP device, unless the interrupt is masked. The software must set and clear the bits in this field. The interrupts are mapped to DSP $\overline{\text{IRQ1}}$.

IMR Interrupt Mask Register

Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	—	—	MFD6	MFD5	MFD4	MFD3	MFD2	MFD1	—	—	MTD6	MTD5	MTD4	MTD3	MTD2	MTD1
TYPE	R										R/W					
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

IMR masks interrupts to and from the DSP farm.

Table 20. IMR Bit Descriptions

Name	Reset	Description
MFD[1–6] 2–7	0	**Mask From DSP** Individual interrupts from each DSP device can by masked by clearing bits in this register. Setting a bit unmasks (enables) interrupts from the DSP device.
MTD[1–6] 10–15	0	**Mask to DSP** Individual interrupts to each DSP device can be masked by clearing bits in this register. Setting a bit unmasks (enables) interrupts to the DSP device issued via the ICSR.

RQSR Request Status Register

Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	—	—	TRS6	TRS5	TRS4	TRS3	TRS2	TRS1	—	—	RRS6	RRS5	RRS4	RRS3	RRS2	RRS1
TYPE								R								
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RQSR shows the status of the HDI16 buffer status signals HTRQ and HRRQ for each DSP device.

Table 21. RQSR Bit Descriptions

Name	Reset	Description
TRS[1–6] 2–7	0	**Transmit Request (HTRQ) Status** Contains the value of the HTRQ signal from each DSP device.
RRS[1–6] 10–15	0	**Mask to DSP** Contains the value of the HRRQ signal from each DSP device.

TDAR Transmit DMA Address Register

Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	—	—	—	—	—	—	—	—	—	—	—	—	—	TDA2	TDA1	TDA0
TYPE														R/W		
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TDAR manually selects the DSP that is mapped into the DSP_DMA address space for the write direction. For example, if this register is cleared, all write bus cycles to the DSP_DMA address space are performed on DSP1. Setting all the bits addresses DSP8, which does not exist on the MSC8101PFC. Therefore, the write cycles to the DSP_DMA have no effect.

RDAR Receive DMA Address Register

Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	—	—	—	—	—	—	—	—	—	—	—	—	—	RDA2	RDA1	RDA0
TYPE	R/W when DMA hunt is disabled. R-only when DMA hunt is enabled.															
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RDAR serves two purposes. When DMA hunt is disabled, it manually selects which DSP is mapped into the DSP_DMA address space for the read direction. For example, if this register is cleared, all read bus cycles to the DSP_DMA address space are performed on DSP1. Setting all the bits addresses DSP8, which does not exist on the MSC8101PFC. Therefore, the read cycles from the DSP_DMA address space return unknown results. When DMA hunt is enabled, this register is updated at the completion of each DMA transfer that is from a DSP device to the host. The register is updated with the address of the DSP from the just completed transfer. When DMA hunt is enabled, the host is denied write permissions to this register. When DMA hunt is disabled, this register returns to the last value written into it.

Appendix A Schematics

The following pages show the schematics of the MSC8101PFC.

Packet Telephony Development Kit
MSC8101 Packet Telephony Farm Card
Version 1.94

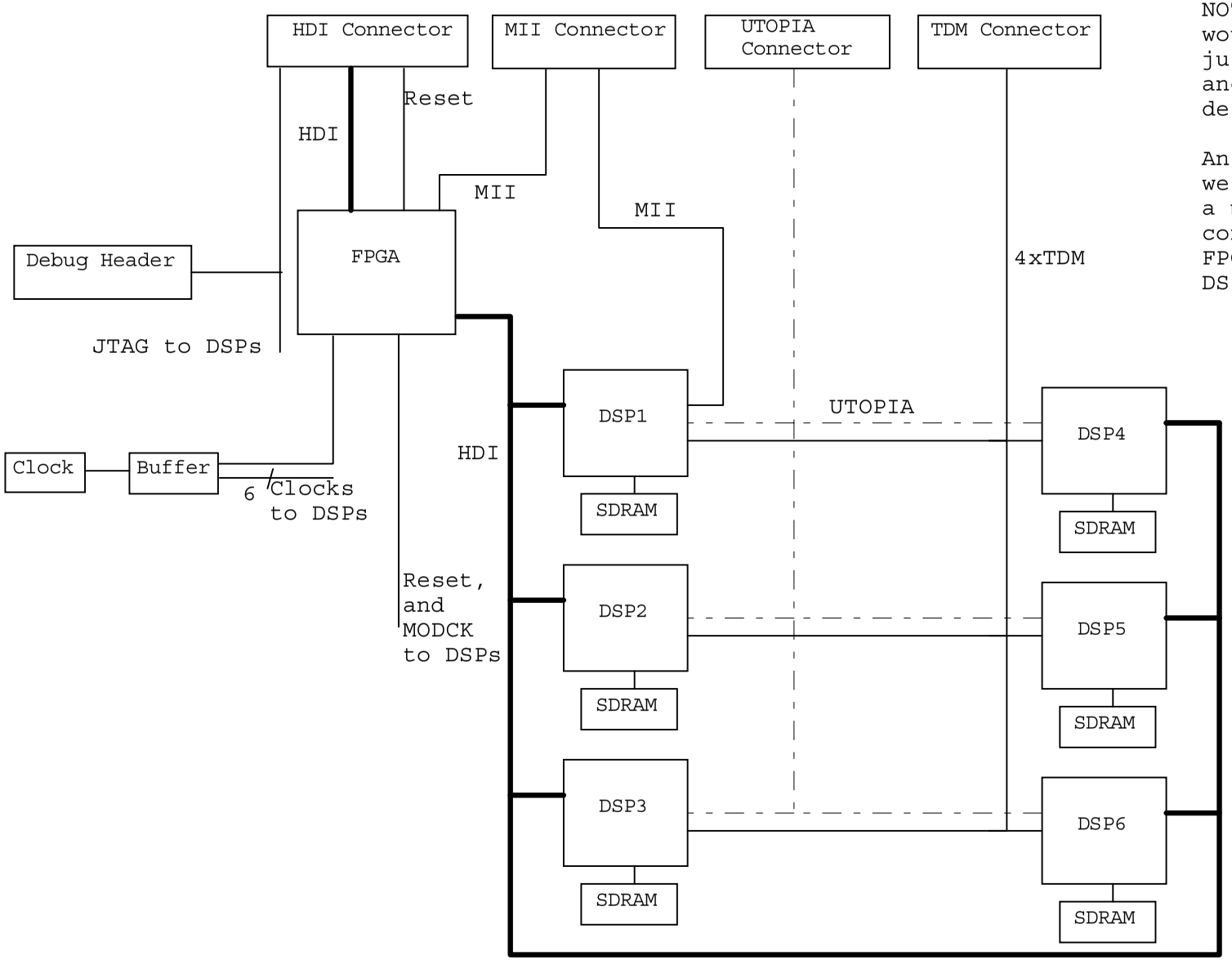
	Table of Contents
Page	Description
1	This Page
2	Block Diagram
3	DSP1 Hierarchical Block
4	DSP2 to DSP6 Hierarchical Blocks
5	FPGA, JTAG, Clocks
6	PMC Connectors
7	DSP Pull-ups
8	TDM Buffer
9	DSP BLOCK: DSP Core
10	DSP BLOCK: DSP CPM
11	DSP BLOCK: DSP Power
12	DSP BLOCK: DSP SDRAM
13+	The DSP block pages repeat for each DSP block.

Revision History	
1.94	Initial Prototypes

Packet telelphony Motorola Copyright 2002 Motorola Confidential Proprietary	Title	TWO DSP SIMM	Block Cover Page
	Name	Rich Cutler	Rev 1.94
	Date:	Friday, April 25, 2003	Sheet 1 of 31

Guide to Schematics

DSP_CARD



NOTE: A minimal system would not require an FPGA, just a CPLD for buffering and address/chip select decoding.

An FPGA was chosen here so we can do experiments with a more sophisticated DMA control or even putting a FPGA MAC directly on the DSP card.

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	Name Rich Cutler		Rev 1.94
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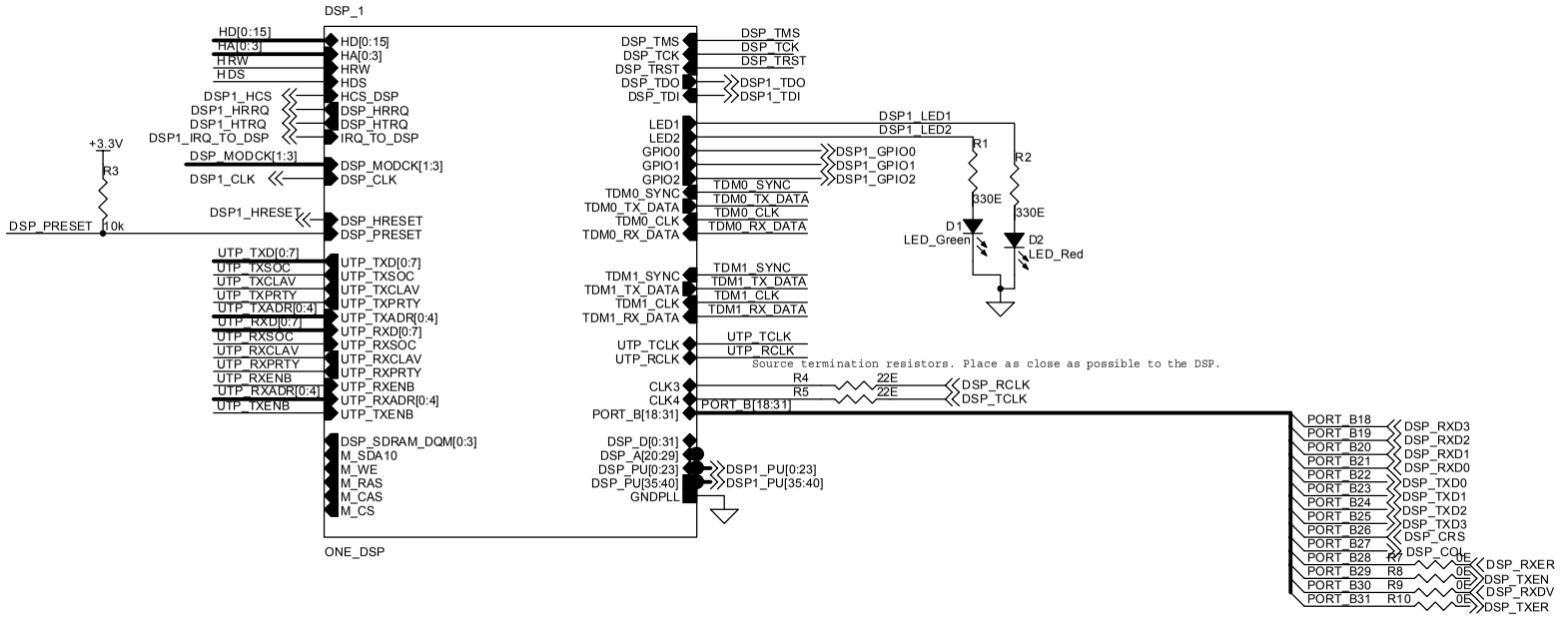


Host Bus

HD[0:15]
HA[0:3]
HRW
HDS

JTAG

DSP_TMS
DSP_TCK
DSP_TRST

TDM0 Bus

TDM0_SYNC
TDM0_TX_DATA
TDM0_CLK
TDM0_RX_DATA

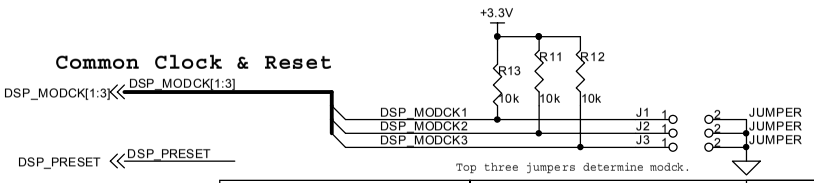
TDM1 Bus

TDM1_CLK
TDM1_TX_DATA
TDM1_SYNC
TDM1_RX_DATA

UTOPIA

UTP_TXCLK
UTP_RXCLK
UTP_TXD[0:7]
UTP_TXSOC
UTP_TXCLAV
UTP_TXPRTY
UTP_TXADR[0:4]
UTP_RXD[0:7]
UTP_RXSOC
UTP_RXCLAV
UTP_RXPRTY
UTP_RXENB
UTP_RXADR[0:4]
UTP_TXENB
UTP_TCLK
UTP_RCLK

Common Clock & Reset



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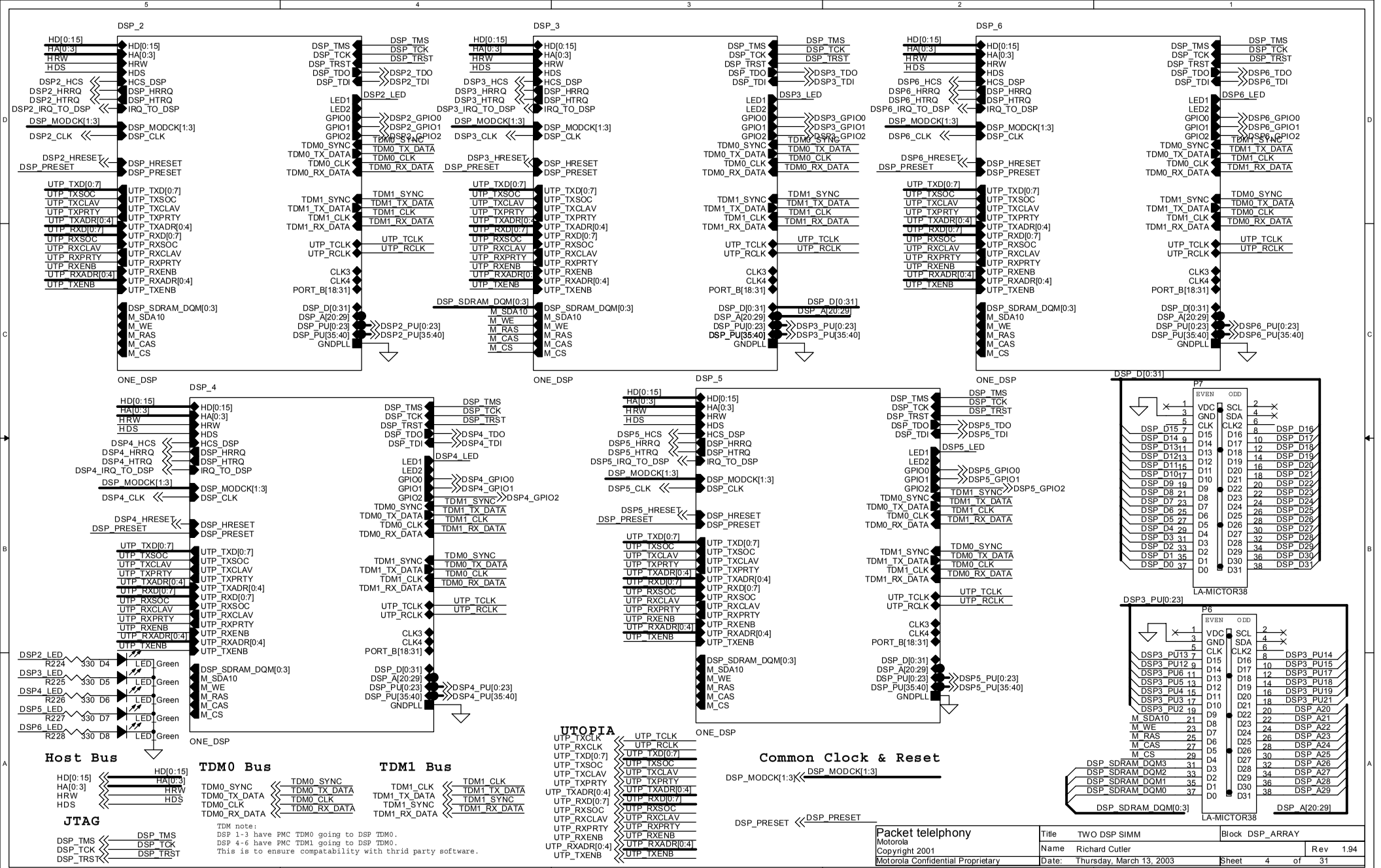
DSP_2
DSP_3
DSP_6
DSP_4
DSP_5
ONE_DSP
Host Bus
TDM0 Bus
TDM1 Bus
JTAG
UTOPIA
Common Clock & Reset
TDM note:
DSP 1-3 have PMC TDM0 going to DSP TDM0.
DSP 4-6 have PMC TDM1 going to DSP TDM0.
This is to ensure compatability with thrid party software.
P7
P6
LA-MICTOR38
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Block DSP_ARRAY
Name Richard Cutler
Rev 1.94
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Sheet 4 of 31

The FPGA is used to control reset, configure the scan chain, buffer the host interface, and implement the logic needed to select between DSPs.

Do not populate R229, R230, R232, R234, R236. These are to be used for unified scan chanin on baseboard only.

Place .01uF & 0.1uF caps within 1cm of FPGA.

Place cap close to osc

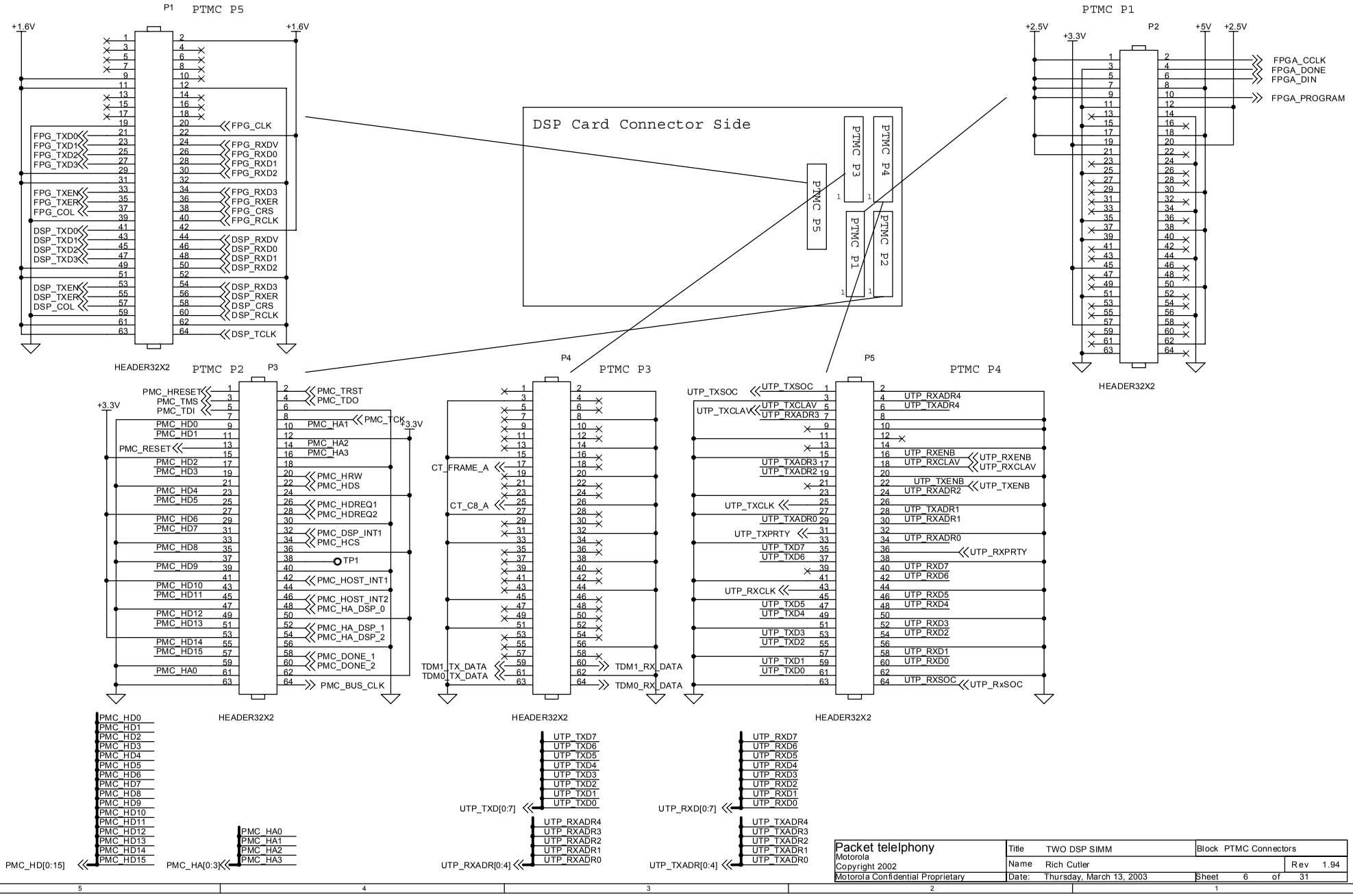
Place power caps close to 2510C

Pinout is optomized for ease of board layout. Assumed layout:

DSP Card Connector side. (FPGA is on the other side).

If layout assumption changes, please contact the Rich to change the FPGA pinout

Packet telelphony Motorola Copyright 2001 Motorola Confidential Proprietary	Title	DSP FARMCARD	Block CPLD
	Name	Rich Cutler	Rev 1.94
	Date:	Friday, April 25, 2003	Sheet 5 of 31


PTMC P5
P1
+1.6V
+1.6V
FPG_CLK
FPG_TXD0
FPG_TXD1
FPG_TXD2
FPG_TXD3
FPG_RXDV
FPG_RXD0
FPG_RXD1
FPG_RXD2
FPG_TXEN
FPG_TXER
FPG_COL
FPG_RXD3
FPG_RXER
FPG_CRS
FPG_RCLK
DSP_TXD0
DSP_TXD1
DSP_TXD2
DSP_TXD3
DSP_RXDV
DSP_RXD0
DSP_RXD1
DSP_RXD2
DSP_TXEN
DSP_TXER
DSP_COL
DSP_RXD3
DSP_RXER
DSP_CRS
DSP_RCLK
DSP_TCLK
HEADER32X2
DSP Card Connector Side
PTMC P5
PTMC P3
PTMC P4
PTMC P1
PTMC P2
PTMC P1
P2
+2.5V
+3.3V
+5V
+2.5V
FPGA_CCLK
FPGA_DONE
FPGA_DIN
FPGA_PROGRAM
HEADER32X2
PTMC P2
P3
+3.3V
PMC_HRESET
PMC_TMS
PMC_TDI
PMC_TRST
PMC_TDO
PMC_TCK
+3.3V
PMC_HA1
PMC_HA2
PMC_HA3
PMC_RESET
PMC_HD0
PMC_HD1
PMC_HD2
PMC_HD3
PMC_HD4
PMC_HD5
PMC_HD6
PMC_HD7
PMC_HD8
PMC_HD9
PMC_HD10
PMC_HD11
PMC_HD12
PMC_HD13
PMC_HD14
PMC_HD15
PMC_HA0
PMC_HRW
PMC_HDS
PMC_HDREQ1
PMC_HDREQ2
PMC_DSP_INT1
PMC_HCS
TP1
PMC_HOST_INT1
PMC_HOST_INT2
PMC_HA_DSP_0
PMC_HA_DSP_1
PMC_HA_DSP_2
PMC_DONE_1
PMC_DONE_2
PMC_BUS_CLK
HEADER32X2
P4
PTMC P3
CT_FRAME_A
CT_C8_A
TDM1_TX_DATA
TDM0_TX_DATA
TDM1_RX_DATA
TDM0_RX_DATA
HEADER32X2
P5
PTMC P4
UTP_TXSOC
UTP_TXCLAV
UTP_RXADR3
UTP_TXADR3
UTP_TXADR2
UTP_TXADR0
UTP_TXPRTY
UTP_TXD7
UTP_TXD6
UTP_TXD5
UTP_TXD4
UTP_TXD3
UTP_TXD2
UTP_TXD1
UTP_TXD0
UTP_RXCLK
UTP_TXCLK
UTP_RXADR4
UTP_TXADR4
UTP_RXENB
UTP_RXCLAV
UTP_TXENB
UTP_RXADR2
UTP_TXADR1
UTP_RXADR1
UTP_RXADR0
UTP_RXPRTY
UTP_RXD7
UTP_RXD6
UTP_RXD5
UTP_RXD4
UTP_RXD3
UTP_RXD2
UTP_RXD1
UTP_RXD0
UTP_RXSOC
UTP_RxSOC
HEADER32X2
PMC_HD[0:15]
PMC_HA[0:3]
UTP_TXD[0:7]
UTP_RXADR[0:4]
UTP_RXD[0:7]
UTP_TXADR[0:4]
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Title TWO DSP SIMM
Block PTMC Connectors
Name Rich Cutler
Rev 1.94
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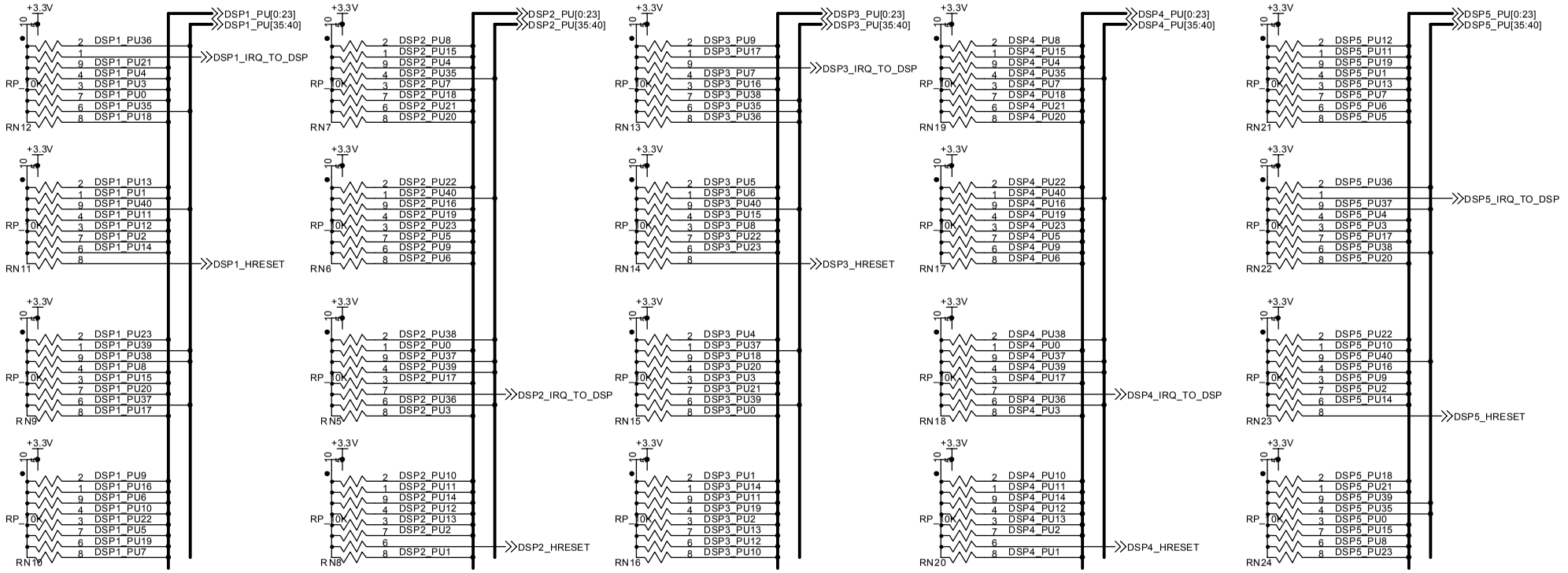
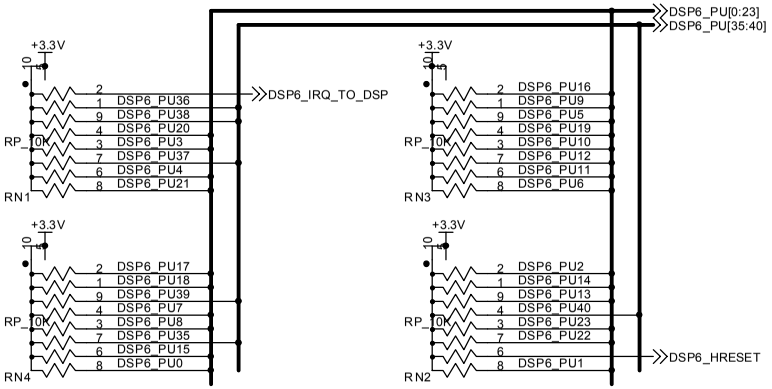
Sheet 6 of 31

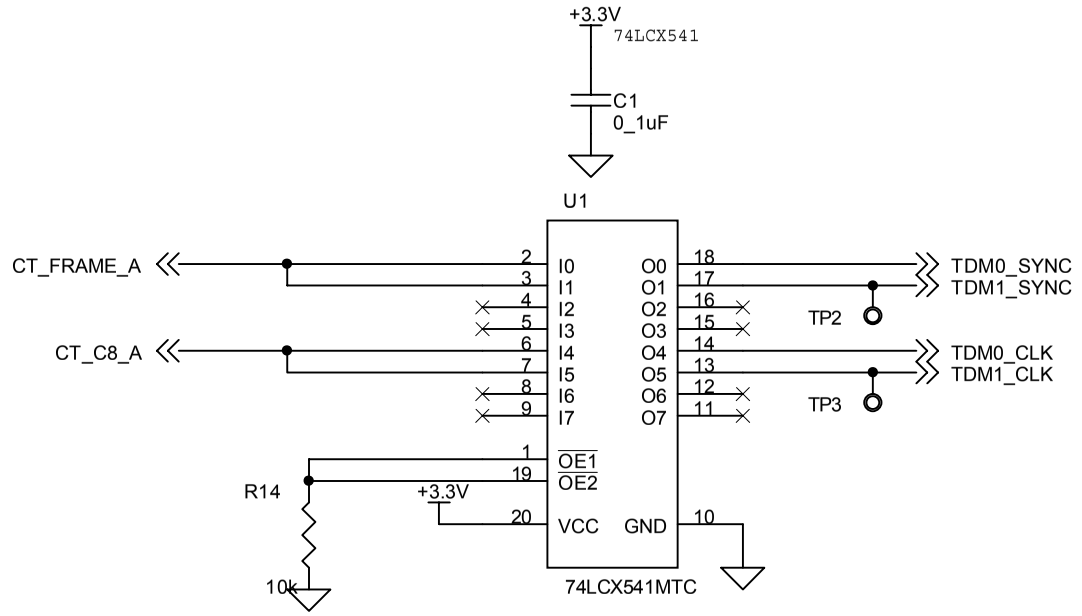


DSP1 DSP2 DSP3 DSP4 DSP5

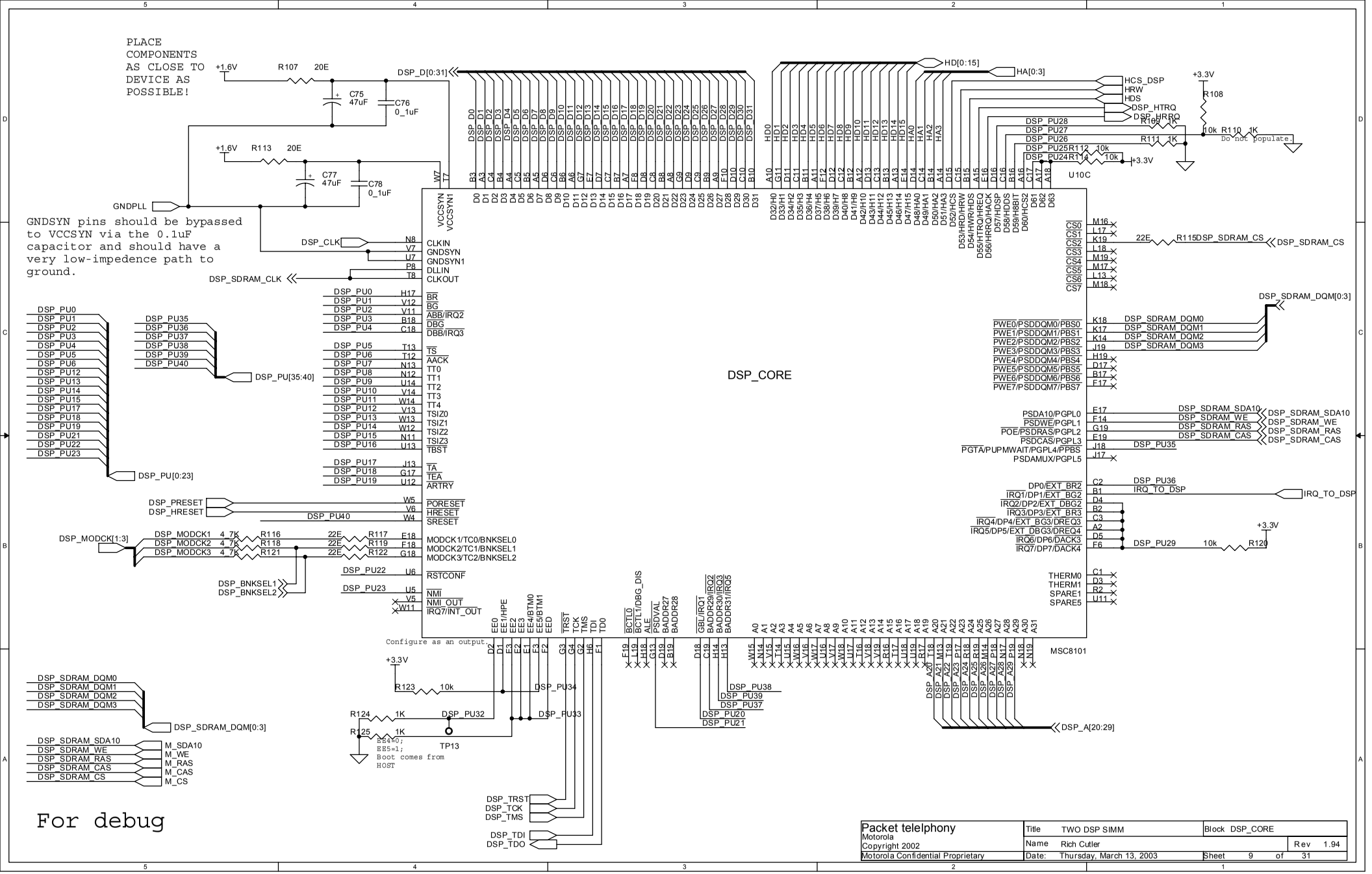


DSP6

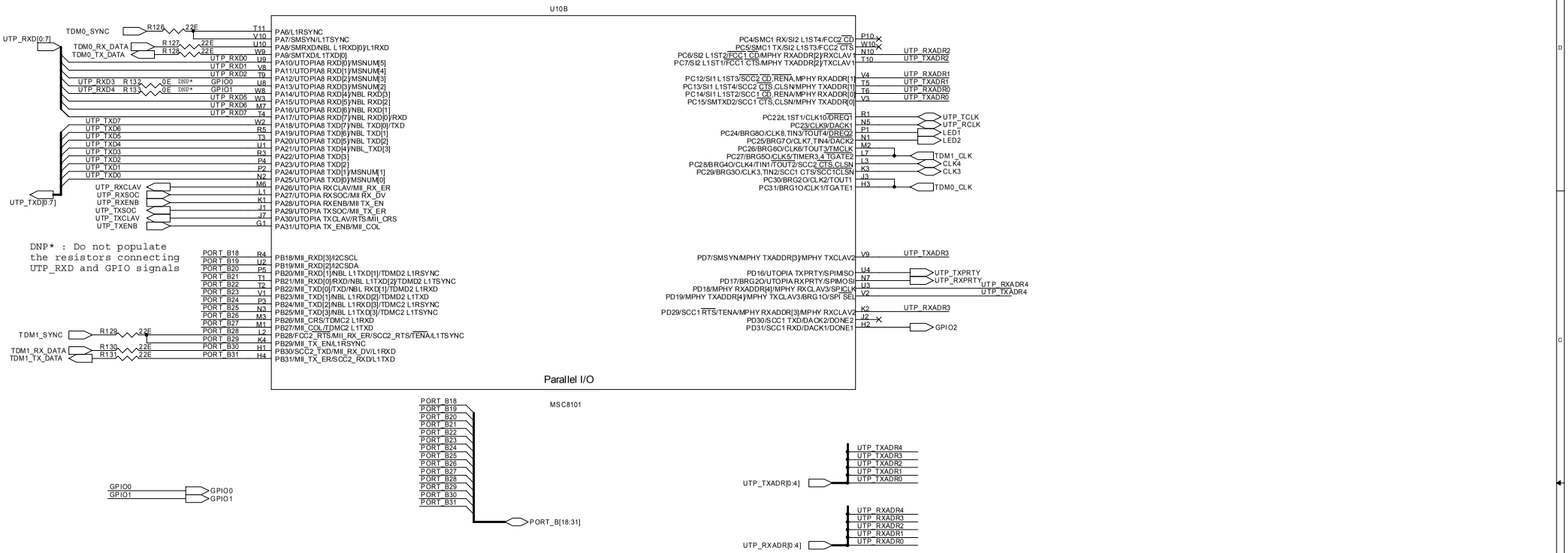
Packet telelphony	Title TWO_DSP_SIMM	Block PULL_UPS	
Motorola	Name Richard Cutler		Rev 1.94
Copyright 2001 Motorola Confidential Proprietary	Date: Thursday, March 13, 2003	Sheet 7 of 10	



Title	Farmcard		
Size A	Document Number <Doc>		Rev 1.94
Date: Thursday, March 13, 2003		Sheet 8 of 31	


PLACE COMPONENTS AS CLOSE TO DEVICE AS POSSIBLE!
GNDSYN pins should be bypassed to VCCSYN via the 0.1uF capacitor and should have a very low-impedence path to ground.
DSP_CORE
MSC8101
U10C
Configure as an output.
EE0=0; EE5=1; Boot comes from HOST
For debug
Packet telelphony
Motorola
Copyright 2002
Motorola Confidential Proprietary
Title TWO DSP SIMM
Block DSP_CORE
Name Rich Cutler
Rev 1.94
Date: Thursday, March 13, 2003
Sheet 9 of 31

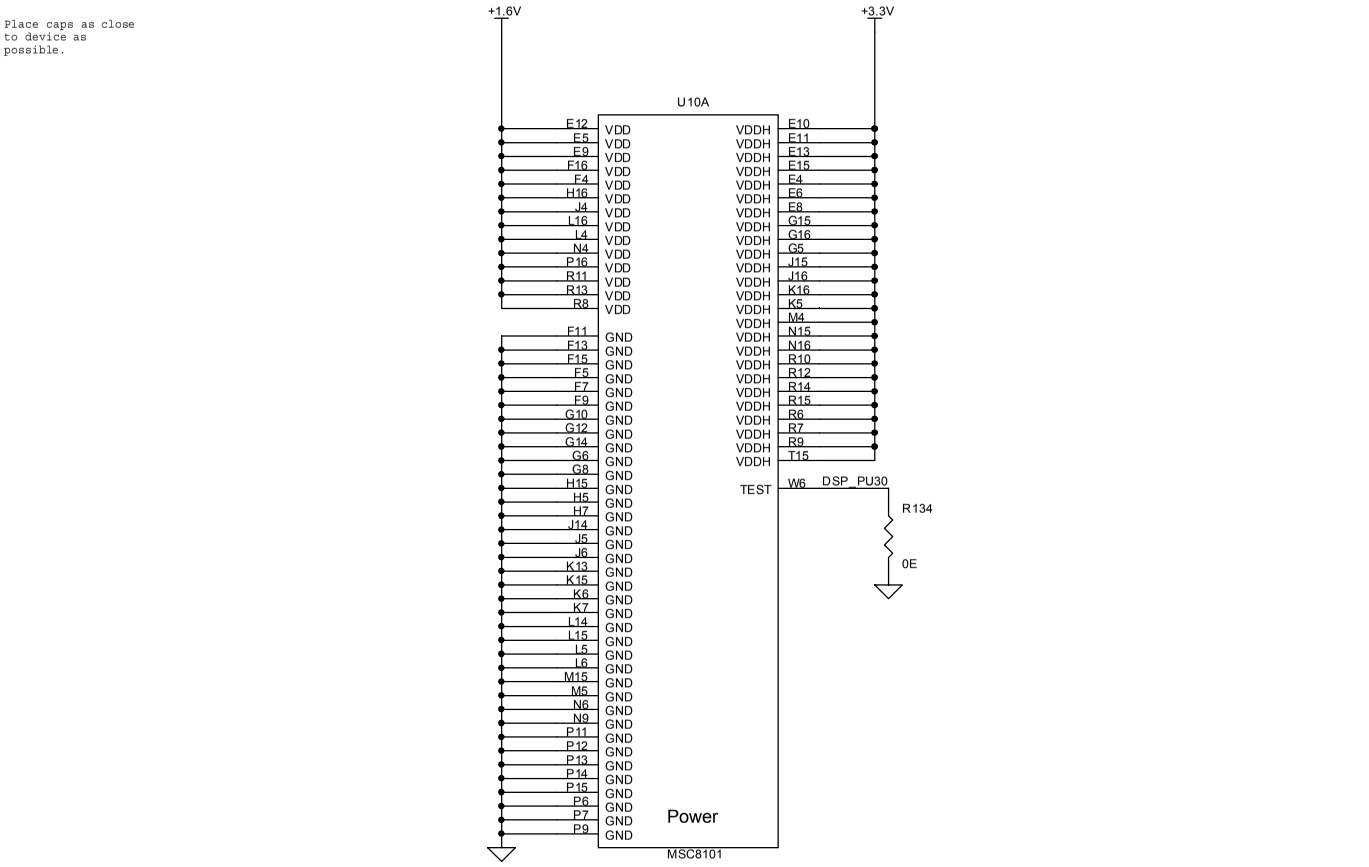
QUARTZ_1A CPM

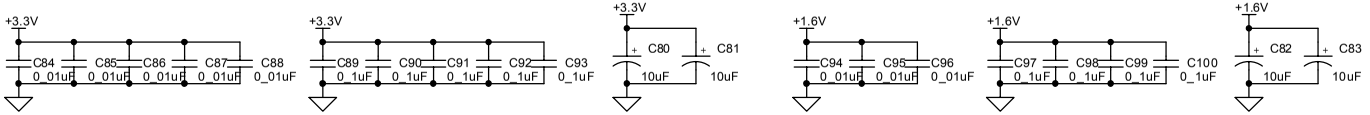


Packet telelphony Motorola Copyright 2002 Motorola Confidential Proprietary	Title: TWO DSP SIMM	Block: DSP_CPM	
	Name: Rich Cutler		Rev: 1.94
	Date: Thursday, March 13, 2003	Sheet: 10 of 31	

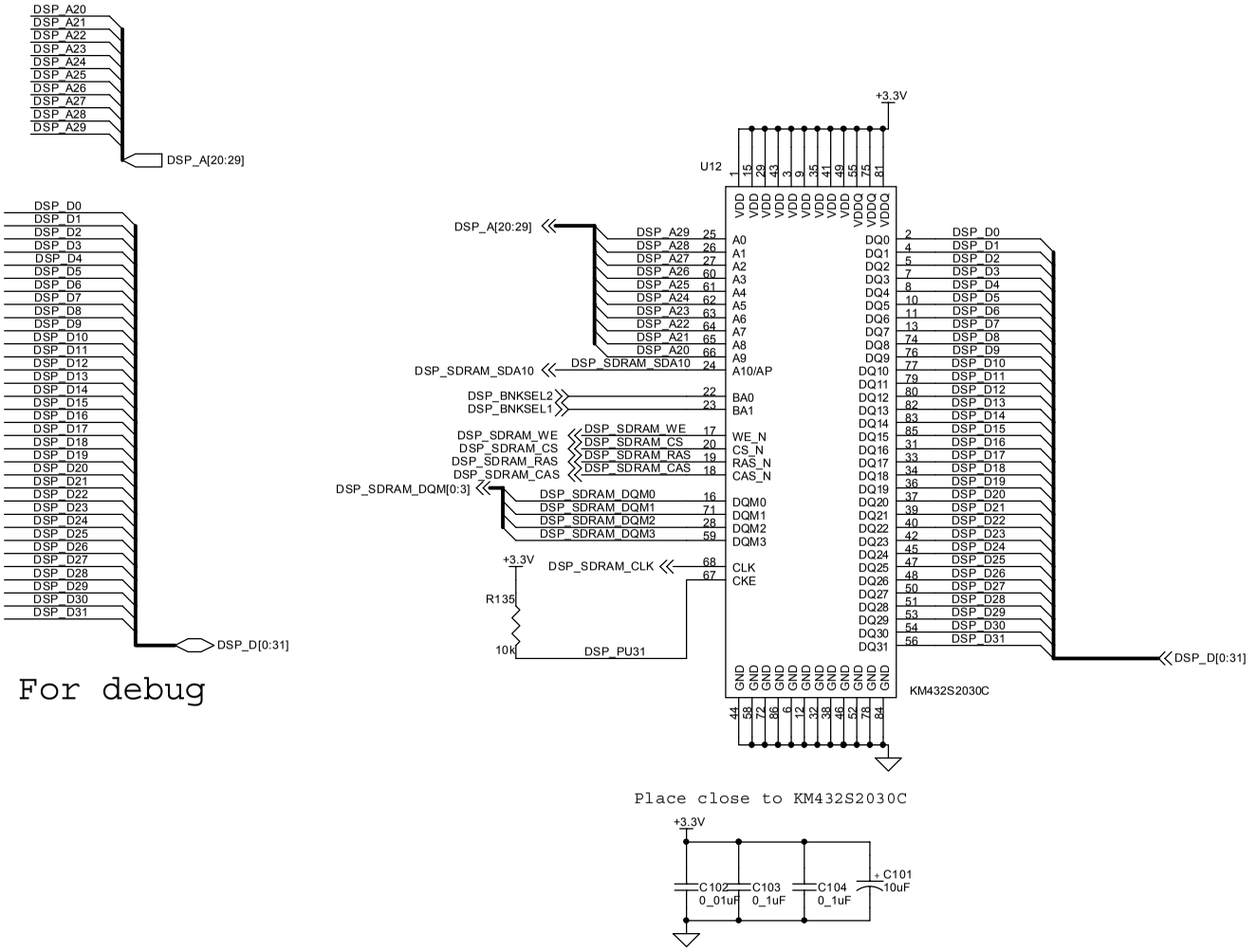
DSP POWER

Place caps as close to device as possible.

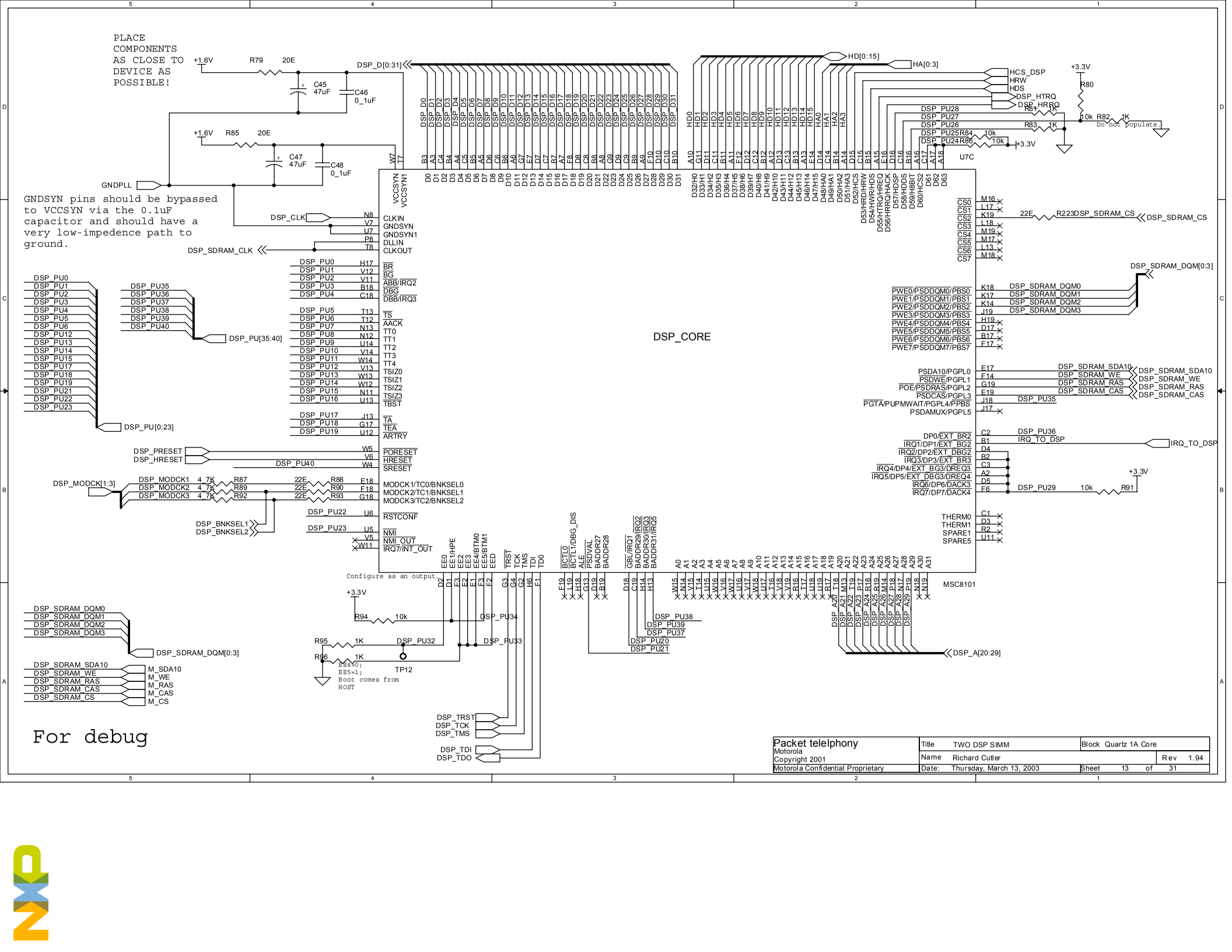




Packet telelphony Motorola Copyright 2002 Motorola Confidential Proprietary	Title TWO DSP SIMM	Block DSP_POWER	
	Name Rich Cutler		Rev 1.94
	Date: Thursday, March 13, 2003	Sheet 11 of 31	



Packet telelphony Motorola Copyright 2002 Motorola Confidential Proprietary	Title TWO DSP SIMM	Block SDRAM	
	Name Rich Cutler		Rev 1.94
	Date: Thursday, March 13, 2003	Sheet 12 of 31	


PLACE COMPONENTS AS CLOSE TO DEVICE AS POSSIBLE!
GNDSYN pins should be bypassed to VCCSYN via the 0.1uF capacitor and should have a very low-impedence path to ground.
DSP_CORE
MSC8101
U7C
Configure as an output.
EE0=0; EE1=1; EE2=0; EE3=0; EE4=0; EE5=1; Boot comes from HOST
Do not populate.
For debug
Packet telelphony
Motorola
Copyright 2001
Motorola Confidential Proprietary
Title TWO DSP SIMM
Block Quartz 1A Core
Name Richard Cutler
Rev 1.94
Date: Thursday, March 13, 2003
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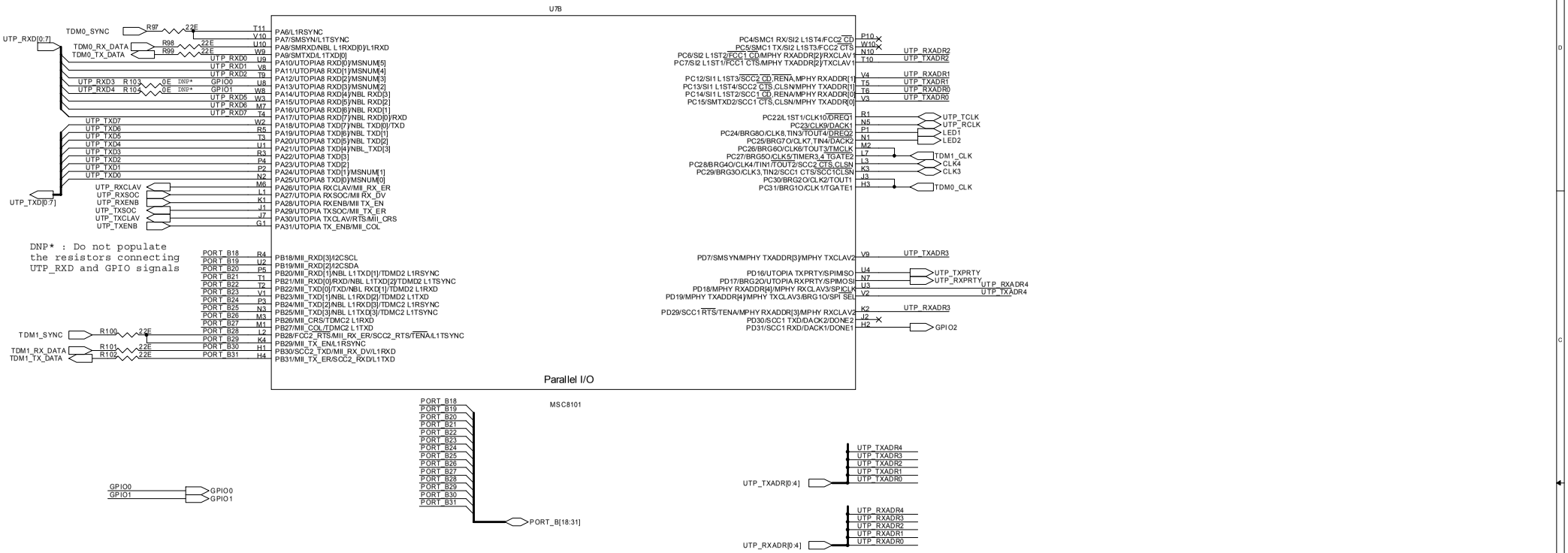
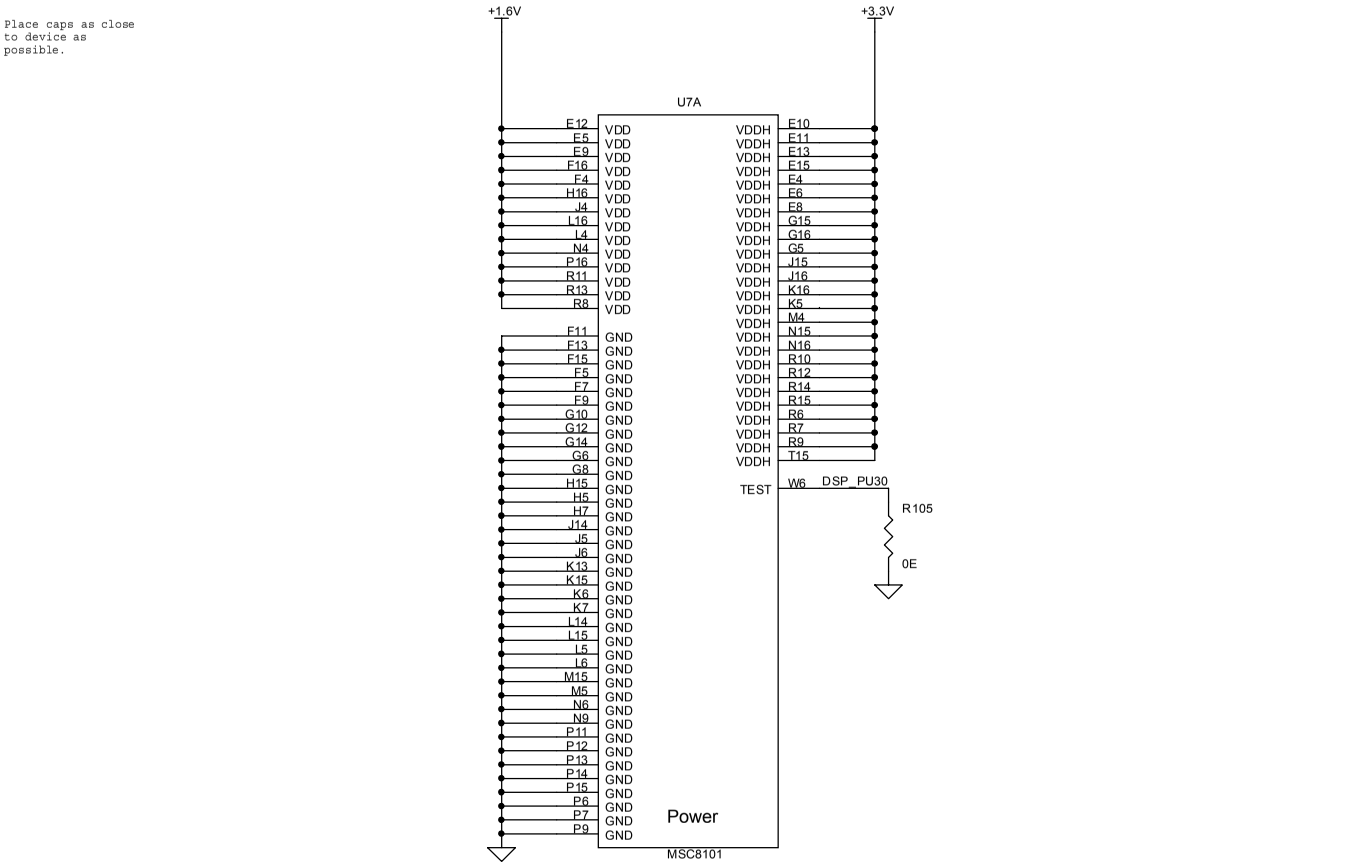
QUARTZ_1A CPM

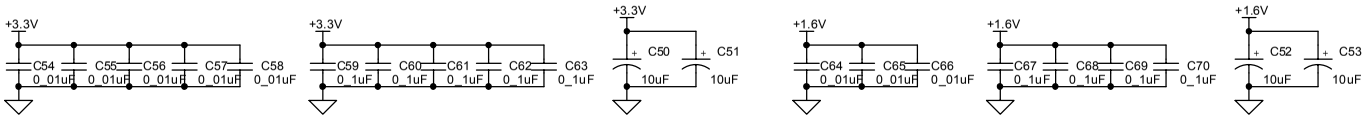


Packet telelphony Motorola Copyright 2001 Motorola Confidential Proprietary	Title: TWO DSP SIMM	Block: Quartz 1A CPM	
	Name: Richard Cutler		Rev: 1.94
	Date: Thursday, March 13, 2003	Sheet 14 of 31	

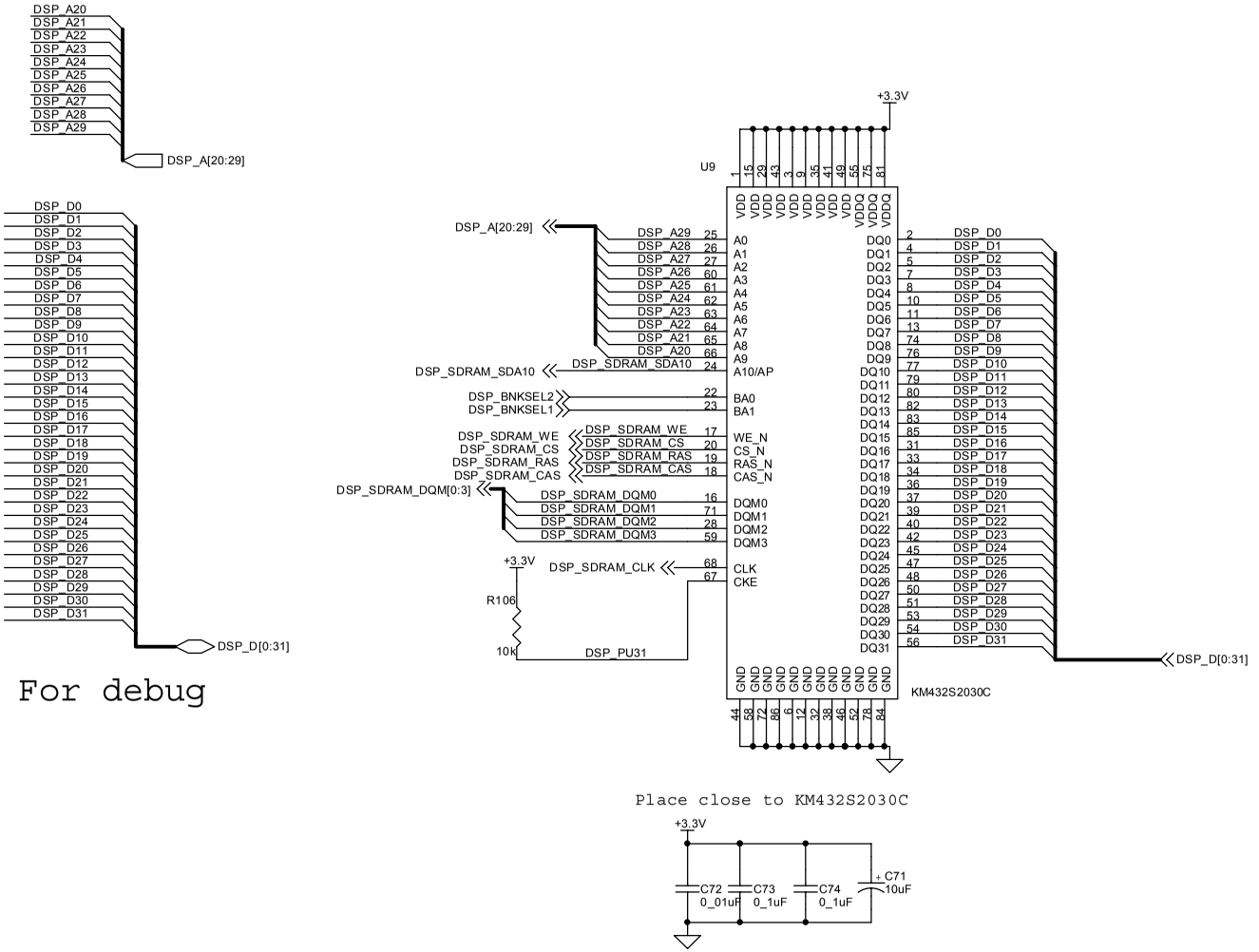
DSP POWER

Place caps as close to device as possible.

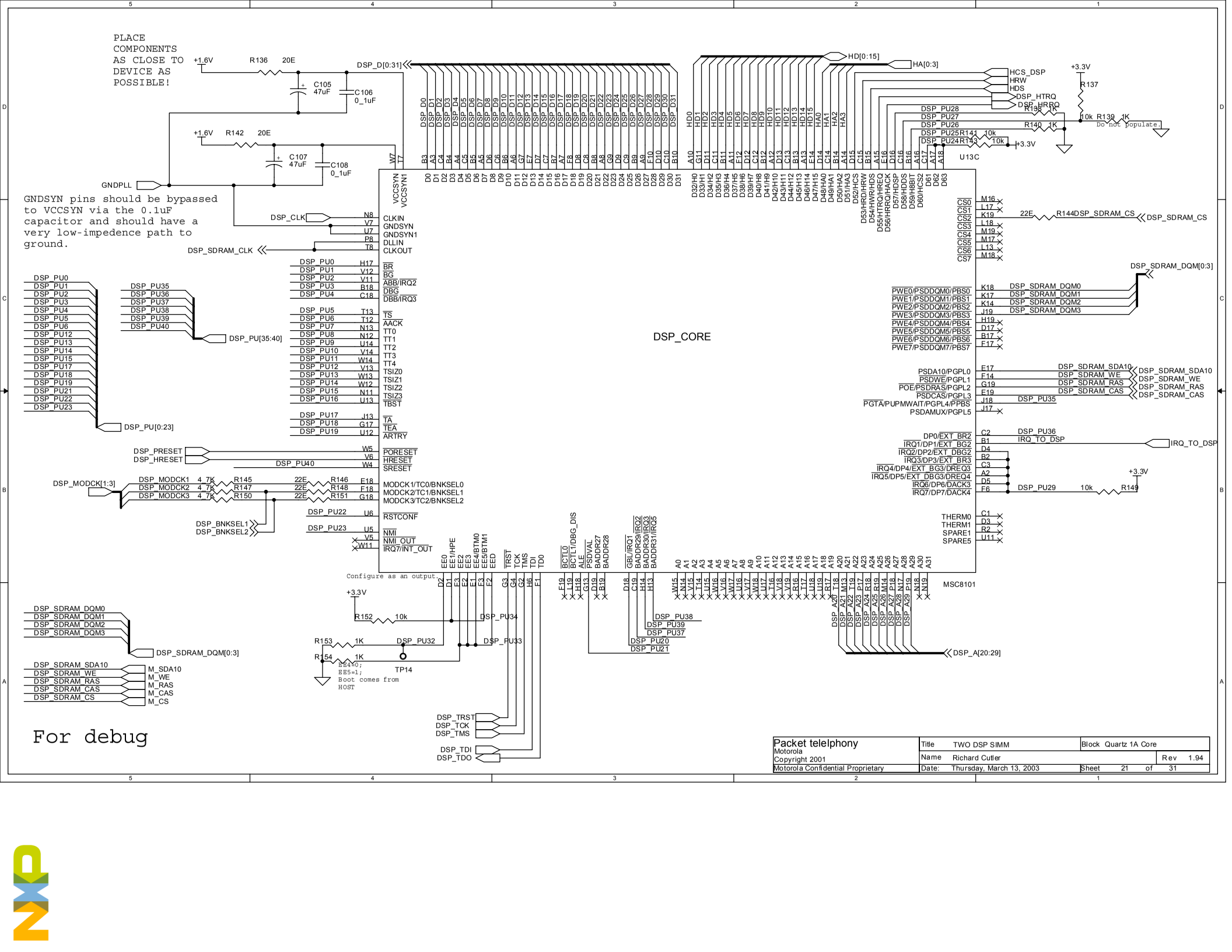




Packet telelphony Motorola Copyright 2001 Motorola Confidential Proprietary	Title TWO DSP SIMM		Block Quartz 1A Power
	Name Richard Cutler		Rev 1.94
	Date: Thursday, March 13, 2003	Sheet 19 of 31	



Packet telelphony Motorola Copyright 2001 Motorola Confidential Proprietary	Title TWO DSP SIMM	Block SDRAM G1A	
	Name Richard Cutler		Rev 1.94
	Date: Thursday, March 13, 2003	Sheet 20 of 31	


PLACE COMPONENTS AS CLOSE TO DEVICE AS POSSIBLE!
GNDSYN pins should be bypassed to VCCSYN via the 0.1uF capacitor and should have a very low-impedence path to ground.
DSP_CORE
MSC8101
U13C
Configure as an output.
EE0=0; EE5=1; Boot comes from HOST
For debug
Packet telelphony
Motorola
Copyright 2001
Motorola Confidential Proprietary
Title TWO DSP SIMM
Block Quartz 1A Core
Name Richard Cutler
Rev 1.94
Date: Thursday, March 13, 2003
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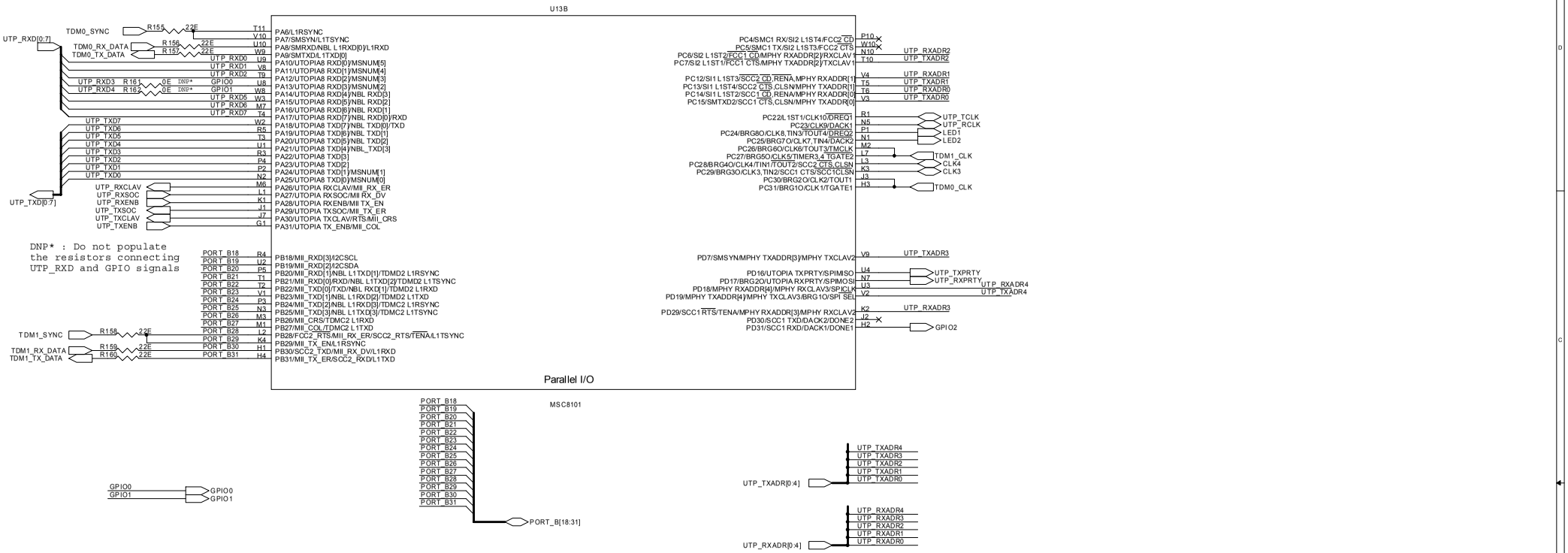
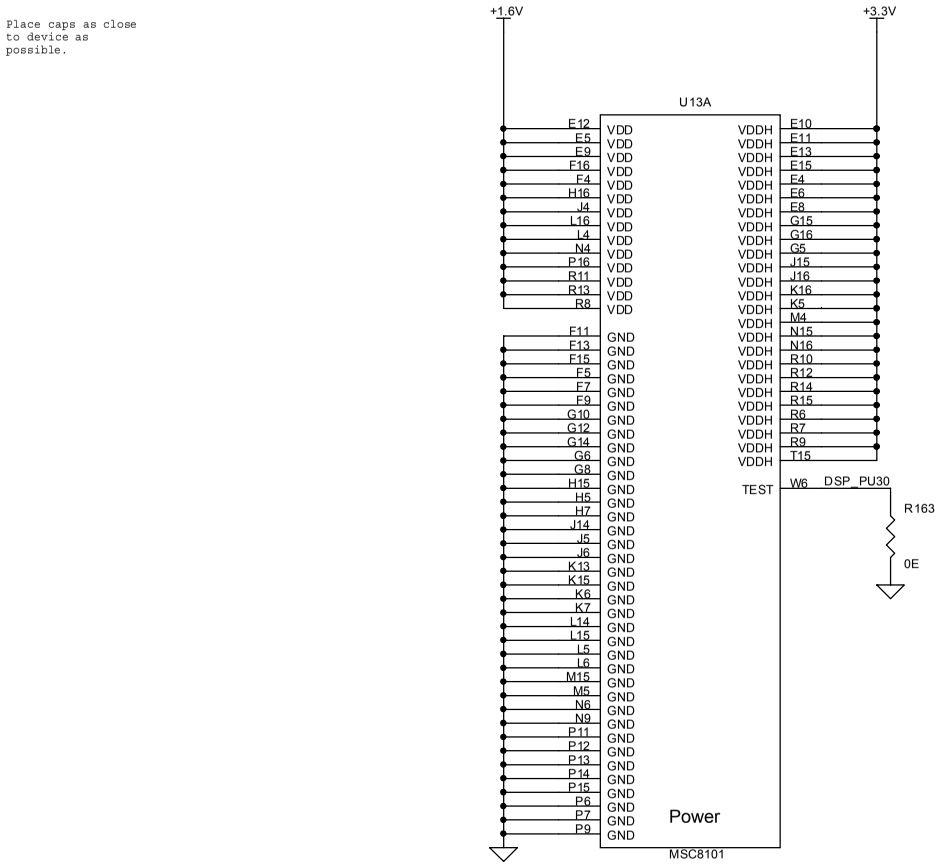
QUARTZ_1A CPM

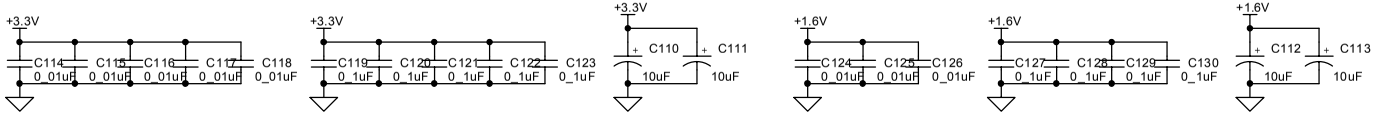


Packet telelphony Motorola Copyright 2001 Motorola Confidential Proprietary	Title: TWO DSP SIMM	Block: Quartz 1A CPM	
	Name: Richard Cutler		Rev: 1.94
	Date: Thursday, March 13, 2003	Sheet 22 of 31	

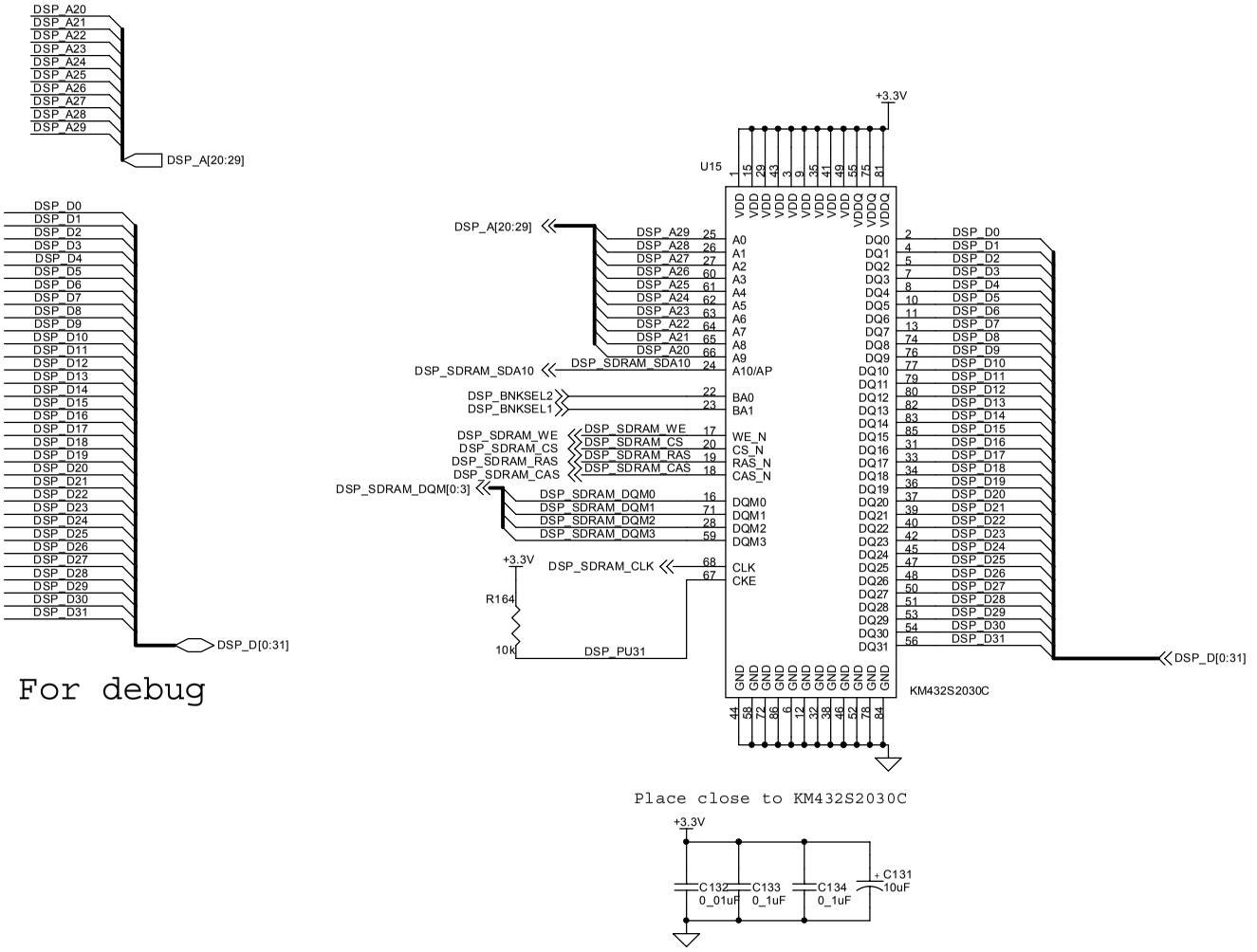
DSP POWER

Place caps as close to device as possible.

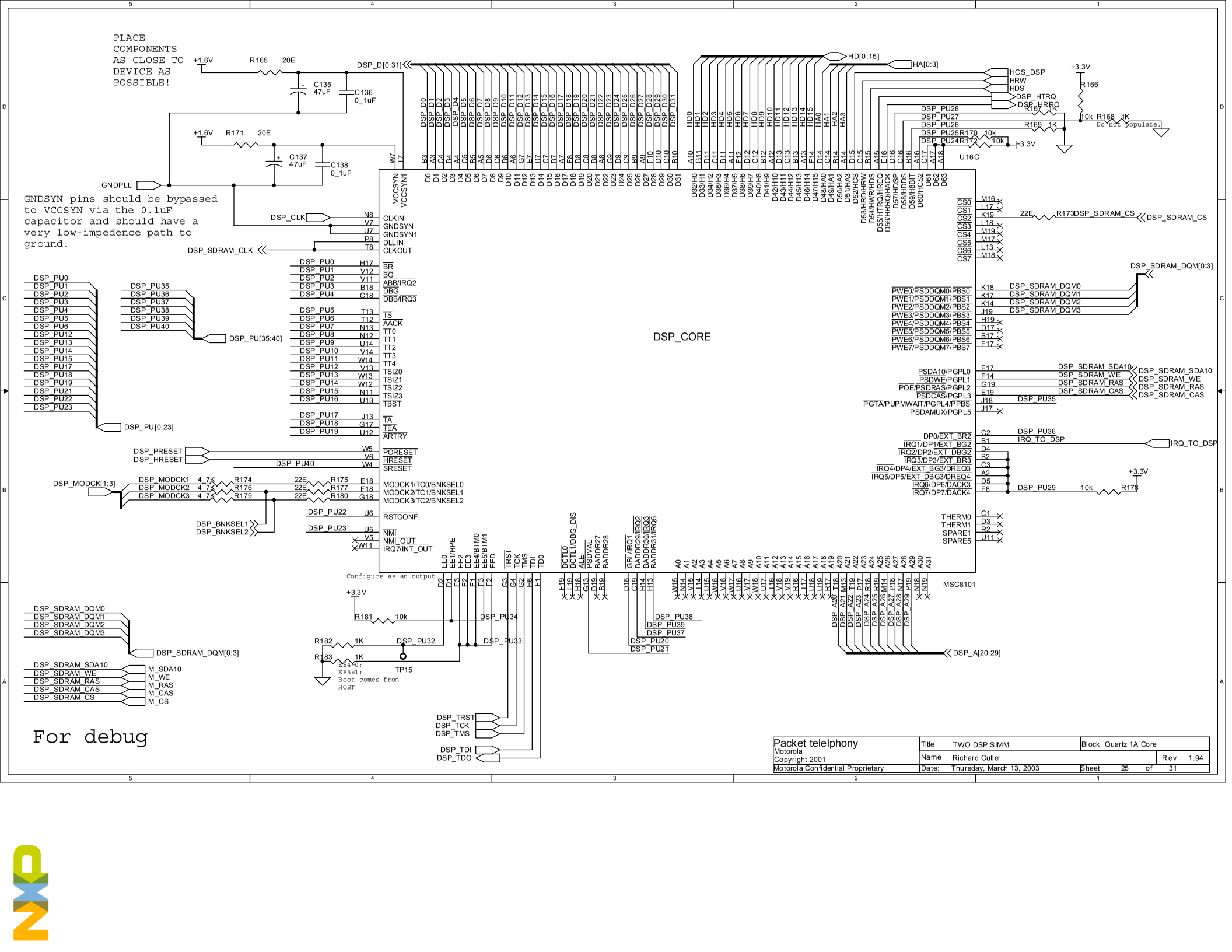




Packet telelphony Motorola Copyright 2001 Motorola Confidential Proprietary	Title TWO DSP SIMM		Block Quartz 1A Power
	Name Richard Cutler		Rev 1.94
	Date: Thursday, March 13, 2003	Sheet 23 of 31	



Packet telelphony Motorola Copyright 2001 Motorola Confidential Proprietary	Title TWO DSP SIMM	Block SDRAM G1A	
	Name Richard Cutler		Rev 1.94
	Date: Thursday, March 13, 2003	Sheet 24 of 31	


PLACE COMPONENTS AS CLOSE TO DEVICE AS POSSIBLE!
GNDSYN pins should be bypassed to VCCSYN via the 0.1uF capacitor and should have a very low-impedence path to ground.
DSP_CORE
MSC8101
U16C
Configure as an output.
EE4=0; EE5=1; Boot comes from HOST
Do not populate.
For debug
Packet telelphony
Motorola
Copyright 2001
Motorola Confidential Proprietary
Title TWO DSP SIMM
Block Quartz 1A Core
Name Richard Cutler
Rev 1.94
Date: Thursday, March 13, 2003
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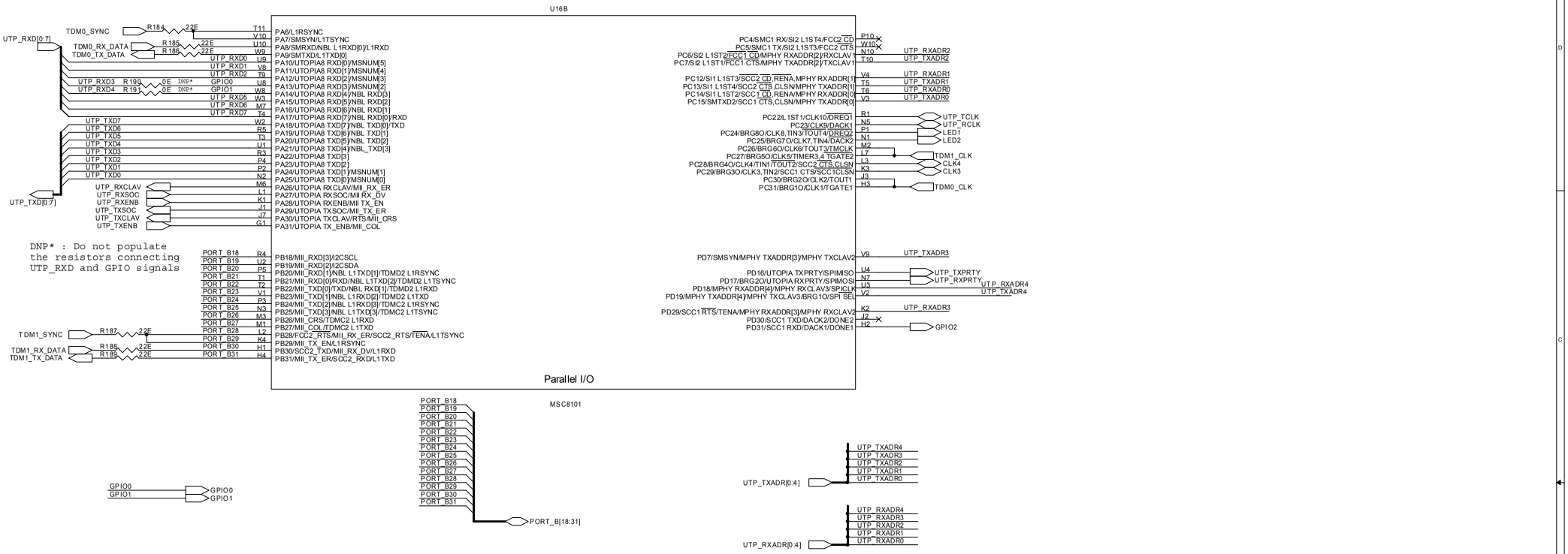
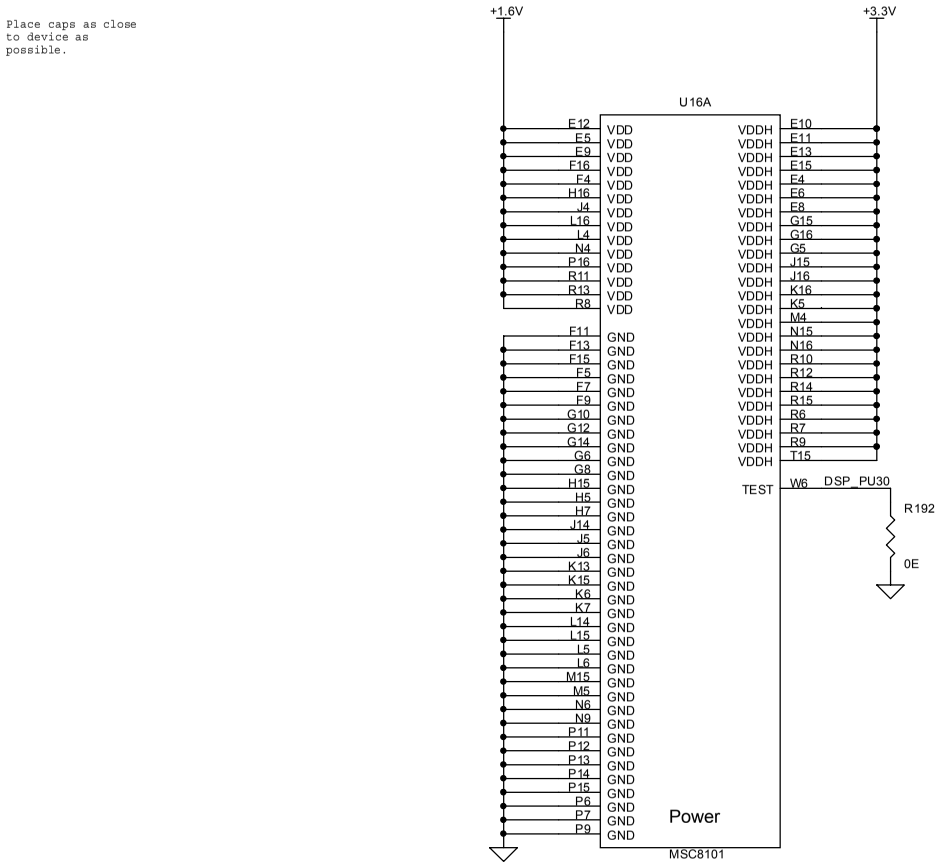
QUARTZ_1A CPM

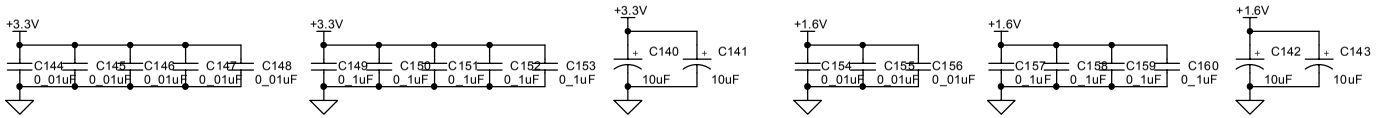


Packet telelphony Motorola Copyright 2001 Motorola Confidential Proprietary	Title: TWO DSP SIMM	Block: Quartz 1A CPM	
	Name: Richard Cutler		Rev: 1.94
	Date: Thursday, March 13, 2003	Sheet 26 of 31	

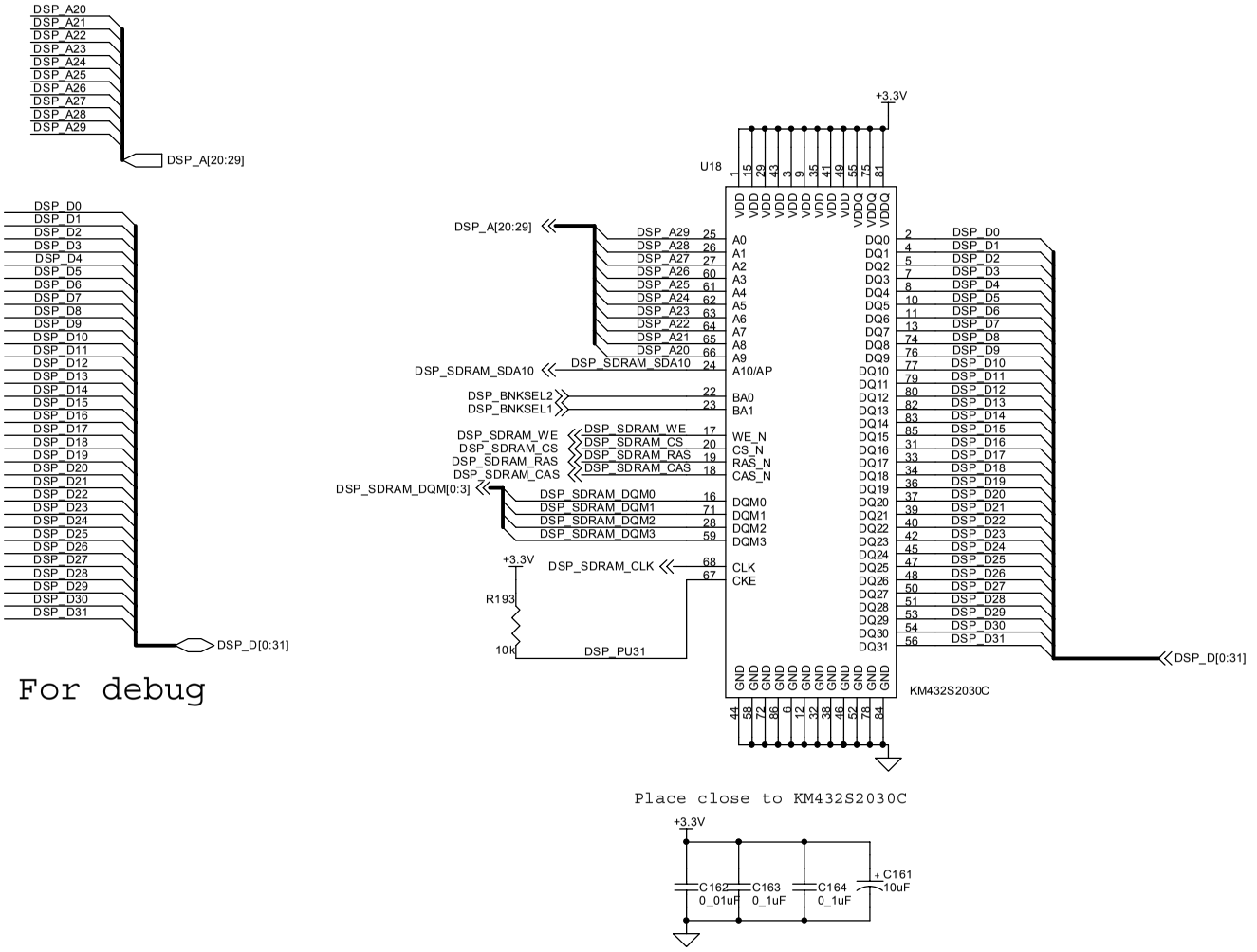
DSP POWER

Place caps as close to device as possible.

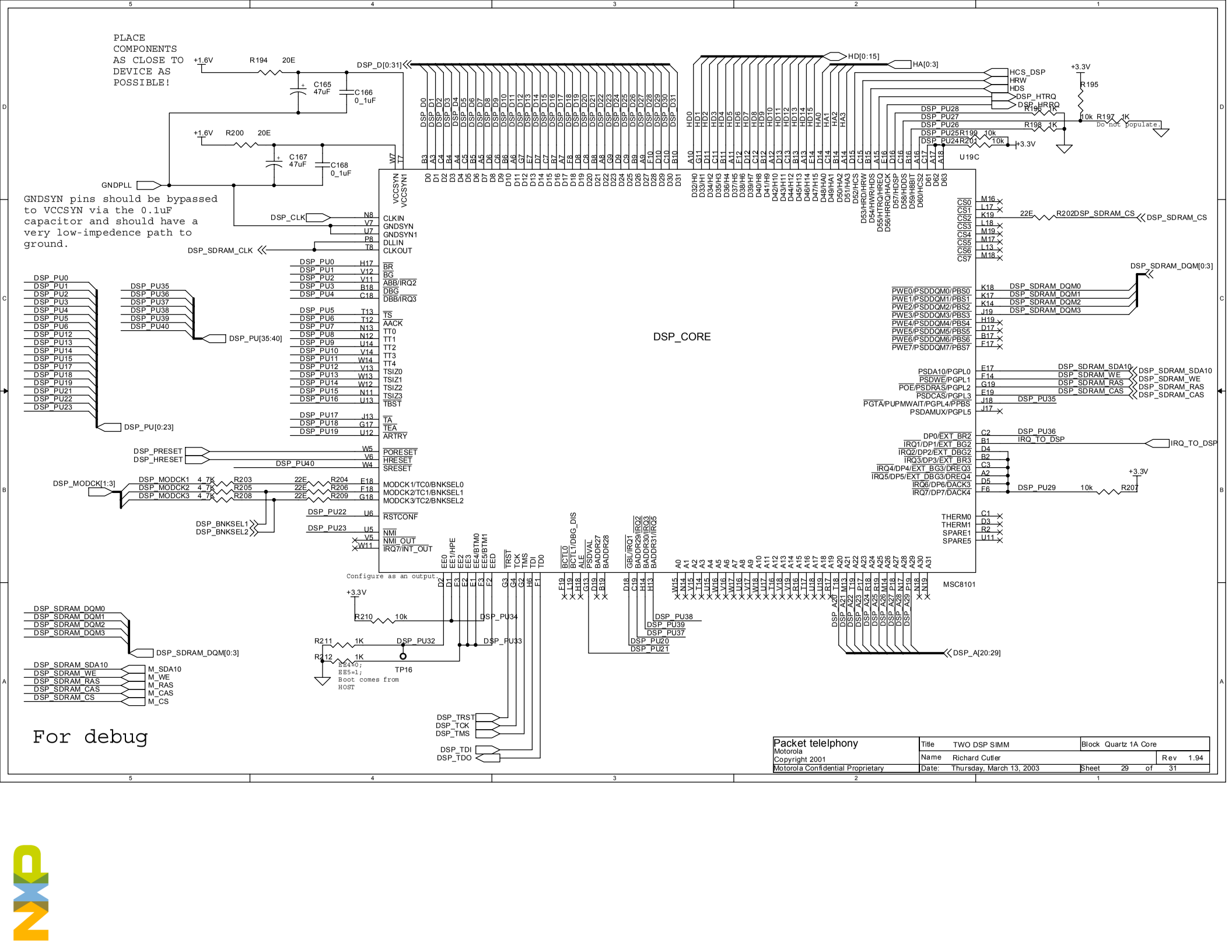




Packet telelphony Motorola Copyright 2001 Motorola Confidential Proprietary	Title TWO DSP SIMM		Block Quartz 1A Power
	Name Richard Cutler		Rev 1.94
	Date: Thursday, March 13, 2003	Sheet 27 of 31	



Packet telelphony Motorola Copyright 2001 Motorola Confidential Proprietary	Title TWO DSP SIMM	Block SDRAM G1A	
	Name Richard Cutler		Rev 1.94
	Date: Thursday, March 13, 2003	Sheet 28 of 31	


PLACE COMPONENTS AS CLOSE TO DEVICE AS POSSIBLE!
GNDSYN pins should be bypassed to VCCSYN via the 0.1uF capacitor and should have a very low-impedence path to ground.
DSP_CORE
MSC8101
Configure as an output.
EE4=0; EE5=1; Boot comes from HOST
For debug
Packet telelphony
Motorola
Copyright 2001
Motorola Confidential Proprietary
Title TWO DSP SIMM
Block Quartz 1A Core
Name Richard Cutler
Rev 1.94
Date: Thursday, March 13, 2003
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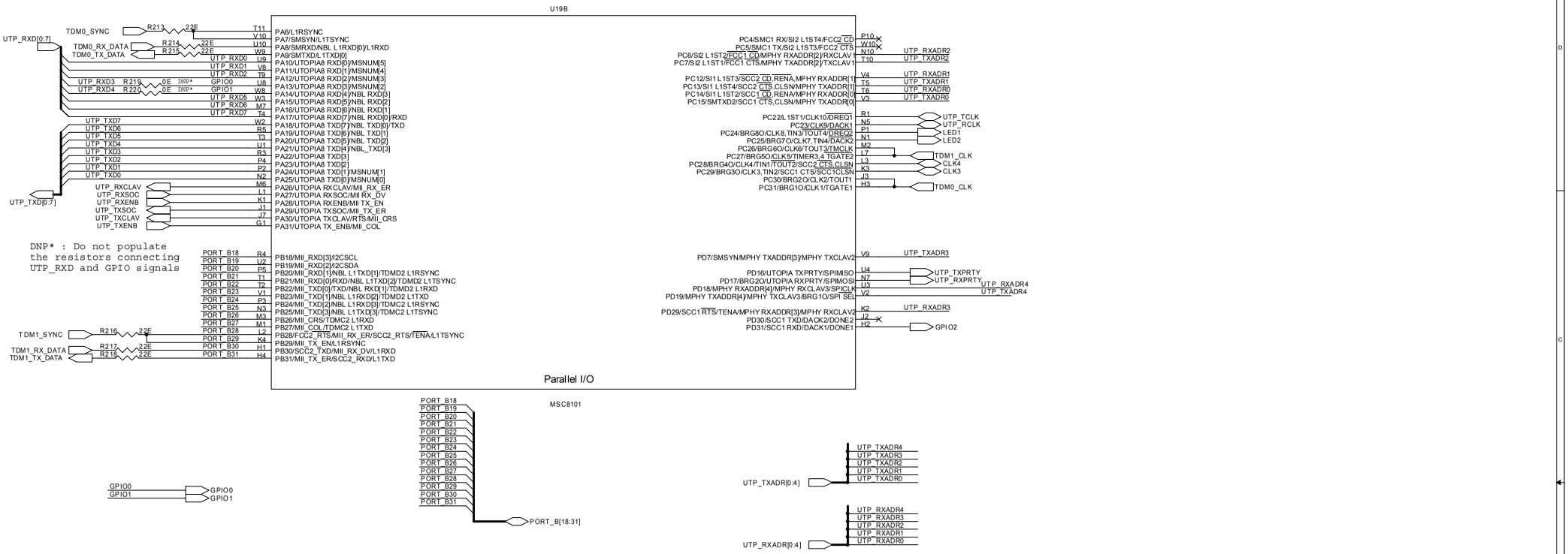
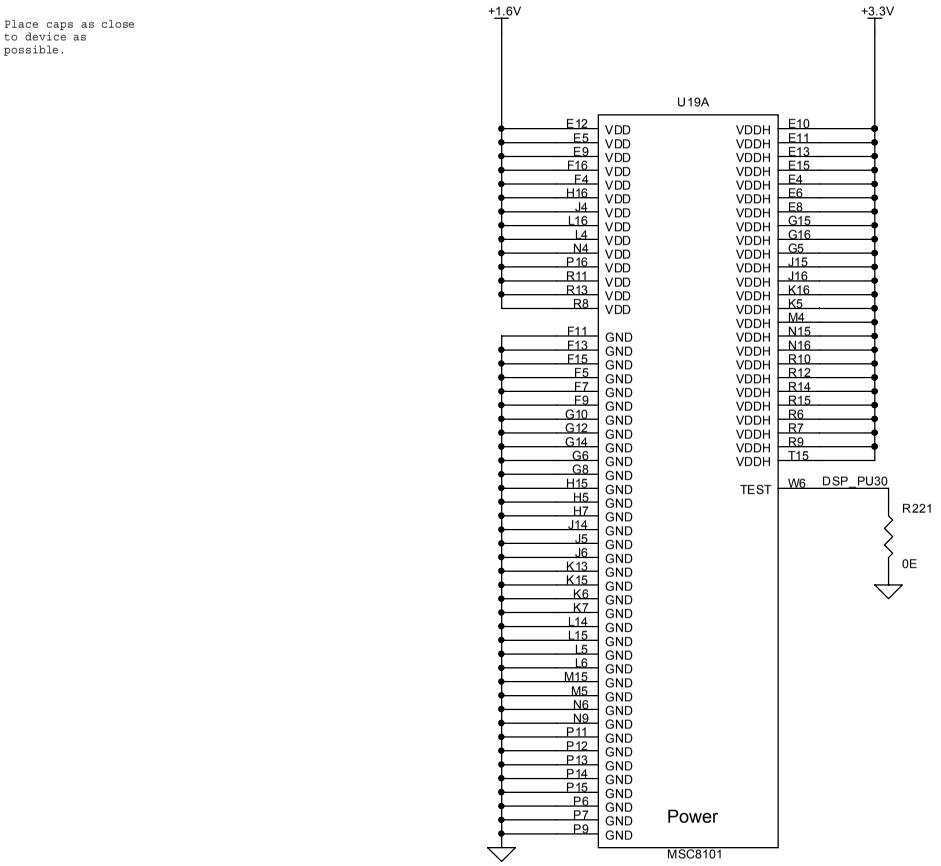
QUARTZ_1A CPM

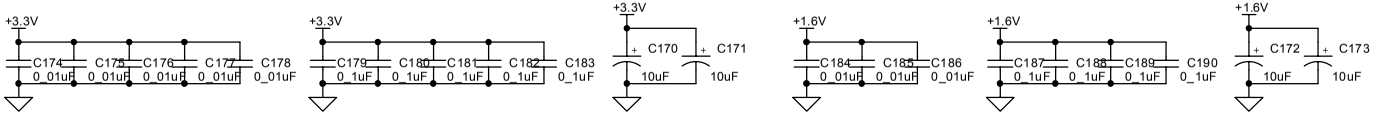


Packet telelphony Motorola Copyright 2001 Motorola Confidential Proprietary	Title: TWO DSP SIMM	Block: Quartz 1A CPM	
	Name: Richard Cutler		Rev: 1.94
	Date: Thursday, March 13, 2003	Sheet: 30 of 31	

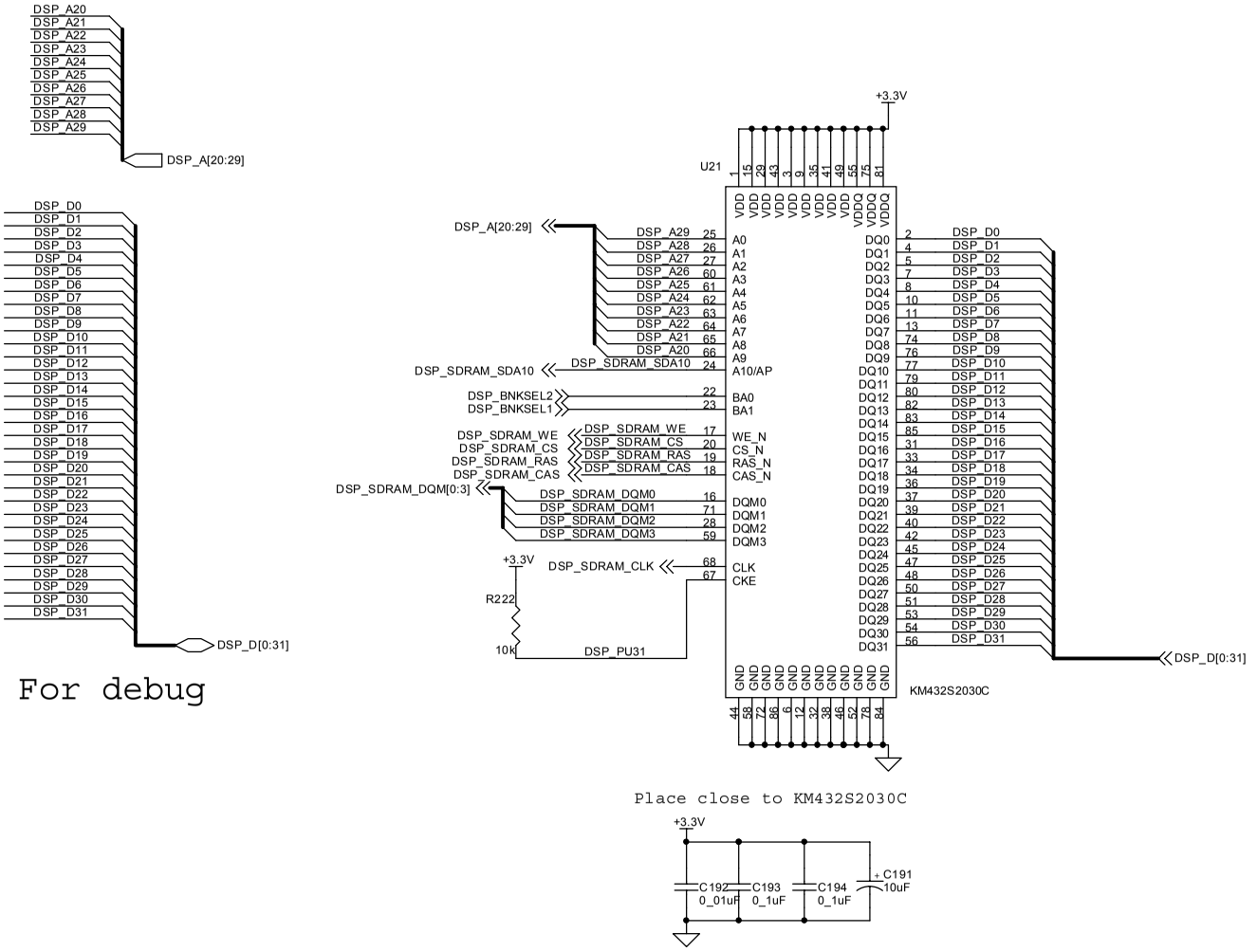
DSP POWER

Place caps as close to device as possible.

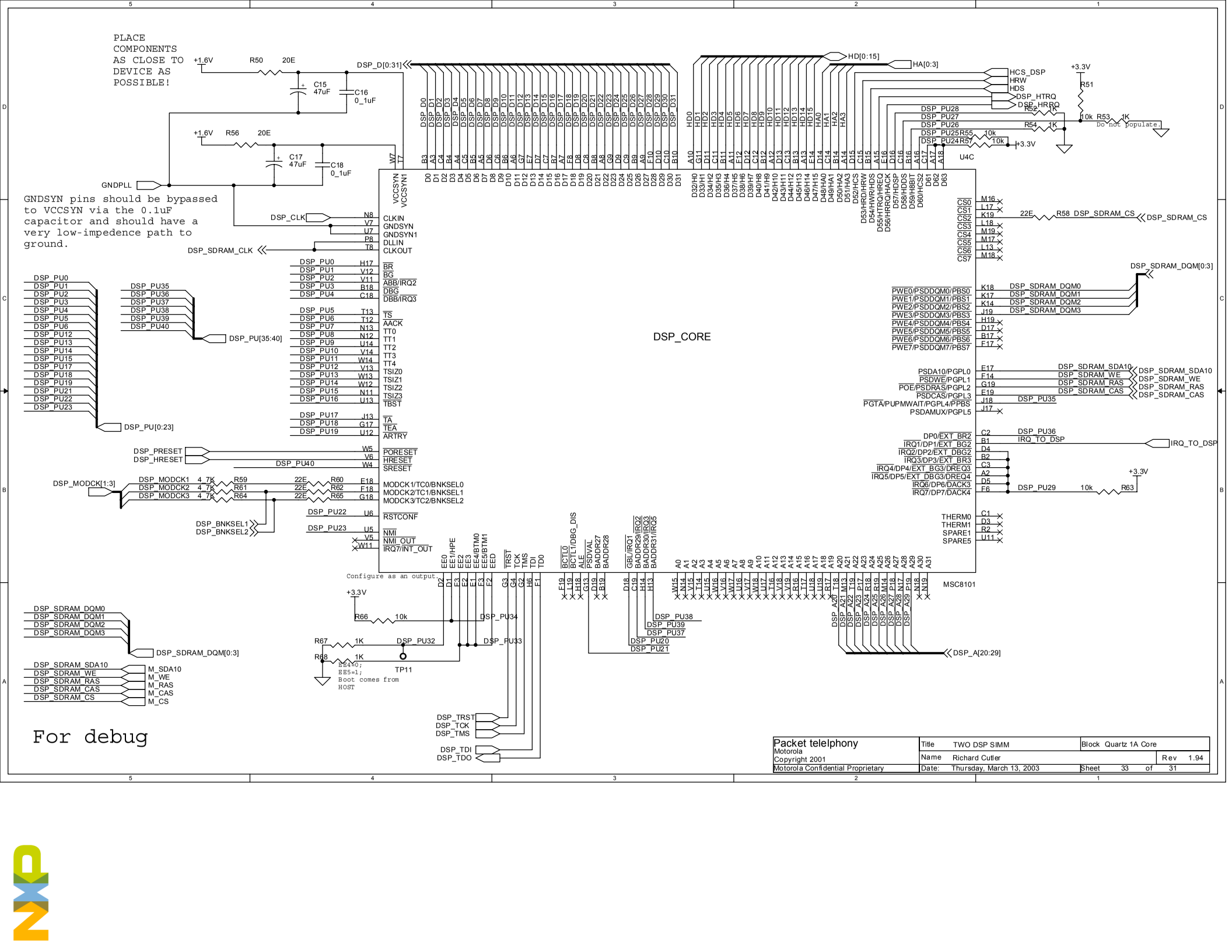




Packet telelphony Motorola Copyright 2001 Motorola Confidential Proprietary	Title TWO DSP SIMM	Block Quartz 1A Power	
	Name Richard Cutler		Rev 1.94
	Date: Thursday, March 13, 2003	Sheet 31 of 31	



Packet telelphony Motorola Copyright 2001 Motorola Confidential Proprietary	Title TWO DSP SIMM	Block SDRAM G1A	
	Name Richard Cutler		Rev 1.94
	Date: Thursday, March 13, 2003	Sheet 32 of 31	


PLACE COMPONENTS AS CLOSE TO DEVICE AS POSSIBLE!
GNDSYN pins should be bypassed to VCCSYN via the 0.1uF capacitor and should have a very low-impedence path to ground.
DSP_CORE
MSC8101
U4C
Configure as an output.
EE0=1; EE1=0; EE4=0; EE5=1; Boot comes from HOST
Do not populate.
For debug
Packet telelphony
Motorola
Copyright 2001
Motorola Confidential Proprietary
Title TWO DSP SIMM
Block Quartz 1A Core
Name Richard Cutler
Rev 1.94
Date: Thursday, March 13, 2003
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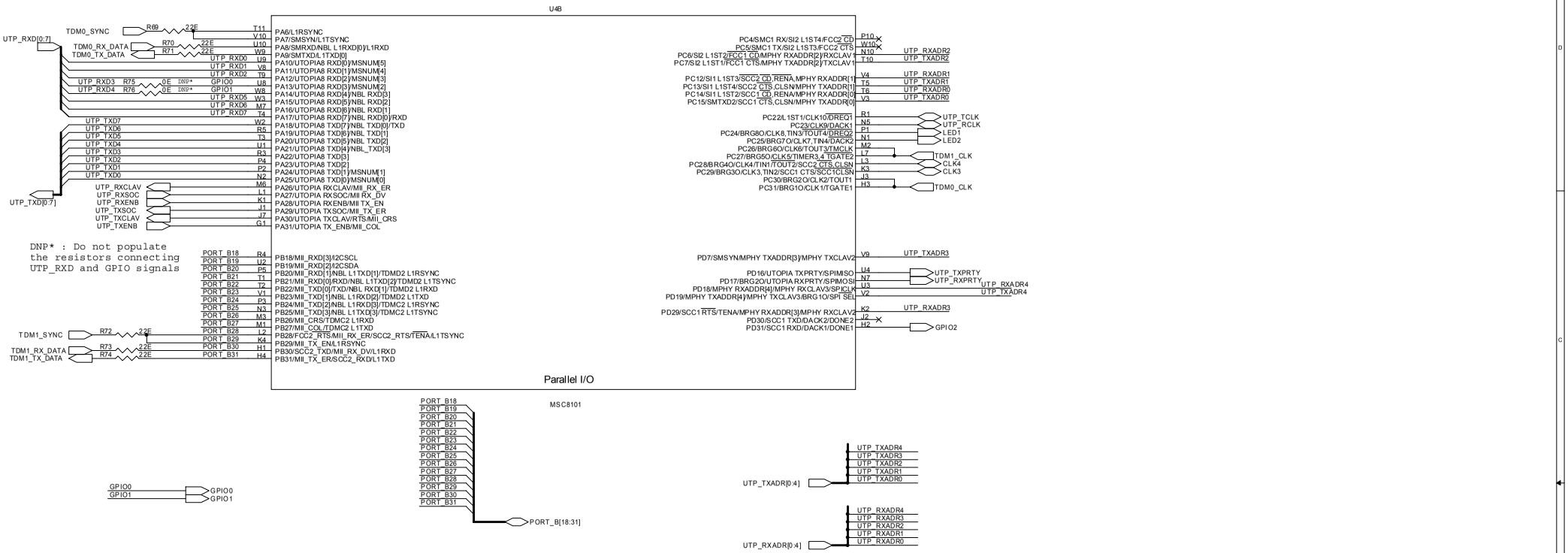
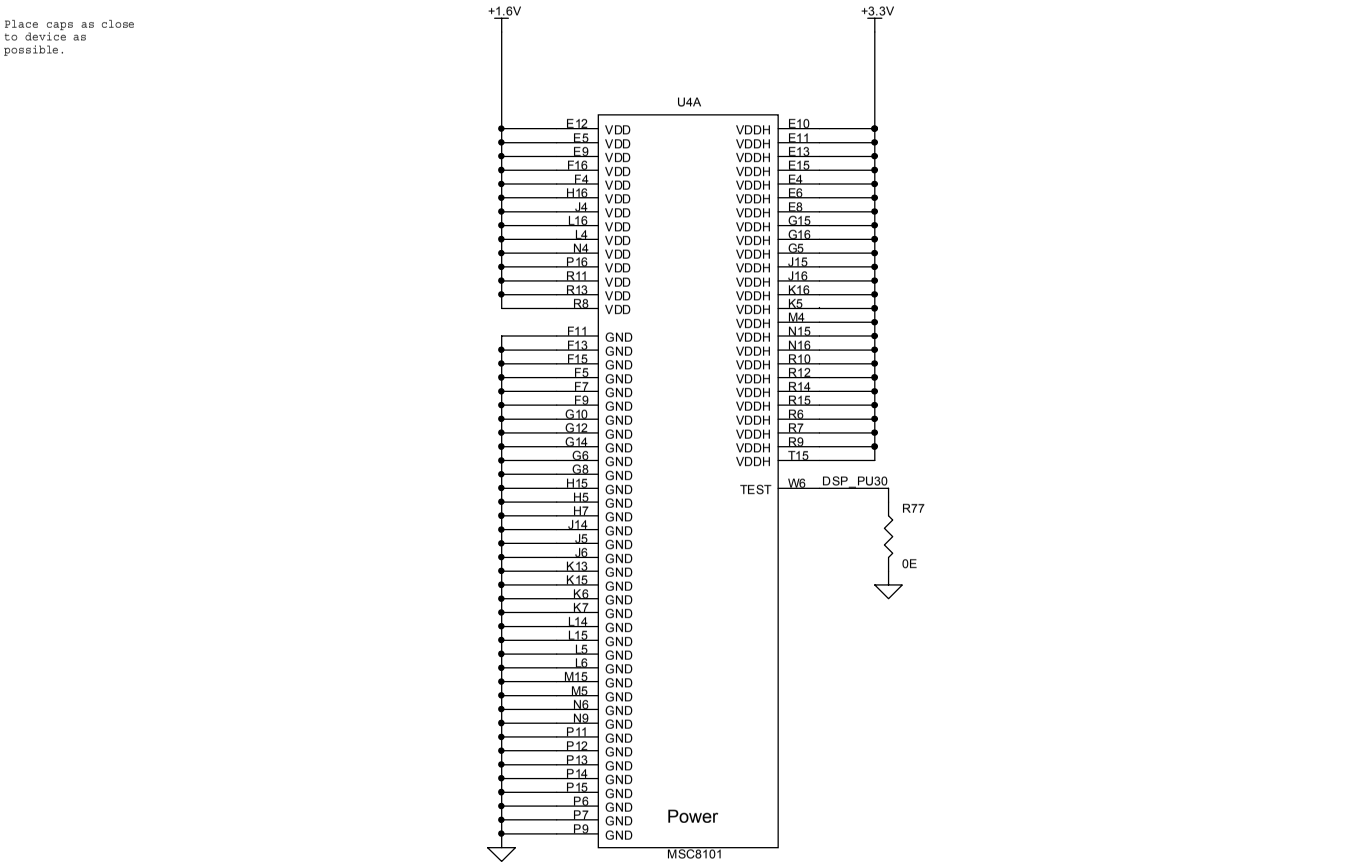
QUARTZ_1A CPM

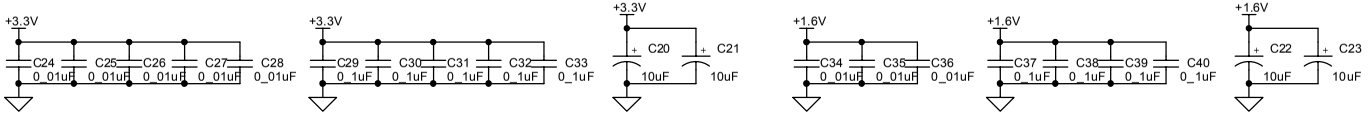


Packet telelphony Motorola Copyright 2001 Motorola Confidential Proprietary	Title: TWO DSP SIMM	Block: Quartz 1A CPM	
	Name: Richard Cutler		Rev: 1.94
	Date: Thursday, March 13, 2003	Sheet 34 of 31	

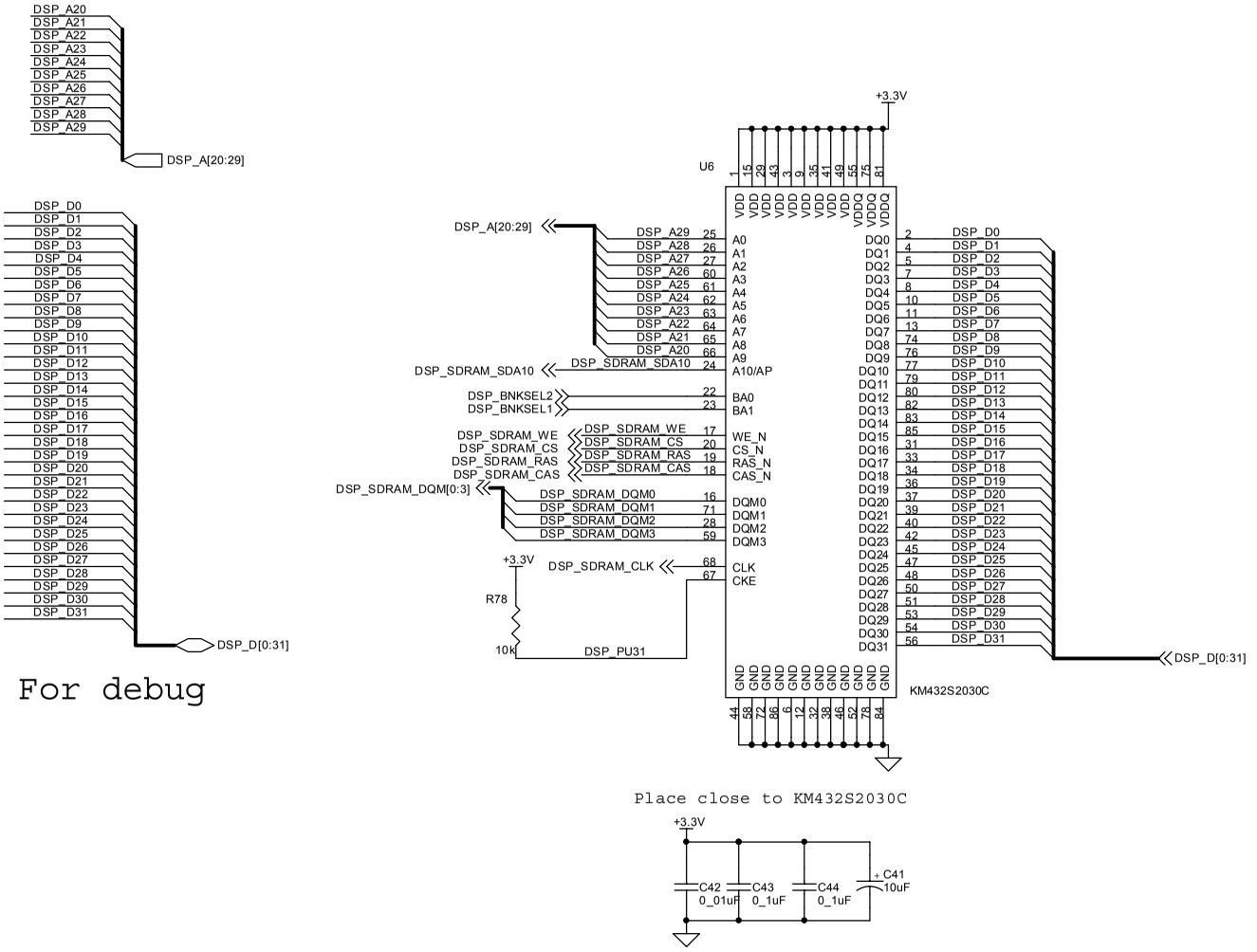
DSP POWER

Place caps as close to device as possible.





Packet telelphony Motorola Copyright 2001 Motorola Confidential Proprietary	Title TWO DSP SIMM		Block Quartz 1A Power
	Name Richard Cutler		Rev 1.94
	Date: Thursday, March 13, 2003	Sheet 35 of 31	



Packet telelphony Motorola Copyright 2001 Motorola Confidential Proprietary	Title TWO DSP SIMM	Block SDRAM G1A	
	Name Richard Cutler		Rev 1.94
	Date: Thursday, March 13, 2003	Sheet 36 of 31	

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