This user manual describes how the TEA1795T demo board can be used in a resonant converter. In addition to the TEA1795T, the demo board contains two power MOSFETs and output capacitors. There are two versions of the demo board available: 6 A, 30 V and 20 A, 12 V. The demo board replaces the secondary part of the resonant converter, excluding the feedback hardware.
Contact information

For more information, please visit: [http://www.nxp.com](http://www.nxp.com)

For sales office addresses, please send an email to: salesaddresses@nxp.com
1. Introduction

This document describes the TEA1795T demo board. A functional description is provided, supported by a set of measurements illustrating the performance of the TEA1795T. The demo board contains the secondary part of a single output LLC converter, excluding the control hardware. To use the demo board correctly, an LLC converter board in which the secondary part can be replaced by the demo board is required. Furthermore, two sense wires need to be connected to the control hardware to provide the feedback loop for controlling the output voltage.

2. The TEA1795T

The TEA1795T is a dual Synchronous Rectifier (SR) driver IC (or SR driver) for resonant converters. It can easily drive MOSFETs used to replace the rectifier diodes on the secondary side.

A simple control algorithm built into the IC determines when a MOSFET needs to be turned on or off: at $V_{DS} = -220$ mV the MOSFET is turned on; between $-25$ mV and $-12$ mV the IC will be in Regulation mode; above $-12$ mV the MOSFET will be turned off. In Regulation mode, the drain-source voltage is held constant at $-25$ mV to minimize turn-off time.

A simplified state diagram of the TEA1795T is shown in Figure 1. The $-25$ mV level was built in to minimize the turn-off delay time (at the expense of additional dissipation). In addition, two blanking time periods were added to prevent spurious switching after a MOSFET is turned on or off.

![Simplified state diagram of the TEA1795T](image)

Fig 1. Simplified state diagram of the TEA1795T

To measure the drain-source voltage of the MOSFETs, sense pins DSA and SSA are connected, respectively, to the drain and source of MOSFET A. Sense pins DSB and SSB are connected to MOSFET B. In addition to the voltage drop due to $R_{Dson}$ of the
MOSFETs, voltage drops are present across the tracks and the package. Incorporating two separate sense pins (SSA and SSB) helps to minimize the influence of these voltage drops.

![Pin configuration](image)

**3. Demo board setup**

To ensure the demo board can be used in a variety of applications, two versions are available: TEA1795T demo board v1 contains two NXP Semiconductors PSMN025-100D (100 V 25 mΩ DPAK) power MOSFETS and is intended for high-voltage, low-current applications (e.g. as a notebook adaptor). TEA1795T demo board v2 contains two NXP Semiconductors PSMN4R5-40PS (40 V 4.5 mΩ TO220) power MOSFETS and was designed for low-voltage, high-current applications (e.g. in a desktop PC power supply). Because of the small heat sink included in the TEA1795T demo board v2, a fan should be used for forced cooling.

**Remark:** The heat sinks are connected to the MOSFET drains in both versions of the demo board. It is possible to modify the TEA1795T demo board v2 to connect the heat sink to ground.

The demo boards were designed to be incorporated into an existing resonant power supply, by replacing the secondary circuit. The demo board is connected to the secondary side of the transformer.

Note that when replacing a diode in the high-voltage line of the transformer with a MOSFET located in the ground path, the center tap of the transformer must be disconnected from ground and connected to $V_{out}$ (see Figure 3). Note also that no provisions have been made to provide a feedback loop to control the output voltage of the demo board. Therefore, connections are needed between the two PCBs to close the loop (see Figure 4). The points on the demo board where the secondary side of the transformer, the feedback loop and the output wires should be connected are illustrated in Figure 5.
Fig 3. Connecting the transformer to the demo board

Fig 4. Connecting the control loop to the demo board

- Replace diode with MOSFET
- Connect to GND (instead of V_{out})
- Connect to V_{O} (instead of GND)
- Connect to GND (instead of V_{out})
- Replace diode with MOSFET

019aaa776
Low-pass filters (R1 & C1 and R2 & C2) are used to filter out ringing in the drain-source voltage caused by the part of the secondary winding that is not coupled to the main secondary winding and the drain-source capacitance. This filtering is needed to prevent the MOSFETs being turned on by mistake. A plot of the ringing in the drain-source voltage is shown in Figure 6. Ringing occurs when one of the MOSFETs stops conducting current or when the half-bridge voltage is changing (rising/falling).
As discussed in application note AN10954, measurement of the drain-source voltage includes voltage drops across the tracks, bonding wires, and the pins of the package. These voltages drops are due, in part, to parasitic inductance, which can lead to serious measurement errors. The RC filters provided on the demo boards to filter out drain-source ringing can also be used to compensate for parasitic inductance. The influence of the parasitic inductance can be minimized by satisfying the following equation:

$$\frac{L_{par}}{R_{DSon}} = R_x \times C_x \quad (x = 1 \text{ or } 2)$$

The magnitude of the parasitic inductance depends on the package used and is much higher in a TO220 package than in a DPAK package. Drain-source ringing is more of an issue with a DPAK package. The dimensioning of the filters in the demo boards takes account of this. RC filter tuning on the TEA1795T demo board v1 is biased towards filtering drain-source ringing whereas the filters on the TEA1795T demo board v2 are optimized to reduce parasitic inductance.

With the TEA1795T demo board v2, the mode of operation of the converter needs to be taken into account. The dimensions of the compensation filter were calculated for Discontinuous Current Mode (DCM). The filter has not been optimized for Continuous Current Mode (CCM), and will need to be adjusted since parasitic inductance has less influence at the instant the MOSFET is turned off. The plot in Figure 7 was measured with the converter in CCM mode, $C_1 = 0 \text{ pF}$ and $I_{load} = 10 \text{ A}$.

Parasitic inductance causes the MOSFETs to turn off too early (premature turn-off). It is clear from Figure 7 and Figure 8 that the influence of parasitic inductance is much greater in DCM mode (1.2 $\mu$s) than in CCM mode (200 ns).
When the filter design is determined primarily by the value of the parasitic inductance (TO220 package), the voltage on the capacitor is clamped by a MOSFET or by an RF-diode with a low voltage drop to avoid a lengthy discharge time.
Adding an external filter reduces the premature turn-off time but increases the turn-on delay time. Ideally, the turn-on delay and premature turn-off times should be equal. The increase in the turn-on delay time can be limited by adding a clamping diode over Cx (see Figure 9).

Adding an external filter reduces the premature turn-off time but increases the turn-on delay time. Ideally, the turn-on delay and premature turn-off times should be equal. The increase in the turn-on delay time can be limited by adding a clamping diode over Cx (see Figure 9).

Increasing the size of the capacitor will increase the turn-on delay time and reduce the premature turn-off time (shifting the waveform to the right see; Figure 10).

A 1 μA (max) current flows through pins DSA and DSB. Therefore, in order to ensure the voltage drop across the resistors does not exceed 4 mV, R1 = R2 = 3.9 kΩ.
A schematic of the TEA1795T demo board v2 is shown in Figure 11. The differences between the two demo boards are summarized in Table 1. The component placement is shown in Figure 12 and Figure 13.

The schematic of the TEA1795T demo board v1 is identical but with component values changed as indicated in Table 1.

Fig 11. Circuit diagram of the TEA1795T demo board v2

Table 1. Differences between demo boards

<table>
<thead>
<tr>
<th>Component</th>
<th>TEA1795T demo board v1</th>
<th>TEA1795T demo board v2</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>not mounted</td>
<td>150 pF/10 %/50 V/NPO</td>
</tr>
<tr>
<td>C2</td>
<td>not mounted</td>
<td>150 pF/10 %/50 V/NPO</td>
</tr>
<tr>
<td>C4</td>
<td>1000 µF/20 %/35 V; Rubycon ZL</td>
<td>2200 µF/20 %/16 V; Rubycon ZL</td>
</tr>
<tr>
<td>C5</td>
<td>1000 µF/20 %/35 V; Rubycon ZL</td>
<td>2200 µF/20 %/16 V; Rubycon ZL</td>
</tr>
<tr>
<td>C6</td>
<td>1000 µF/20 %/35 V; Rubycon ZL</td>
<td>2200 µF/20 %/16 V; Rubycon ZL</td>
</tr>
<tr>
<td>C7</td>
<td>1000 µF/20 %/35 V; Rubycon ZL</td>
<td>2200 µF/20 %/16 V; Rubycon ZL</td>
</tr>
<tr>
<td>D3</td>
<td>not mounted</td>
<td>BAT17</td>
</tr>
<tr>
<td>D4</td>
<td>not mounted</td>
<td>BAT17</td>
</tr>
<tr>
<td>HS1</td>
<td>heat sink FK-244-08-D-PAK; Fischer</td>
<td>heat sink TO220; Redpoint</td>
</tr>
<tr>
<td>HS2</td>
<td>heat sink FK-244-08-D-PAK; Fischer</td>
<td>heat sink TO220; Redpoint</td>
</tr>
<tr>
<td>Q1</td>
<td>PSMN025-100D; NXP Semiconductors</td>
<td>PSMN4R5-40PS; NXP Semiconductors</td>
</tr>
<tr>
<td>Q2</td>
<td>PSMN025-100D; NXP Semiconductors</td>
<td>PSMN4R5-40PS; NXP Semiconductors</td>
</tr>
</tbody>
</table>

[1] C1, C2, D3 and D4 are included in the schematic diagram (Figure 12) and PCB layout drawings (Figure 21 and Figure 22) but are not mounted on the TEA1795T demo board v1.
Fig 12. Component placement: TEA1795T demo board v1 (DPAK)

Fig 13. Component placement: TEA1795T demo board v2 (TO220)
4. Operation

4.1 Turn-on and blanking time

The MOSFETs are turned on when the drain-source voltage falls below the turn-on threshold (\(-220\) mV) and the gate is charged. An internal clamping circuit limits the maximum gate voltage to approximately 10 V (see Figure 14 (a)). The minimum gate voltage (\(V_{GS}\)) will be 6 V when \(V_{CC}\) is at a minimum (\(\approx 8\) V).

A blanking time of 520 ns is built in to prevent the MOSFET turning off again immediately after turning on. After the blanking time, the gate voltage remains at the same level or is partly or totally discharged. In the plots in Figure 14, the gate remains charged. In the plot in Figure 15, the gate is discharged after the blanking time.

![Figure 14](image1.png)

- a. maximum gate voltage = 9.7 V
- b. gate voltage = 6.1 V

(1) Primary current.
(2) \(V_{CC}\).
(3) \(V_{GS}\).
(4) \(V_{DS}\).

Fig 14. Gate voltage
If $V_{DS}$ rises above $-25\, \text{mV}$, the gate will be discharged until $V_{DS}$ is again equal to $-25\, \text{mV}$ and the IC remains in Regulation mode. The gate is discharged through an internal MOSFET ($R_{DSon} = 24\, \Omega$). A 5 mA current source provides the charge current, ensuring the gate voltage rises (see slowly rising edge in Figure 15).

4.2 Regulation mode and turn-off

Regulation mode is provided in order to minimize turn-off time. In this mode, the drain-source voltage is stabilized independently of the value of the current, at $-25\, \text{mV}$ (see Figure 8 and Figure 14). If the current falls so low that it’s impossible to retain a drain-source voltage of $-25\, \text{mV}$, the MOSFET will be turned off. In Regulation mode, the gate voltage is stabilized at just above the threshold voltage for turning off the MOSFET. Therefore, only a small fall in $V_{DS}$ is needed to turn off the MOSFET.

4.3 Compromise between turn-on, turn-off and blanking times

In Figure 16 (a), a small filter ($R_1 = 3.9\, \text{k}\Omega$ and $C_1 = 0\, \text{pF}$) was added to reduce ringing. As can be seen, the turn-on behavior is close to ideal. However, the premature turn-off time is too long. The gate pulse can be shifted to the right by increasing the value of $C_x$ (to 150 pF in this example; see Figure 16 (b)) and adding a clamping diode. This improves the turn-off behavior but results in a less ideal turn-on time.
The value of $C_x$ should be selected such that the gate pulse is centered in relation to the MOSFET current. An additional blanking time has been built in to prevent spurious switching after the MOSFET has been turned off (see Figure 17).

When the blanking time has expired, it is possible to charge the gate and turn the MOSFET on again, so multiple pulses are possible (see Figure 18).
4.4 Parasitic turn-on

When $V_{DS} > -12$ mV, an internal sink MOSFET is turned on. However, it might not start conducting immediately due to an internal delay in the IC, reducing sinking capability. During the rising edge on $V_{GS}$, the MOSFET will be turned on by the Miller capacitance of the MOSFET. This is illustrated in Figure 19.
5. PCB layout

5.1 Layout considerations

To ensure optimal performance and to minimize impedance, the following guidelines should be taken into account when designing the PCB layout:

- Dedicated tracks should be used to connect the sense pins on the IC to the MOSFET pins and the tracks should be as short as possible.
- The loop area between the drain sense track and the source sense track should be as small as possible.

![Diagram of layout recommendations](image)

- DSA = drain sense input (MOSFET A)
- SSA = source sense input (MOSFET A)
- GDA = gate driver output (MOSFET A)

Fig 20. Layout recommendations
5.2 Copper pattern

Fig 21. Layout of TEA1795T demo board v1 (DPAK)

Fig 22. Layout of TEA1795T demo board v2 (TO220)
## 6. Bill of materials

<table>
<thead>
<tr>
<th>Component</th>
<th>TEA1795T demo board v1</th>
<th>TEA1795T demo board v2</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>not mounted</td>
<td>150 pF/10 %/50 V/NPO</td>
</tr>
<tr>
<td>C2</td>
<td>not mounted</td>
<td>150 pF/10 %/50 V/NPO</td>
</tr>
<tr>
<td>C3</td>
<td>220 nF/10 %/50 V (DC)</td>
<td>220 nF/10 %/50 V (DC)</td>
</tr>
<tr>
<td>C4</td>
<td>1000 μF/20 %/35 V; Rubycon ZL</td>
<td>2200 μF/20 %/16 V; Rubycon ZL</td>
</tr>
<tr>
<td>C5</td>
<td>1000 μF/20 %/35 V; Rubycon ZL</td>
<td>2200 μF/20 %/16 V; Rubycon ZL</td>
</tr>
<tr>
<td>C6</td>
<td>1000 μF/20 %/35 V; Rubycon ZL</td>
<td>2200 μF/20 %/16 V; Rubycon ZL</td>
</tr>
<tr>
<td>C7</td>
<td>1000 μF/20 %/35 V; Rubycon ZL</td>
<td>2200 μF/20 %/16 V; Rubycon ZL</td>
</tr>
<tr>
<td>C8</td>
<td>220 nF/10 %/50 V (DC) X7R</td>
<td>220 nF/10 %/50 V (DC) X7R</td>
</tr>
<tr>
<td>D1</td>
<td>not mounted</td>
<td>not mounted</td>
</tr>
<tr>
<td>D2</td>
<td>not mounted</td>
<td>not mounted</td>
</tr>
<tr>
<td>D3</td>
<td>not mounted</td>
<td>BAT17</td>
</tr>
<tr>
<td>D4</td>
<td>not mounted</td>
<td>BAT17</td>
</tr>
<tr>
<td>HS1</td>
<td>heat sink FK-244-08-D-PAK Fischer</td>
<td>heat sink TO220 Redpoint thermal pad Bergquist TO220</td>
</tr>
<tr>
<td>HS2</td>
<td>heat sink FK-244-08-D-PAK Fischer</td>
<td>heat sink TO220 Redpoint thermal pad Bergquist TO220</td>
</tr>
<tr>
<td>IC1</td>
<td>TEA1795T/N1</td>
<td>TEA1795T/N1</td>
</tr>
<tr>
<td>J1</td>
<td>micro shunt pitch 2.54 mm jumper or equivalent</td>
<td>micro shunt pitch 2.54 mm jumper or equivalent</td>
</tr>
<tr>
<td>L1</td>
<td>not mounted</td>
<td>not mounted</td>
</tr>
<tr>
<td>L2</td>
<td>not mounted</td>
<td>not mounted</td>
</tr>
<tr>
<td>L3</td>
<td>not mounted</td>
<td>not mounted</td>
</tr>
<tr>
<td>L4</td>
<td>not mounted</td>
<td>not mounted</td>
</tr>
<tr>
<td>Q1</td>
<td>PSMN025-100D; NXP Semiconductors</td>
<td>PSMN4R5-40PS; NXP Semiconductors</td>
</tr>
<tr>
<td>Q2</td>
<td>PSMN025-100D; NXP Semiconductors</td>
<td>PSMN4R5-40PS; NXP Semiconductors</td>
</tr>
<tr>
<td>R1</td>
<td>3.9 kΩ/1 %/0.1 W</td>
<td>3.9 kΩ/1 %/0.1 W</td>
</tr>
<tr>
<td>R2</td>
<td>3.9 kΩ/1 %/0.1 W</td>
<td>3.9 kΩ/1 %/0.1 W</td>
</tr>
<tr>
<td>R3</td>
<td>10 Ω/1 %/0.1 W</td>
<td>10 Ω/1 %/0.1 W</td>
</tr>
</tbody>
</table>
7. Legal information

7.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

7.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors’ aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only, NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

7.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.
8. Contents

1  Introduction ................................................. 3
2  The TEA1795T ................................................. 3
3  Demo board setup ................................. 4
4  Operation .................................................. 12
  4.1  Turn-on and blanking time .................. 12
  4.2  Regulation mode and turn-off ................ 13
  4.3  Compromise between turn-on, turn-off and
       blanking times .................................. 13
  4.4  Parasitic turn-on .................................. 15
5  PCB layout .................................................. 16
  5.1  Layout considerations .......................... 16
  5.2  Copper pattern ...................................... 17
6  Bill of materials ........................................... 18
7  Legal information ........................................ 19
  7.1  Definitions ............................................. 19
  7.2  Disclaimers ............................................ 19
  7.3  Trademarks ............................................. 19
8  Contents ...................................................... 20