

UM11228

NTS0304E evaluation board OM13543

Rev. 1.0 — 11 July 2019

User manual

Document information

Information	Content
Keywords	NTS0304E, OM13543, voltage translator, level translator, level shift, passive voltage translator, passive level translator, passive level shift, I2C-bus, SMBus, SPI
Abstract	Installation guide and User Manual for the OM13543 - NTS0304E evaluation board. NTS0304E is a 4-bit, dual supply translating transceiver family with auto direction sensing, that enables bidirectional voltage level translation.



Revision history

Rev	Date	Description
v.1	20190711	Initial version

1 Introduction

NTS0304E evaluation board (OM13543) is designed to evaluate NTS0304E, which is a 4-bit, dual supply translating transceiver with auto direction sensing that enables bidirectional voltage level translation. It features eight 1-bit input-output ports (A and B), one output enable input (OE) and two supply pins (VCC(A) and CC(B)). VCC(A) can be supplied at any voltage between 0.95 V and 3.6 V. VCC(B) can be supplied at any voltage between 1.65 V and 5.5 V. This flexibility makes the device suitable for translating between any of the voltage nodes (0.95 V, 1.2 V, 1.8 V, 2.5 V, 3.3 V and 5.0 V). Pins A and OE are referenced to VCC(A) and pin B is referenced to VCC(B). A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state

[Table 1](#) lists the supported devices.

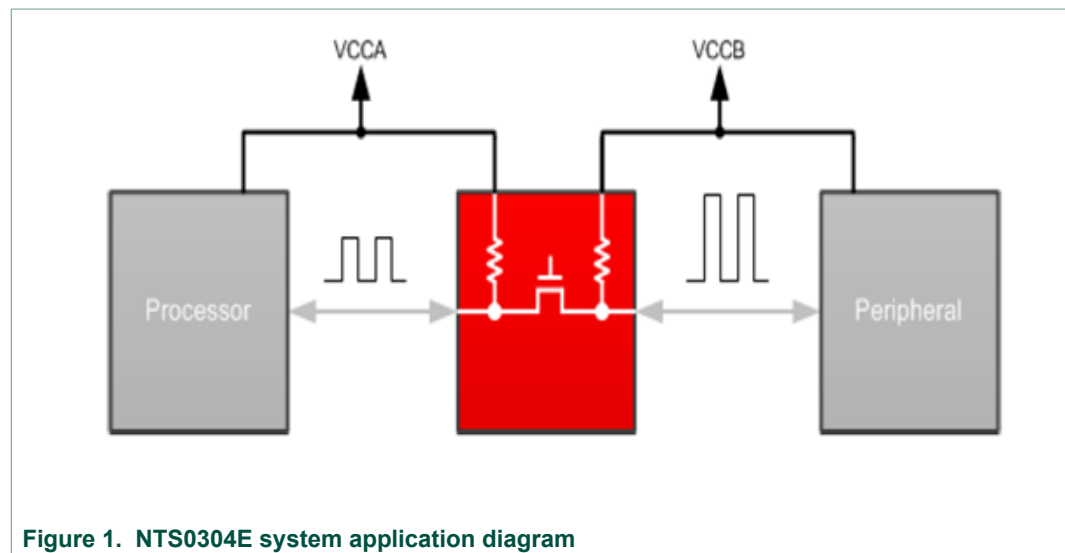
OM13543 is shipped with NTS0304EPW (TSSOP14) soldered on the board.

There are two package footprints for NTS0304E: NTS0304EUK (WLCSP12), and NTS0304EPW (TSSOP14).

Table 1. NTS0304E Package

Part Number	Package Number	Package Description
NTS0304EUK	SPT1390-10	WLCSP12
NTS0304EPW	SOT402-1	TSSOP14

Please refer to NTS0304E data sheet for more detailed information.



2 Hardware description

2.1 OM13543 board view and components placement

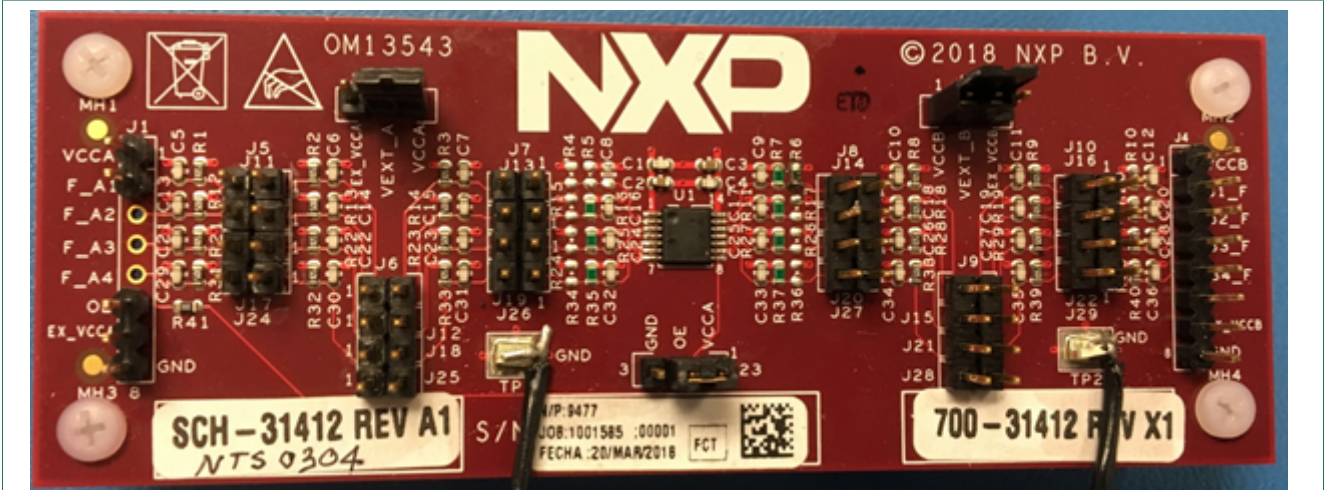


Figure 2. OM13543 board view

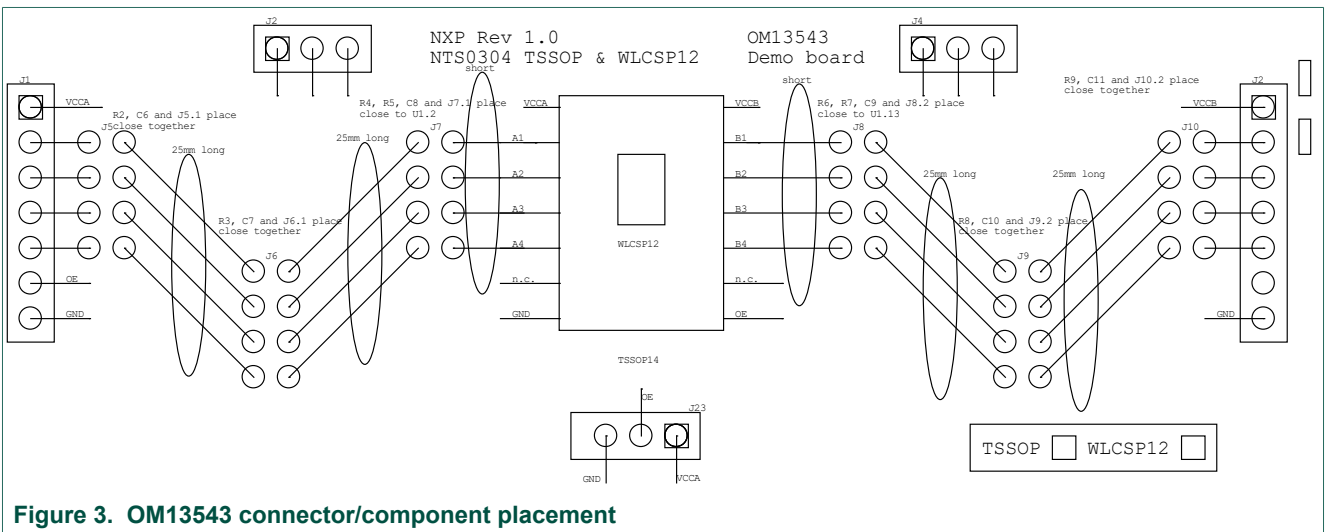


Figure 3. OM13543 connector/component placement

2.2 OM13543 board jumper location and configuration

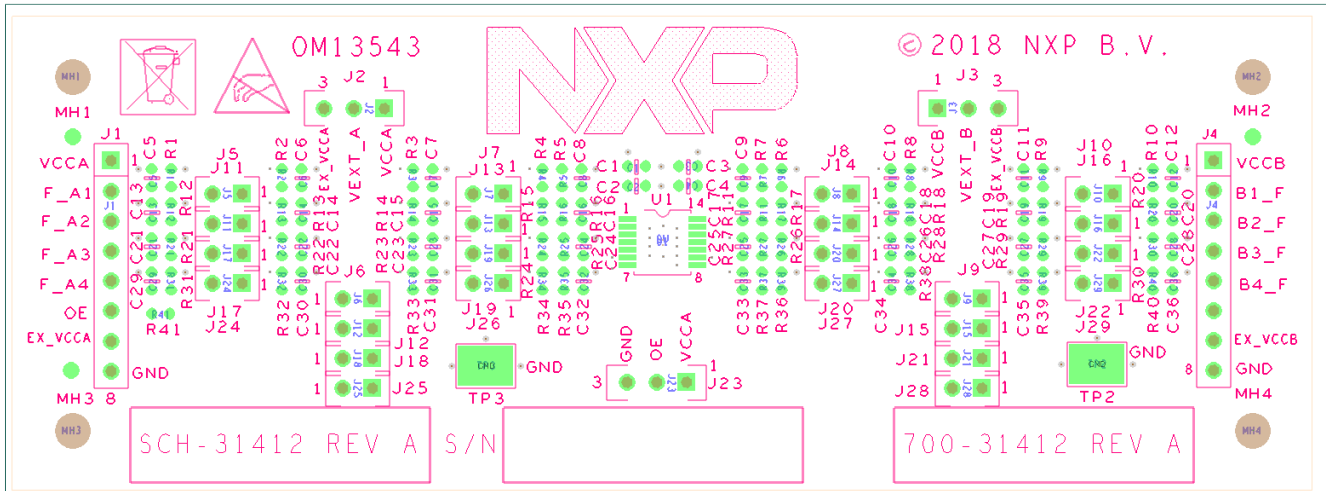


Figure 4. OM13543 board jumper location

Table 2. J1 header functions

J1 header	Function	Notes
J1-1	VCCA	Supply voltage for A port
J1-2	A1_F	Signal for A1 input or output port
J1-3	A2_F	Signal for A2 input or output port
J1-4	A3_F	Signal for A3 input or output port
J1-5	A4_F	Signal for A4 input or output port
J1-6	OE	Output enable input port
J1-7	EX-VCCA	Second supply voltage for A port
J1-8	GND	Ground

Table 3. J2 header functions

J2 header	Function	Notes
Pin 1-2 shorted (default)	VEXT_A = VCCA	Use VCCA for A port pull-up voltage
Pin 2-3 shorted	VEXT_A = EX-VCCA	Use EX-VCCA for A port pull-up voltage

Table 4. J3 header functions

J3 header	Function	Notes
Pin 1-2 shorted (default)	VEXT_B = VCCB	Use VCCB for B port pull-up voltage
Pin 2-3 shorted	VEXT_B = EX-VCCB	Use EX-VCCB for B port pull-up voltage

Table 5. J4 header functions

J4 header	Function	Notes
J4-1	VCCB	Supply voltage for B port
J4-2	B1_F	Signal for B1 input or output port
J4-3	B2_F	Signal for B2 input or output port
J4-4	B3_F	Signal for B3 input or output port
J4-5	B4_F	Signal for B4 input or output port
J4-6	NC	No connect
J4-7	EX-VCCB	Second supply voltage for B port
J4-8	GND	Ground

Table 6. J5-J29 header functions

J5-J29 header	Function	Notes
J5-J7	A->B B->A	J5-J7 are used to select pull-up resistors for A1 port J5-J7 are used to select load capacitors for A1 port
J8-J10	A->B B->A	J8-J10 are used to select load capacitors for B1 port J8-J10 are used to select pull-up resistors for B1 port
J11-J13	A->B B->A	J11-J13 are used to select pull-up resistors for A2 port J11-J13 are used to select load capacitors for A2 port
J14-J16	A->B B->A	J14-J16 are used to select load capacitors for B2 port J14-J16 are used to select pull-up resistors for B2 port
J17-J19	A->B B->A	J17-J19 are used to select pull-up resistors for A3 port J17-J19 are used to select load capacitors for A3 port
J20-J22	A->B B->A	J20-J22 are used to select load capacitors for B3 port J20-J22 are used to select pull-up resistors for B3 port
J24-26	A->B B->A	J24-J26 are used to select pull-up resistors for A4 port J24-J26 are used to select load capacitors for A4 port
J27-J29	A->B B->A	J27-J29 are used to select load capacitors for B4 port J27-J29 are used to select pull-up resistors for B4 port

Table 7. J23 header functions

J23 header	Function	Notes
Open	OE = J-6	OE is controlled by J1-6
Pin 1-2 shorted (default)	OE = VCCA	Output port is enabled
Pin 2-3 shorted	OE = GND	Output port is disabled

3 Test Setup

3.1 A -> B test setup

1. Provide power supply to (0.9V-3.6V) to NTS0304E VCCA pin through J1 (J1-1 or J1-7) and J2.
2. Provide power supply to (1.6V-5.5V) to NTS0304E VCCB pin through J4 (J4-1 or J4-7) and J3.
3. Set J23 pin 1-2 shorted to enable output port
4. Use J5-J7 to select pull-up resistors for A1 port.
 - Connect signal A1_F to J1-2 (A1_F) and short J5-J7, A1 port has R1-R3 pull-up resistors in parallel, or
 - Connect signal A1_F to J5-1 and short J6-J7, A1port has R2/R3 pull-up resistors in parallel, or
 - Connect signal A1_F to J6-1 and short J7, A1port has R3 pull-up resistors, or
 - Connect signal A1_F to J7-1, A1port has no pull-up resistor.
5. Use J8-J10 to select load capacitors for B1 port.
 - Connect signal B1_F to J4-2 (B1_F) and short J8-J10, B1 port has C9-12 load capacitors in parallel, or
 - Connect signal B1_F to J10-2 and short J8-J9, B1 port has C9-11 load capacitors in parallel, or
 - Connect signal B1_F to J9-2 and short J8, B1 port has C9-10 load capacitors in parallel, or
 - Connect signal A1_F to J8-2, B1 port has C9 load capacitor.
6. Use J11-J13 for signal A2_F pull-up resistors selection.
7. Use J14-J16 for signal B2_F load capacitors selection.
8. Use J17-J19 for signal A3_F pull-up resistors selection.
9. Use J20-J22 for signal B3_F load capacitors selection.
10. Use J24-J26 for signal A4_F pull-up resistors selection.
11. Use J27-J29 for signal B4_F load capacitors selection.
12. Input signals to A1_F-A4_F ports and receive level translating signals from B1_F-B4_F ports.

3.2 B -> A test setup

1. Provide power supply to (0.9V-3.6V) to NTS0304E VCCA pin through J1 (J1-1 or J1-7) and J2.
2. Provide power supply to (1.6V-5.5V) to NTS0304E VCCB pin through J4 (J4-1 or J4-7) and J3.
3. Set J23 pin 1-2 shorted to enable output port
4. Use J8-10 to select pull-up resistors for B1 port.
 - Connect signal B1_F to J4-2 (B1_F) and short J8-J10, B1 port has R8-R10 pull-up resistors in parallel, or
 - Connect signal B1_F to J10-2 and short J8-J9, B1 port has R8-R9 pull-up resistors in parallel, or
 - Connect signal B1_F to J9-2 and short J8, B1 port has R8 pull-up resistors, or
 - Connect signal B1_F to J8-2, B1 port has no pull-up resistor.
5. Use J5-J7 to select load capacitors for A1 port.

- Connect signal A1_F to J1-2 (A1_F) and short J5-J7, A1 port has C5-8 load capacitors in parallel, or
 - Connect signal A1_F to J5-1 and short J6-J7, A1 port has C6-8 load capacitors in parallel, or
 - Connect signal A1_F to J6-1 and short J7, A1 port has C7-8 load capacitors in parallel, or
 - Connect signal A1_F to J7-1, A1 port has C8 load capacitor.
6. Use J14-J16 for signal B2_F pull-up resistors selection.
 7. Use J11-J13 for signal A2_F load capacitors selection.
 8. Use J20-J22 for signal B3_F pull-up resistors selection.
 9. Use J17-J19 for signal A3_F load capacitors selection.
 10. Use J27-J29 for signal B4_F pull-up resistors selection.
 11. Use J24-J26 for signal A4_F load capacitors selection.
 12. Input signals to B1_F-B4_F ports and receive level translating signals from A1_F-A4_F ports.

4 Schematic

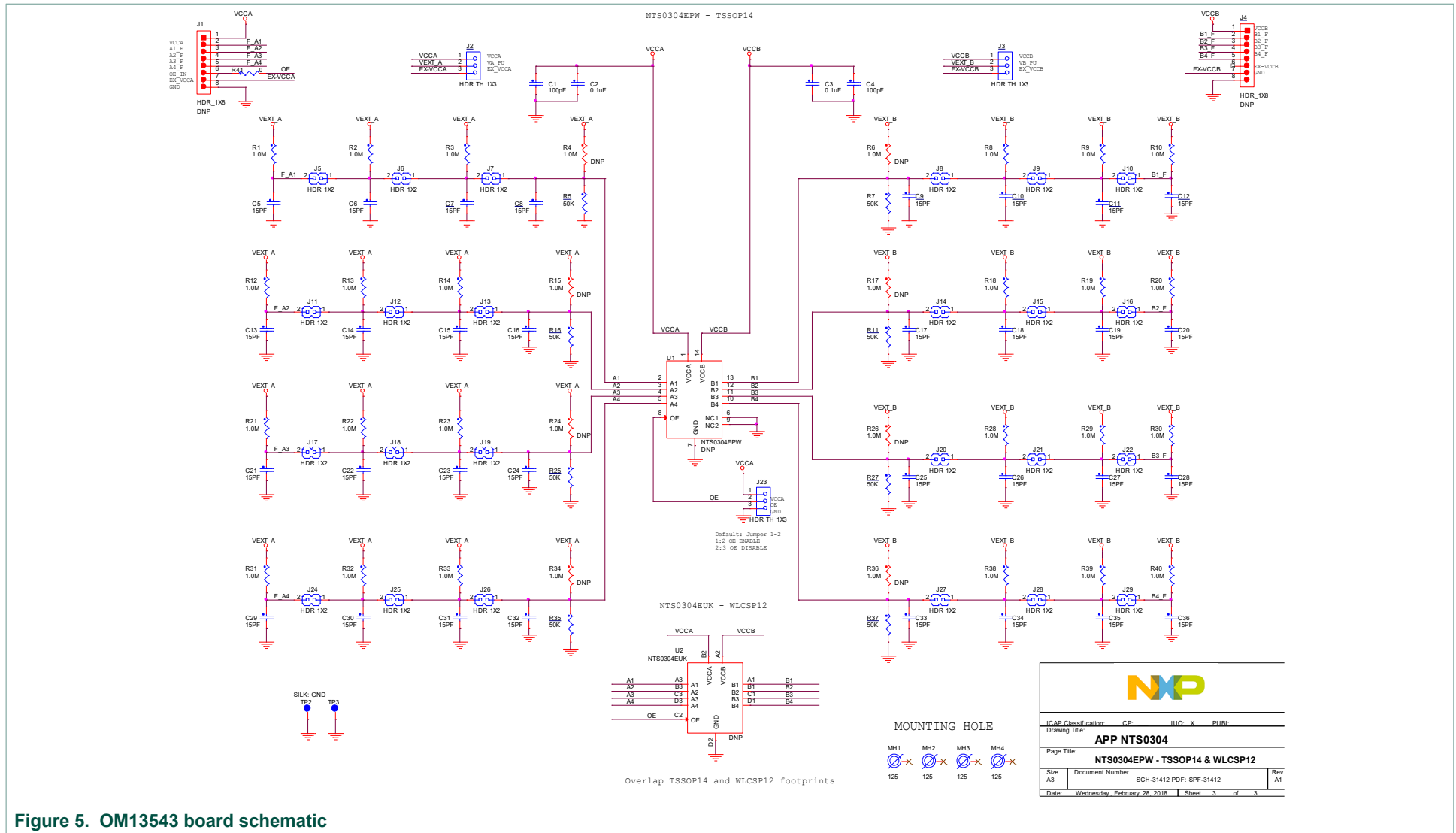


Figure 5. OM13543 board schematic

5 Notes

6 Legal information

6.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

6.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and

products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer. In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out of the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages. Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US\$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

6.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Tables

Tab. 1.	NTS0304E Package	3	Tab. 5.	J4 header functions	6
Tab. 2.	J1 header functions	5	Tab. 6.	J5-J29 header functions	6
Tab. 3.	J2 header functions	5	Tab. 7.	J23 header functions	6
Tab. 4.	J3 header functions	5			

Figures

Fig. 1.	NTS0304E system application diagram	3	Fig. 4.	OM13543 board jumper location	5
Fig. 2.	OM13543 board view	4	Fig. 5.	OM13543 board schematic	9
Fig. 3.	OM13543 connector/component placement	4			

Contents

1	Introduction	3
2	Hardware description	4
2.1	OM13543 board view and components placement	4
2.2	OM13543 board jumper location and configuration	5
3	Test Setup	7
3.1	A -> B test setup	7
3.2	B -> A test setup	7
4	Schematic	9
5	Notes	10
6	Legal information	11

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2019.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 11 July 2019
Document identifier: UM11228