Novel Devices to Overcome Planar Limits and Enable Novel Circuits

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OVERVIEW

Planar CMOS technology has revolutionized the electronics industry over the last few decades. Rapid and predictable miniaturization was predicted by Moore's law; this has allowed the semiconductor industry to make new products with added functions with each new generation of technology. Most commercial products are now in the 90nm technology node as defined by ITRS [Ref 2], with work on 65nm and 45nm nodes progressing rapidly. This predictable scaling is now reaching its limit [Ref 1] and has forced the industry to look to novel device architectures beyond the 45 nm technology node.

In all these years of digital CMOS innovation and scaling, we have only scratched the surface of the semiconductor substrate. The Planar CMOS device—the workhorse of digital applications used in modern electronic systems—have a channel only on the surface of the silicon. These devices have a single gate on the surface of the silicon to modulate the channel on the surface of the semiconductor. Scaling of these planar devices has now begun to hit its limits for power, noise, reliability, parasitic capacitances and resistance. New device architectures using multiple sides of the semiconductor—not just the planar surface—offer a path to overcome these performance limits. In addition, these non-planar CMOS devices enable new circuits previously not possible with single gate CMOS devices. [Ref 4-6]

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A Better Switch

The fundamental function of a transistor in a digital system is to be a switch: to conduct as much current as possible when on, and to shut down when off. The limits of planar CMOS technologies make this fundamental operation impractical as gate lengths and supply voltages are scaled down. The current in the on state is reduced when device sizes are scaled down, due to reduced mobility of the electrons and parasitic resistances (among other effects). The leakage current increases when the device is turned off; this substantially higher leakage can drain batteries quickly, making many mobile applications difficult to engineer (Figure 1.a).

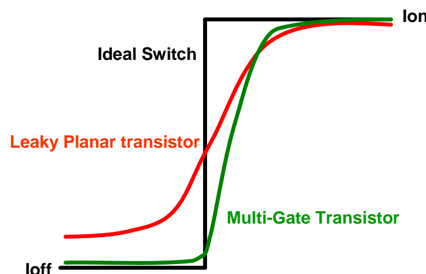


Figure 1a: Ideal switch vs. a good switch and leaky switch

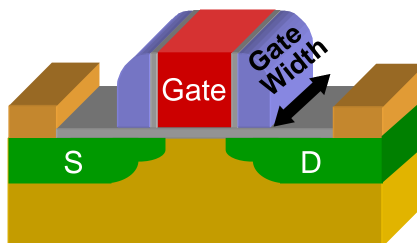


Figure 1b: The planar MOSFET, gate is only on surface

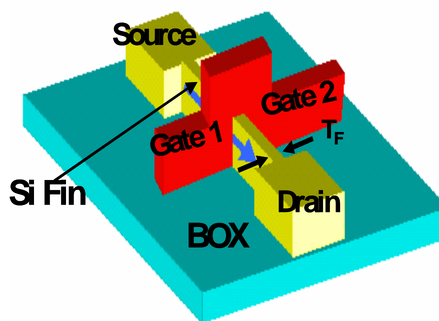


Figure 1c: Multi-gate FinFET gate controls many sides

The fundamental limiting factors to scaling a single gate planar CMOS transistor are the leakage through the gate, and the effect of the drain taking control of the channel making it difficult to control the switch using the gate (Figure 1b); this is known as short channel effects. In a multi-gate device, the channel of the device is controlled (gated) by gates from multiple sides and the body of the device where the channel is formed is made ultra-thin, so the gate bias controls the channels more efficiently from multiple sides (Figure 1c).

Changes and Solutions

While individual transistor structures that behave as better switches than the existing planar transistors have been demonstrated, manufacturing a complete product using these devices still has many challenges. The challenges include process technologies, design methodologies and new compact models to represent these devices.

These multi-gate devices such as the planar MOSFET still have a single gate electrode, but this single gate electrode wraps around many sides and controls the channel from multiple sides. These have various names, such as Mesa Isolated FET, DELTAFET, FINFET, TriGATE, MuGFET etc. In all these devices, a single gate electrode controls the channel from multiple sides yielding better control of the device and lower leakage when its shutdown and conducts more current when turned on. A version of these devices with the gates separated and Independently controlling the channel is called the MIGFET (Multiple Independent Gate FET) and the novel circuits feasible with this device is discussed later in this paper [Ref. 7-9].

Process Technologies

The multi-gate device architecture requires two basic technologies that are substantially new compared to existing processes:

- A process technology to make very thin silicon body of the order of 20nm
- A process to fabricate identical gates on at least two sides of this very thin silicon

Various process technologies have been proposed to fabricate such a structure (Figure 2). While many process have been identified to make a very thin silicon channel, a process that easily allows gates on both sides of this channel that are aligned to each other has been provided only on the structure now called FinFET, TriGate etc. Currently most research efforts to make multi-gate devices involve these FinFET device structures. While devices with sub-20 nm silicon body and gates less than 40 nm have been demonstrated, there are still manufacturing challenges to make a product with millions of such transistors [Ref. 10-14].

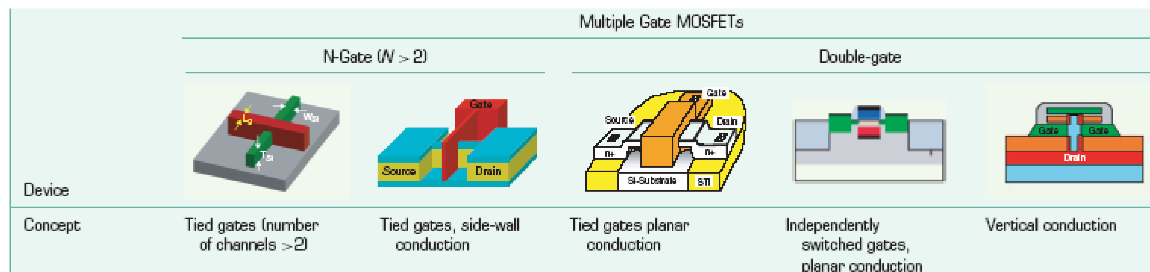


Figure 2. Multiple gate MOSFETs

Currently, the challenge to fabricate very thin silicon body is met by process optimizations such as trimming the silicon and using non-conventional masking procedures and dimensions as low as 10 nm which have already been demonstrated [Ref 3]. The other challenge is to pattern gates over tall topography. Once again, process changes and optimizations have been successfully used to demonstrate these gates over very large areas, as in the SRAM memory area shown in Figure 4b. While these novel devices make progress, new materials such as new gate materials are also researched. Incorporating these new materials is crucial to gain the maximum benefits out of these novel structures. The use of metal gates instead of conventional poysilicon gates will allow less parasitic resistance and poly depletion effects. Patterning these metal gates on FinFETs with traditional oxides is a challenge, but they have been demonstrated with new process techniques (Figure 3).

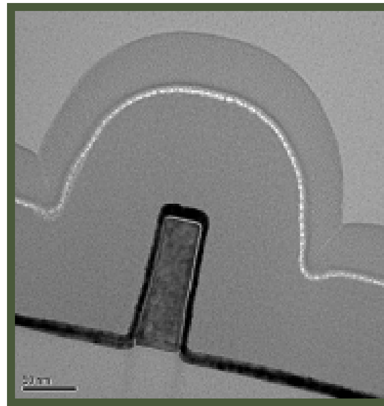


Figure 3a. A TEM cross section of a FinFET with metal gate

Figure 3b. A SEM 3D view of the FinFET device

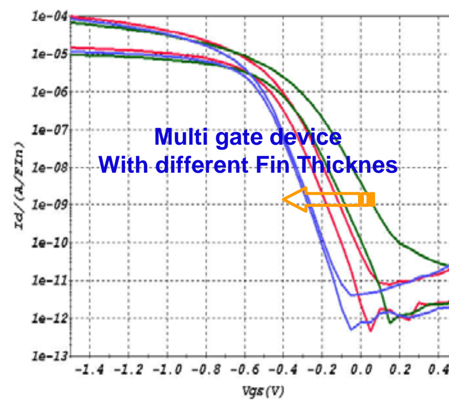


Figure 3c. Characteristics of a metal gate electrode PMOS FinFET

Design

We have seen that a switch in the multi-gate devices offers far better performance, but to be part of a product, these devices must be designed into them. There is substantial investment in existing designs. Any new technology should be able to seamlessly convert or use the existing design infrastructure. All multi-gate device technologies need some level of re-design to optimize the products and to incorporate new process conditions. Vertical devices such as FinFET can be modified using existing design tools by

converting one or more design layers. An Inverter using 90 nm SOI design converted using an automated tool is featured in Figure 4a. The silicon fabricated using such silicon is shown in Figure 5b. These design conversion methodologies need to become part of standard electronic design automation (EDA) tools to make these technologies mainstream.

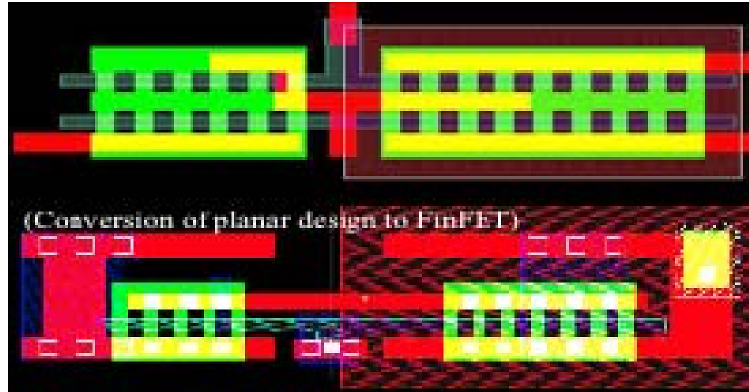


Figure 4a. A planar logic gate converted to a FinFET layout. Tools to convert and generate these devices are needed.

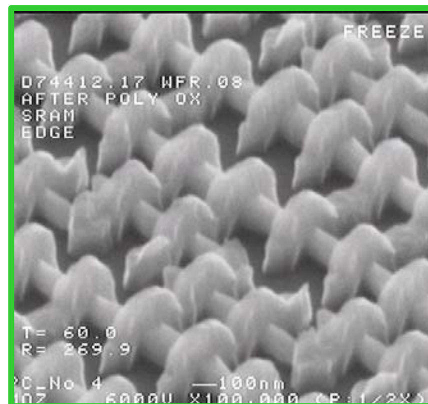
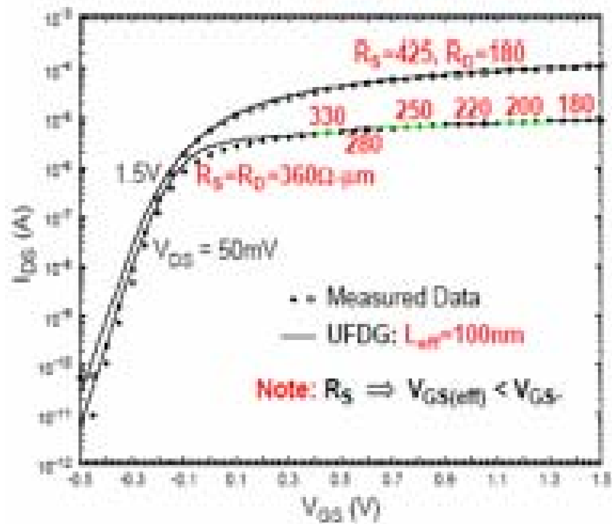


Figure 4b. An array of SRAM cells patterned over 100 nm topography

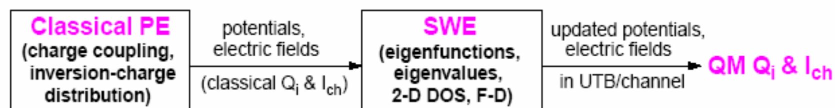
Compact Models

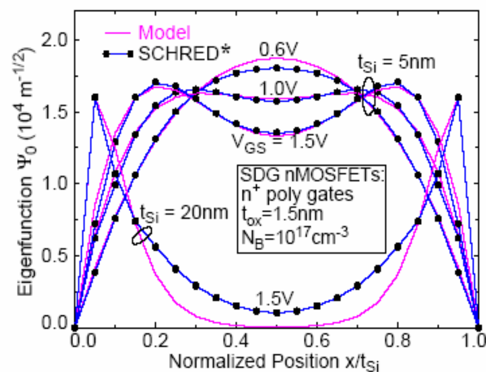
The multi-gate devices that control the channel from multiple sides and very thin body devices are new to circuit and system designers. These devices need to be modeled to understand and predict the physics and functionality of the circuits. Compact computer models are used in circuit design. Designing semiconductor devices using simulators such as SPICE models are just beginning to be developed for use in these simulators. New compact models that accurately model these novel devices, and are computationally efficient, are in development. There are new physical characteristics that now need to be incorporated into these device models.

The University of Florida Double Gate Model (UFDG) is one of the earliest models to address this need. The model incorporates the physics of quantum-mechanical effects that are inherent in very thin body devices. Other effects such as resistance modulation with bias, parasitic effects and the use of multiple independent gates are all incorporated in this model. Compact models such as UFDG allow circuit and system designers to model the systems, study the tradeoff of new devices in the systems and also invent the new circuits that are feasible due to these new device structures [Ref 15].



UFDG is actually a Compact Poisson-Schrödinger Solver:





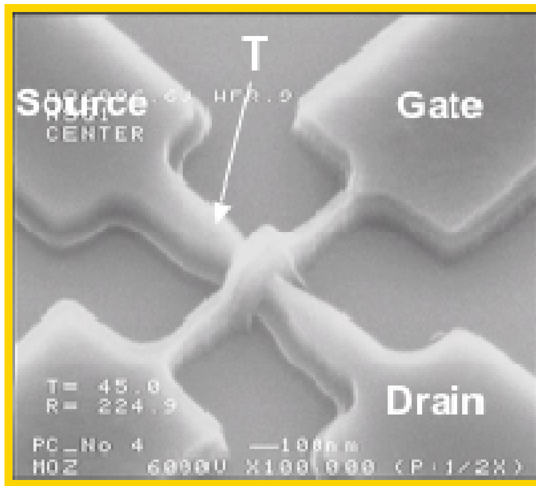
1-D SWE analytical solution is derived using a variational approach, then coupled to PE and $Q_i(V_{Gfs}, V_{Gbs})$ via Newton-Raphson iteration, all with dependence on t_{Si} and Si orientation, as well as E_x.

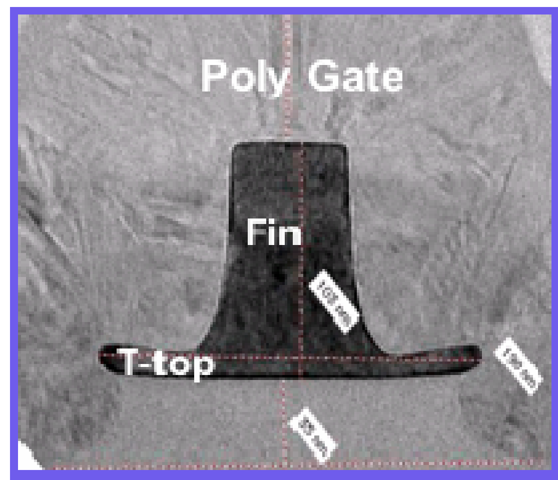
The QM modeling is also the basis for a physical mobility model for the UTB carrier transport.

Figures 5a and 5b: Compact models for double-gate devices need to consider new effects due to the second gate, very thin silicon body. UFDG is a physics based model used for prediction and new designs.

This Is "IT"

Multigate device architectures are rapidly evolving. The FinFET, with all its advantages, still has a significant drawback: the region between the fins is not used as part of the switch. A new family of devices called ITFET that uses both the vertical and horizontal regions of silicon has been proposed and demonstrated for the first time. The ITFET has both vertical and horizontal thin body regions shaped like an "inverted T". The ITFET offers maximum surface area utilization on the wafer for the channel and allows optimization of crucial circuit elements such as the SRAM-based cache that is ubiquitous in all modern digital CMOS products [Ref 16, 17].





Figures 6a and 6b. The ITFET has a channel that is shaped like an "inverted T". This structure provides the advantages of both planar and vertical thin body device.

Multiple Independent Gate FET (MIGFET)

In a MIGFET, multiple gate electrodes control a thin silicon channel using multiple gate electrodes that are separated from each other (Figures 8, 9). This class of devices allows new circuits and applications that were previously impractical or impossible in planar CMOS applications which have only one gate on the surface. Many new applications have been proposed and demonstrated using these devices, including MIGFET-based 4T/6TSRAM, MIGFET RF Mixer, MIGFET FPGA and MIGFET 1T Dynamic Memory [Ref 9].

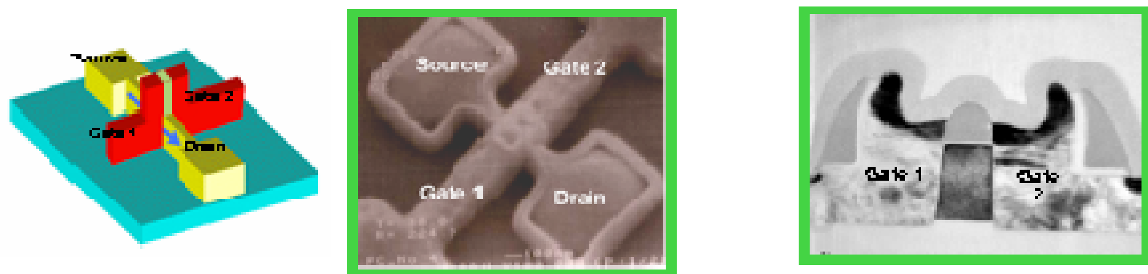


Figure 8a. The MIGFET has independent gates on either side of a thin channel.
A schematic, SEM view and TEM cross section through it are shown.

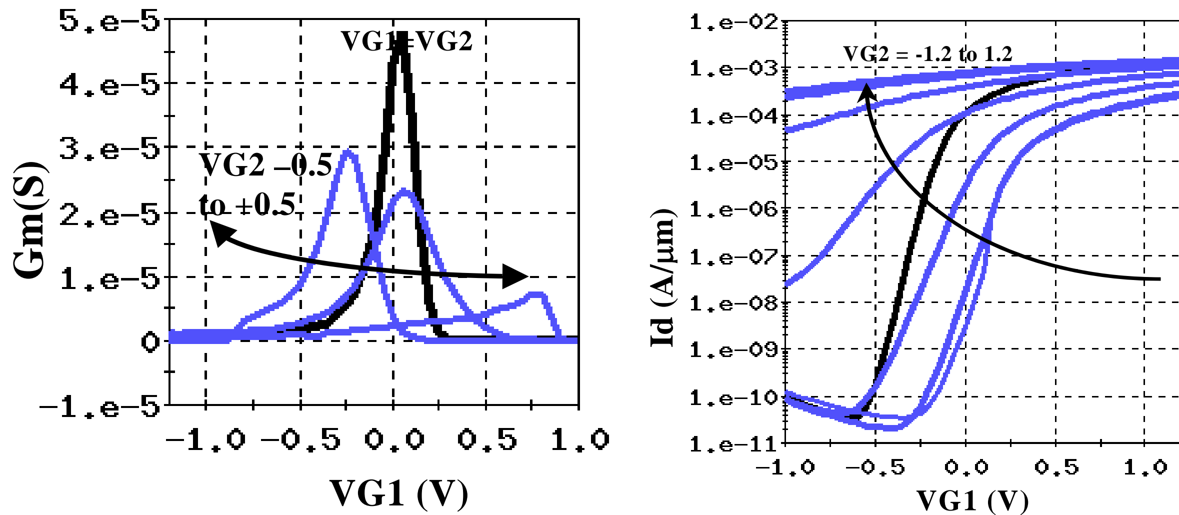


Figure 8b. MIGFET with two independent gates. Both gates modulates the device performance separately. Normal transistors have one gate and only one of these characteristics (shown in black) is possible.

New Logic Circuits with a Better Switch

Traditional digital CMOS has operated between ON and OFF states, as explained in Figure 1. The excellent Ion and Ioff characteristics of the multi-gate devices allow future scaling of traditional circuits for a few generations. Even this is not sufficient for certain low-power applications such as pacemakers, hearing aids and other self-powered logic devices. While subthreshold logic has been proposed as a low-power circuit alternative, it has not been widely used, due in part to the limitations of single gate devices. Multi-gate devices, with their steep turn on characteristics and extremely low leakage characteristics, promise to be ideal to make these systems practical [Ref 18].

New Analog Circuits Can Use Multiple Independent Gates

RF Applications

While digital CMOS logic leads the process technology roadmap for computing applications, the communications applications have a substantial mix of analog components that are integrated into the CMOS logic or as standalone products. The double gate device architecture allows better scaling of these analog applications and new functions that were not possible with single gate transistors. Just as in CMOS logic, the fundamental switch is improved by the double gate architecture for analog applications. The double gate architecture offers better gain and can be used as a better mixer, amplifier or VCO.

RF Mixers

Wireless systems typically consist of multiple mixers to convert frequencies. The mixer is a very crucial analog component used for frequency conversion. Typically these mixers are integrated with the CMOS logic when possible, but it is difficult to scale and match the analog devices. These devices are often forced off-chip, increasing cost and complexity. The MultiGate transistor with independent gates—the MIGFET—has been studied for mixer operations and promises to be an excellent device to allow analog scaling as digital devices continue to scale.

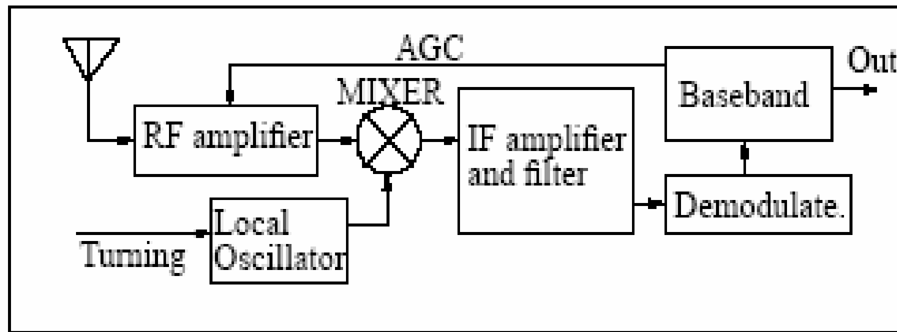


Figure 9. Wireless systems use various analog components that can be enhanced by multi-gate devices. The transceiver shown has mixer which currently use multiple transistors and can be replaced by MIGFET.

The MIGFET has a unique feature: two independent gates modulating the channel. These gates allow new modes of operation such as an RF mixer. In this operation, the RF and LO signals used in the mixer are fed to the two gates and the corresponding mixed output is obtained. This has been demonstrated, and simulation of such new circuits suggest that these devices have substantial gains up to 100 GHz. This will substantially improve future wireless performance and reduce power consumption [19, 20].

Novel implementation of a simple MIGFET mixer has been simulated, and its double-balanced counterpart has been simulated using the double gate compact model UFDG. For the former, a small RF signal and a large LO signal applied to the two gates of a single MIGFET yield mixing via the charge coupling between the gates. Good design of the mixer in terms of good conversion gain and linearity, while still satisfying small size/low-voltage/low-power requirements for specific applications, can be achieved with optimal biases of the two gates and good transistor design. The double-balanced mixer uses four MIGFETs, and generally offers better conversion gain, linearity and superb port isolation with the compromise of larger power consumption and area [Ref. 6].

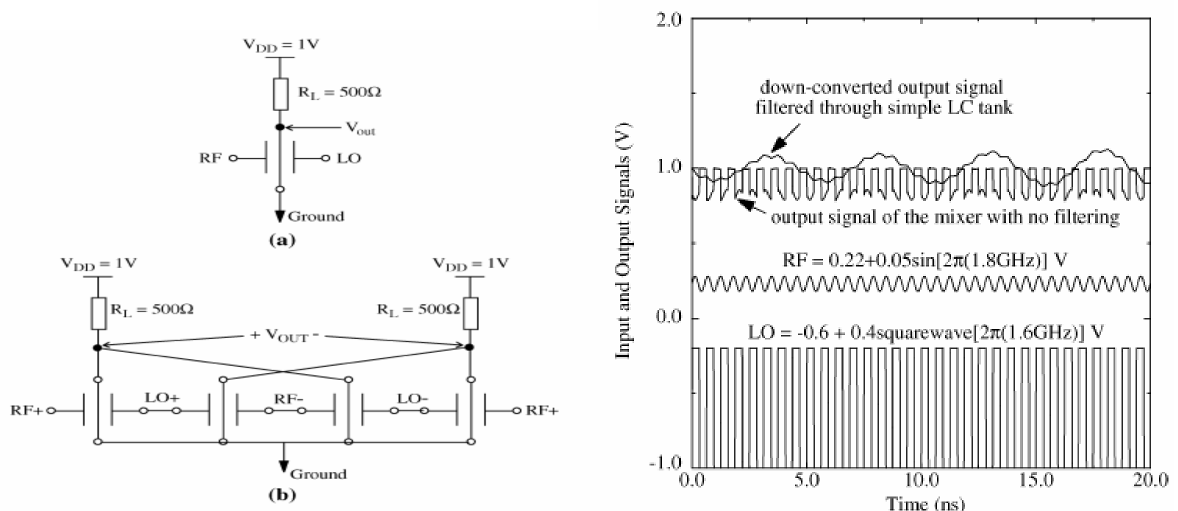


Figure 7. Mixer schematics: (a) mixer using one MIGFET; (b) double-balanced mixer using four MIGFETs. Note that RF+/RF- and LO+/LO- are antiphase signals.

New Memory Circuits

A substantial part of any system now is memory. Typically, high-performance logic uses SRAM. Large data files are saved in non-volatile memory (NVM) or dynamic RAM. All three memory types can be improved using these devices in novel configurations that were not practical in single gate planar technologies.

SRAM with Dynamic Feedback

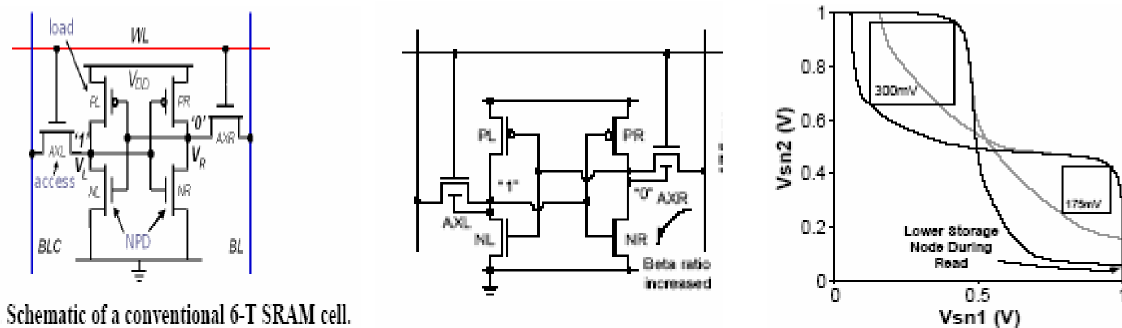


Figure 10. The 6T SRAM cell can be substantially improved with MIGFET feedback

Intrinsic variations and challenging leakage control in today's planar Si MOSFETs limit the scaling of SRAM. The 6-T and 4-T FinFET-based SRAM cells designed with built-in feedback achieve significant improvements in the cell static noise margin (SNM) without area penalty. Up to 2x improvement in SNM can be achieved in 6-T FinFET-based SRAM cells. A 4-T FinFET-based SRAM cell with built-in feedback can achieve sub-100 pA per-cell standby current and offer similar improvements in SNM as the 6-T cell with feedback, making them attractive for low-power, low-voltage applications [Ref 4]. 1T ZRAM- High Density Integrated Dynamic RAM

The DRAM is one of the densest devices in the semiconductor industry. Current dynamic RAM processes are so different from planar CMOS technologies that it is usually not cost-effective to integrate these DRAMs with CMOS. The MIGFET device has some floating body characteristics that enable it to be used as a one-transistor (1T) RAM called ZRAM. These 1T ZRAM devices are possible because of the unique features in vertical MIGFET devices such as the additional independent gate electrode. And since the device is essentially a transistor, but can be operated as a RAM, it could be integrated with similar CMOS logic devices in products that can take advantage of large on-chip storage [Ref 5].

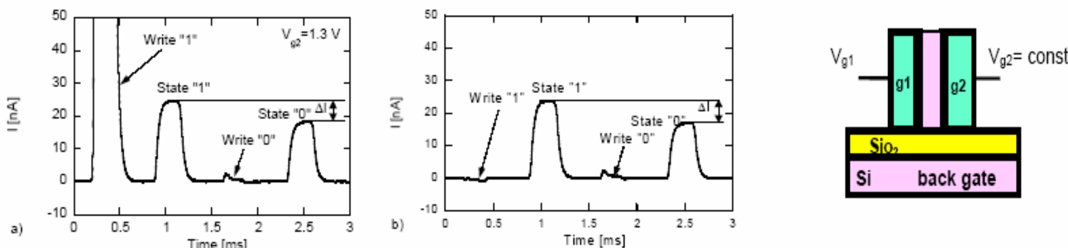


Figure 4. Source current time dependencies measured in the first operation mode. State "1" is written with the impact ionization mechanism (a) and with band to band tunneling (b).

Figure 2. First operation mode: gate 2 is used to form the floating body storage node.

Figure 11. The MIGFET device used as a DRAM the channel between the two gates can be held floating to store data using the first gate and read using the second independent gate.

Multi-Gate Flash

Non-volatile memory devices have now become widely used in automotive, communication and multimedia products. The non-volatile nature of these memories makes them very attractive in such applications. Multi-gate devices allow further shrinking of these memory devices. The sidewalls of the multi-gate transistor can have charge storage layers such as silicon nitride or silicon nanocrystals. The performance of conventional charge storage layers such as poly can also be enhanced, since they can now be formed on both sides of these vertical devices. In combination with the multiple gate option, these devices can store multiple bits in a single transistor, increasing density and performance [Ref 21].

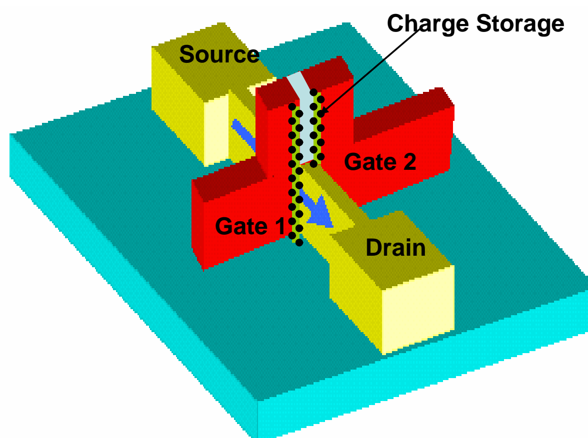


Figure 12. The MIGFET Flash device has storage elements under both gates and can store multiple bits in each device

Looking Ahead

With CMOS scaling reaching various limits, multi-gate devices offer an alternative path to increase the functions/unit silicon by providing better transistors for existing circuits and making new applications feasible using the novel features made possible by these devices. An ideal product would integrate these advantages. A hypothetical product that takes advantage of most of the devices discussed here would:

- Include single-gate electrode multi-gate devices to reduce leakage and improve switching performance
- Use the ITFET and 6T SRAM with feedback for high performance static memory
- Include a large on chip 1-T ZRAM and embedded multi-bit multi-gate flash memory

The analog and I/O subsystems will take advantage of the better gain and noise immunity of the multi-gate architecture in some circuits and novel circuits such as balanced MIGFET mixer.

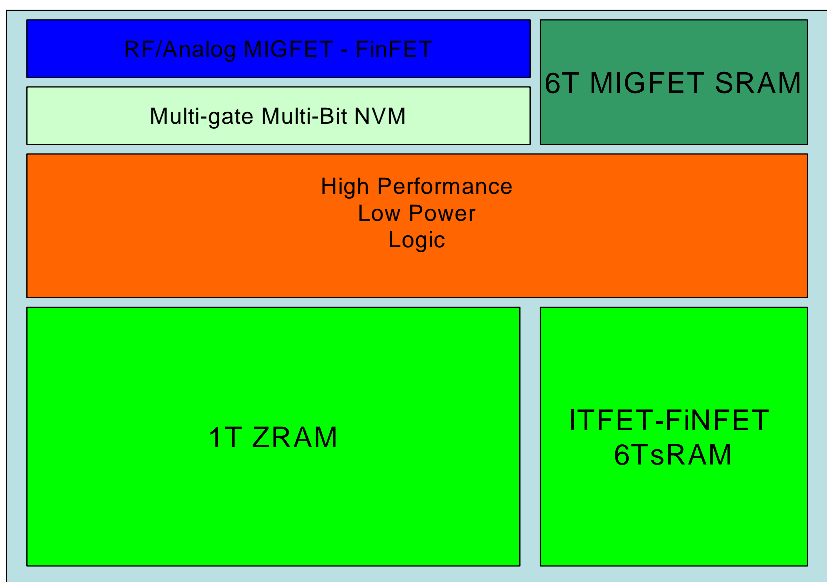


Figure 13. Multi-gate devices can be used to improve all device functions: logic/memory/analog

Summary

Rapid and predictable scaling of planar CMOS devices is becoming difficult. New device structures to replace planar CMOS devices are being researched. Multi-gate devices using multiple surfaces are promising continued scaling, and could even make new circuits feasible. These devices can provide new and better characteristics across all logic, memory and analog device function. The challenges in making these devices to enter mainstream products are many. However, rapid strides in process, design and modeling in the last few years has delivered substantial progress.

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