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Integrated Circuits for Implantable Medical Devices

Authors

James McDonald: Co-founder and president of Cactus Semiconductor, a fabless semiconductor firm that specializes in custom medical integrated circuits including ASICs used in implantable applications

Steven Dean: Global medical market lead for Freescale

David Niewolny: Medical segment manager with Freescale's Microcontroller Solutions Group

Donnie Garcia: Systems engineer with Freescale's Microcontroller Solutions Group

Navjot Chhabra: Manager, redistributed chip packaging operations, research and development. Freescale Packaging Solutions Development

Loris Chang: Biomedical engineering student at the University of Texas at Austin

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This white paper describes the electronic features of implantable circuits and the integration of these features into silicon

1 Introduction

Implantable medical devices have been around for decades. Early on, most of the established applications for medical devices focused on cardiac rhythm management. Such devices were used to treat irregular heart rhythms, such as bradycardia (beating too slow) or tachycardia (beating too fast).

Alternatively, today's implantable circuits provide therapy to treat numerous conditions. Exciting new applications in neurological stimulation can be used to treat sleep apnea, pain management, Parkinson's Disease, epilepsy, bladder control, gastrointestinal disorders, numerous autoimmune diseases and psychological disorders such as obsessive compulsive disorder (OCD). Implantable systems can now provide precise dosage and interval delivery of drugs to more effectively treat patient's conditions while minimizing side effects.

With the ever increasing clinical need for implantable devices comes the continuous flow of technical challenges. As with commercial portable products, implantable devices share the same need to reduce size, weight and power (SWaP). Thus, the need for device integration becomes imperative. There are many challenges when creating an implantable medical device. While this white paper focuses on the key electronic features of implantable circuits and the integration of these features into silicon, it will cover how Freescale and Cactus Semiconductor together can provide solutions that meet different aspects of the design. Freescale drives innovation and enables medical devices with their latest technology for microcontrollers, sensors, analog and wireless products. The white paper will also explore the different ways a design can be partitioned as well as the trade-offs associated with those design choices. Finally, the white paper will briefly cover the key attributes required in the silicon technology used for implementing implantable integrated circuit (IC) designs.

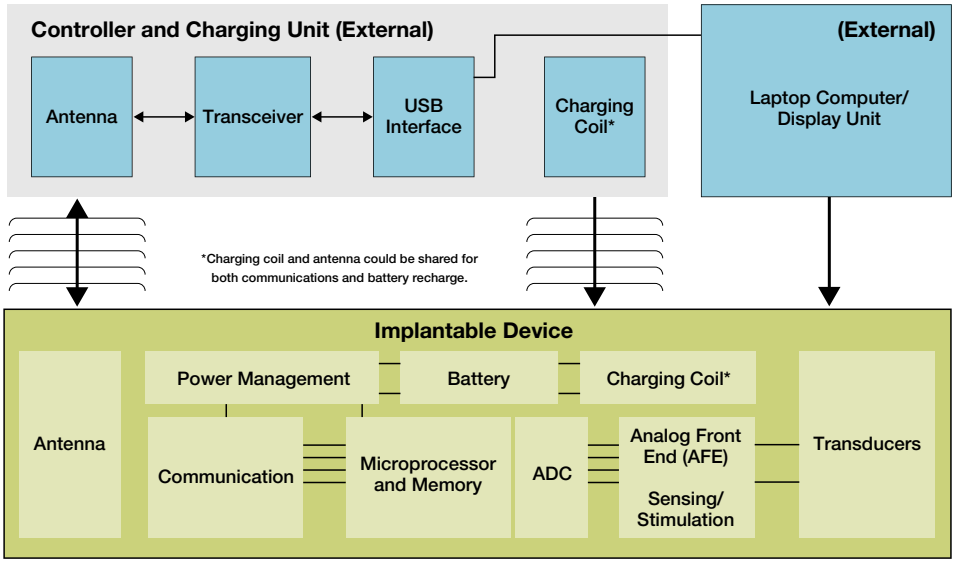
2 Common Functions for Implantable Integrated Circuits

A vast majority of the integrated circuits supporting the implantable device can be divided into the following sections:

1. Analog Front End
    a. Sensing
    b. Stimulation (or Delivery)
2. Memory Storage
3. Microprocessor (CPU)
4. Communications
5. Power Management

We will now look briefly at each of these sections to provide a baseline understanding of the hardware requirements and the associated technology requirements to support these functions. Figure 1 depicts a diagram of a generic implantable device with the five main functional sections outlined above.

Figure 1: Implantable Device with External Controller



The sensing and stimulation sections of an implantable IC can be referred to collectively as the **analog front end** (AFE). The AFE's unique requirements are often responsible for many IC technology challenges. These analog interfaces often require high voltages for sensing or for delivering the required therapy. In the digital world, IC technology continues to shrink in size, with smaller geometries that inherently cannot tolerate the higher voltages required for these applications. In addition, the pure digital technologies focus solely on digital density and low cost. These digital "centric" technologies may not provide the devices necessary to support the ultra low power and precision requirements for implantable devices. Design partitioning and implantable IC technology will be covered in section 3 of the paper.

The **sensing** function allows a medical device to determine what action to take and/or what therapy to deliver. There is a need and requirement to integrate more sensing devices, such as accelerometers and pressure sensors for medical implantables (such as catheters). Examples of sensing in an implantable application would be detecting heart rhythm irregularities, or sensing the amount of glucose in the bloodstream. Various types of sensors exist, such as pressure, magnetic, inertial, touch, optical, temperature, voltage and current sensors. Freescale's MMA8451Q device, part of the Xtrinsic family of smart sensors, is a low-power, three-axis, capacitive micromachined accelerometer with 14 bits of resolution. The device can be configured to generate inertial wake-up interrupt signals from any combination of the configurable embedded functions, allowing the MMA8451Q to monitor events and remain in a low power mode during periods of inactivity.

Many sensors are developed using micro-electromechanical systems (MEMS) technology. MEMS-based sensors are a class of devices that build very small electrical and mechanical components on a single chip. In addition to accelerometers, Freescale's Xtrinsic portfolio contains several types of sensing devices, including magnetic, pressure, and touch sensors as well as intelligent sensing platforms.

Another important feature of the sensing function is monitoring. The sensor can be used to collect data continuously over a period of time to determine the effectiveness of the therapy being delivered. The data collected can be used to modify treatment as necessary.

Stimulation, or therapy delivery, will be defined as the output or response of the implanted device. In many cases the response is based on the sensing of the condition being monitored, such as heart rate or glucose levels in the blood. However, some implantable devices run in "open loop" where the device is programmed in the doctor's office to deliver a specific therapy. Once the device is turned on, the device delivers the programmed therapy with no real-time closed loop feedback.

Implantable devices have become increasingly used for neurological stimulation. Neurological stimulation consists of generating current and/or voltage pulses that provide stimulation to a particular nerve. The implantable device is then called upon to generate and control several pulse parameters, such as pulse frequency, duration, amplitude and ramp rate.

Freescale's portfolio of MCUs includes digital to analog converters and digital pins which can be used to create stimulation by controlling voltage and/or currents. Freescale's DAC blocks can support conversion times as low as 1 µs and contain a 16-word FIFO that allows a generation of complex waveforms without CPU intervention.

Memory storage is essential for an implantable device. Memory for the integrated circuit comes in two main forms, volatile and non-volatile. Volatile memory, such as RAM, does not retain its contents when the device is powered off. Non-volatile memory, such as ROM, retains its contents. In addition, some non-volatile memory types are one-time or multi-programmable, including flash and EEPROM. Freescale offers a unique type of memory system called FlexMemory technology. FlexMemory may be configured as a fast-write, high-endurance EEPROM or a data/program flash memory. Kinetis MCUs contain this innovative FlexMemory which allows flash to be used as EEPROM, reducing average power consumption and improving the endurance of a standard EEPROM. FlexMemory can improve endurance and is capable of exceeding 10 million cycles.

In addition to memory used for program and data storage, other devices, such as metal fuses, act like one-time programmable memory. This type of storage is usually limited in size and primarily used to "trim-in" analog performance of the device. The trimming may be done at the IC manufacturer's test site or at final hybrid assembly. Some fuse programming might be done at hybrid assembly to associate tracking or lot information with a device. Traceability is a key component for medical device manufacturers.

The "brain" of the implantable integrated circuit is the **CPU**, often referred to as the **microcontroller** or **microprocessor**. The microprocessor executes the program memory and establishes the register contents that control the AFE. The control of the AFE output is often derived from the analysis of the incoming data that has been digitized by an analog-to-digital converter (ADC) and read by the microprocessor. In many cases, the ADC may be built into the same integrated circuit as the microprocessor. In other cases, the ADC is considered part of the AFE. In addition, some microprocessor units may also have a companion floating point unit (FPU) or digital signal processing unit (DSP) that allows for more detailed analysis of the incoming sensed data. Freescale has a broad portfolio of 8-bit to 64-bit, as well as multicore options. An example of a CPU is the Kinetis K50 family of microprocessors. The K50 includes a 100 MHz ARM® Cortex™-M4 core and a 1.25 DMIPs/MHz DSP and comes with up to 512 KB of flash, 128 KB of SRAM, and 256 KB of FlexMemory. The 10 flexible power modes of the K50 allow customization of power usage based on application requirements. The microprocessor, combined with memory storage devices, can be referred to as the digital backend. As with the Kinetis microprocessor family, many analog functions are integrated with the microprocessor and memory.

Communication must occur between the implantable device and an external controller. Communication is necessary for initial setup of the implantable device and for monitoring and control of the implantable device. There are numerous communication standards that may be used to communicate between the implantable unit and the external controller or programmer. These standards include medical band radio MedRadio or Medical Implantable Communication Service (MICS), Bluetooth®, Bluetooth Low Energy and ANT. New system architectures include translation functions which convert the more common MedRadio/MICs protocol to one of the more open standards such as Bluetooth to allow ubiquitous connectivity to smart mobile devices.

There are also many proprietary, inductively coupled, short range telemetry methods used for communications with implantable devices. Typical carrier frequencies are 100 to 200 KHz with a transmission range of less than 20 cm.

In addition to Freescale's offerings, Cactus Semiconductor has developed multiple telemetry platforms capable of bidirectional communication using back telemetry load modulation. In some systems the communications link may also be used to recharge the battery. This eliminates the need for two coils in the controlling unit and two coils in implantable device.

Power management is critical in the development of implantable devices. Implantable devices are powered by some type of battery or charge storage device such as a super capacitor. Though many of these power sources are rechargeable, the recharging process involves patient interaction or may be otherwise inconvenient. Thus, maximizing the battery life or time between recharges is important. We will define power management as the means by which we optimize and conserve the use of power for the implantable device.

Power management can be optimized in several ways. One of these is by controlling which circuits are consuming power during specific operations or states. By only powering up circuits that are required to run in a given state, we can reduce the power consumed. As previously mentioned, the Kinetis K50 microprocessor does exactly this. The K50, along with the other members of the Kinetis family, has 10 power modes. Besides the low power modes, the peripherals on the K50 are also low power. For example, the K50 op amp has a low power configuration bit that allows operation at less than 200 µA. Table 1 indicates the specific power modes of operation for the Kinetis K50 microprocessor and the corresponding current consumption in each mode.

Table 1: K50 Modes of Operation and Power Consumption

Modes of Operation	Current Consumption of K50 @ 50 MHz
Run	10.5 mA (210 uA/MHz)
Wait	7.1 mA
Stop	130 uA
VLP Run	710 uA
VLP Wait	210 uA
VLP Stop	5.1 uA
LLS	3.5 uA
VLLSx	800–900 nA
RTC only	550 nA
RTC off	100 nA

A second method to reduce power consumption is to tailor the power consumption of the individual circuits to the specific application. This includes the development of innovative circuits that inherently consume less power while maintaining the necessary performance level for the application. Many off-the-shelf components are designed to operate over a broad range of applications and performance requirements. This increased device flexibility and performance typically results in additional power consumption. From a system perspective, the use of many off-the-shelf discrete components requires many output signals to be driven off chip. The increased parasitic capacitance associated with driving output bond pads and printed circuit board traces increase power consumption. The integration of several components into a single integrated circuit reduces inter-chip connections and reduces power consumption. In addition, the reduction in component count also reduces overall device size and improves reliability. Both reliability and device size are critical parameters for any implantable device.

Finally, the use of switch mode power supplies (SMPS), such as boost converters, buck converters, and charge pumps, allows circuits to be run with minimum overhead voltage. Reducing the overhead voltage for a circuit reduces the power that a circuit wastes. If noise becomes an issue on sensitive analog circuits, a low dropout linear regulator can be used between the SMPS and the analog supply rail. This technique provides a good compromise between power consumption and noise injection from the supply.

3 Design Partitioning and Silicon Technologies

Choosing how to partition the electronics is one of the most debated topics in IC design. This is true not only for implantable circuits but most electronic integrated circuits. First, we should clearly define what is meant by design partitioning as this term applies to integrated circuits. Design partitioning is the process by which we determine which electronic blocks or features will be grouped together on a single silicon die and/or in an IC package. For example, Freescale considered system partitioning when designing the Kinetis portfolio, allowing different peripherals to be added on. The Kinetis portfolio contains devices with or without analog front-end features. Devices like the K10 have standard features and no AFE, while devices like the K50 include standard features of the K10 but have integrated AFE and USB peripherals. As previously stated, since smaller size and lower power are critical parameters of implantable circuits, it might seem obvious that maximum integration is always preferred. However, there are many trade-offs and options that must be considered when determining an optimum design partition.

First and foremost, integration of certain components and/or component values may not lend themselves to silicon integration. This is usually the case for inductors and large capacitor values. Certain protection structures for enhanced ESD, cauterization and defibrillation might be more efficiently implemented with a small external discrete device.

Another factor to consider in design partitioning is flexibility. Embedding a microprocessor and memory into a full custom system-on-a-chip (SoC) means that any future upgrades to the microprocessor and memory equates to a full revision of the SoC. A revision to a custom integrated circuit is usually costly and time consuming. Similarly, embedding the RF communications into a SoC locks the device into a specific communications standard. For these reasons as well as others, designed flexibility must be considered when partitioning the design.

Finally, performance trade-offs and risk must be considered when partitioning a design. Integration of an entire system onto a single piece of silicon means both the sensitive AFE circuits and the "noisy" digital circuits will reside on the same silicon substrate. This presents noise challenges that can compromise the performance of the analog. Also, as previously stated, pure digital processes are optimized for gate density and minimum processing steps to reduce cost. Therefore, critical analog features may not be available in a more digital-centric process. While digital technology is driven towards ever decreasing geometries, this drives up off-state leakage and reduces the allowed voltage levels on an IC. These issues increase off–state power dissipation and may compromise analog performance levels. Conversely, a process optimized for the analog requirements of an implantable IC may not provide the desired density for integration of the digital. This can result in an IC that is significantly larger than desired and/or a sacrifice in digital performance. Therefore, the design partitioning of an IC must take into consideration the available silicon technologies

There is not an optimum process for an implantable integrated circuit. As previously stated, the system design partitioning will play a central role in the selection of the silicon technology. Is the design for a pure AFE or a complete SoC? Silicon technologies for implantable devices must take into account the key features and specification requirements for the device. These requirements will vary based on the application. However, within the constraints mentioned above, there are some general considerations for selecting a process that will allow for a successful IC development. Table 2 lists the key considerations for selecting a technology. This list is not meant to be all inclusive, but serves as an excellent starting point. Depending on the design partitioning, some of the key considerations may not be applicable.

Table 2: Key Process Considerations for Implantable ICs

Technical Feature Considerations	Business/Supply Considerations
• HV MOS Devices: Maximum Voltage	• Production Maturity
• Substrate Isolated MOS Devices	• Production Longevity (Commitment)
• Bipolar Devices	• On Approved Supplier List
• Diodes (Types: Zener, Rectifier)	• Quality Systems Status
• Low Leakage Analog Devices	• Capacity Capabilities
• High Density Linear Capacitors	• Cost
• High Sheet Rho Thin Film Resistors	
• High Current Output Drivers	
• ESD Library	
• Digital Library Characterized at Voltage	
• Memory Types (Flash, EEPROM, RAM)	
• Number Of Metal Layers	
• Process Density (Geometry)	
• Process Design Kit (PDK): Which Platform	
• Simulation Models: Noise, Sub-Threshold, Leakage and Voltage Coefficient Modeling Supported	
• Table 2.0 Key Process Considerations for Implantable ICs	

A couple of unique process considerations for the implantable device space are process maturity and longevity. Unlike many commercial digital ICs where advantages are gained by quickly migrating to the latest and greatest technology, process maturity is extremely important for implantable ICs. Many implantable devices are life sustaining devices. A mature and well established process will be less likely to have process revisions that can result in a full product requalification. A mature process will also have significantly more quality and reliability data available to ensure robustness.

In addition, process longevity is essential to ensure a supply line for the IC. Many ICs for implantable devices will take years to obtain full approval by the FDA and begin production. Once in production, the device may remain in production for 10 years or more. Therefore, it becomes imperative that the technology supporting the IC remains supported by the IC manufacturer. Many high density digital technologies become obsolete well before the life cycle of an implantable device is complete. IC obsolescence can require the medical device company to make a lifetime buy of the IC or create the need to embark on a redesign of the IC in another technology or with another supplier. All of these options are considered costly and undesirable. For example, Cactus Semiconductor recently completed a port of a SoC neurological stimulation device. This device was originally designed in the 1990s on a 3.0 um N-substrate technology. This device will continue in production for at least another five to seven years.

Freescale's SMARTMOS8 (L/M)V family of processes is particularly suited for implantable AFE ICs. These technologies are mature processes with a long-term commit to production. The processes provide for a wide set of features, making them an excellent choice for many custom AFE designs. CMOS, bipolar and LDMOS transistors are

available with support of voltages up to 80 volts. Passive components, such as thin film resistors and double poly capacitors, are available for precision analog design. High valued poly resistors and low off-state leakage help to conserve power. Excellent protection against substrate injection is provided, which also helps to provide for superior noise immunity. The process can leverage up to four layers of metal and bond over an active area to reduce die interconnect and overall die size. The technology offers a full process design kit (PDK) compatible with the most widely used suite of IC design tools. Freescale's latest generation of SMARTMOS technology has improved analog, power and digital capabilities on a reduced chip size. Both SMARTMOS 10 and 8 are highly capable, robust, cost-effective and innovatively packaged.

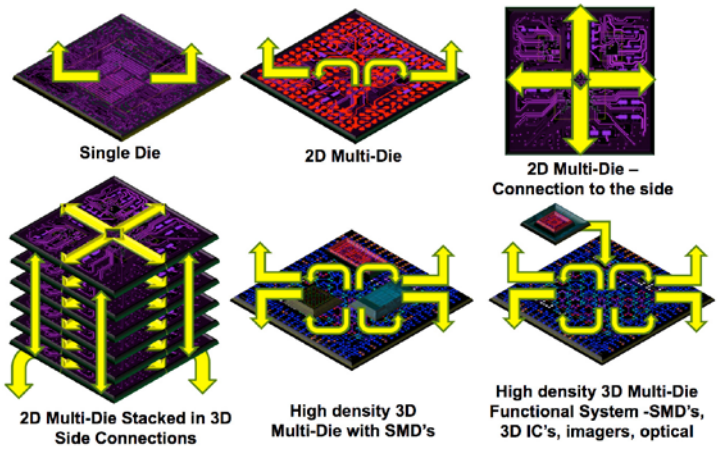
4 Forward-Looking Projections: Beyond the Integrated Circuit

Integrated circuits are only one component of an implantable medical device. In order to address the size, weight and power challenges of the system we must look at the system in its entirety. For example, battery technology is another key component. Decades ago, batteries accounted for a majority of the weight and size of a pacemaker. Through the reduction in power requirements and advances in battery technology, the size and weight of the implantable device has dropped significantly. However, battery size still presents a challenge to the overall size of the system. Integrated intelligent thin film battery technology and energy harvesting techniques may provide future advances in this area. A solid state battery can be made extremely small with custom sizes and aspect ratios. The battery can be rechargeable with a DC voltage, requiring no current charging. For increased battery capacity, the cells can be paralleled or made larger. Cactus Semiconductor has developed two implantable systems based on this type of battery technology.

Mechanical aspects of the design present similar challenges in size. As mentioned previously, MEMS-based sensors are becoming more prevalent. Benefits include low cost, low power, miniaturization, high performance and integration. The availability of MEMS and sensors (transducers) in standard IC processing can provide further advances in integration. Bringing MEMS into the standard IC design flow will also require IC design tools (PDKs) to support this integration.

Advanced packaging technologies will also help reduce overall size and improve performance. It is imperative to reduce cost and overcome temperature challenges, as markets increasingly require smaller, faster, higher performing devices. Freescale offers a broad array of packaging technologies, including redistributed chip packaging (RCP). This interconnect technology makes the package a functional part of the die and/or system. RCP has a number of key advantages, including the elimination of wire bonds, package substrates and bumping, which improve performance, reduce size, reduce power consumption and improve manufacturability. The RCP package platform allows for significant flexibility to the system integrator. Options include ultra thin packages (< 125 µm including solder bumps), multi-layer stacked packages, 2-D multi-die, 3-D heterogeneous systems, integration of multiple die, surface mounted devices (SMDs), integrated passive devices (IPDs), memory, MEMs sensors, imager, etc. For several leading customers and especially for key medical implantable companies, the RCP technology is providing a game changing opportunity. Size, performance and power are everything. These advancements provide compelling solutions while supporting today's wafer technology and manufacturing process as well as those advanced nodes currently in development. Figure 2 depicts a diagram of the different types of redistributed chip packaging.

Figure 2: Redistributed Chip Packaging Options



5 Summary

When considering integrated circuits for an implantable device, one must examine the entire system from the top level. Overall system-level requirements, such as functionality, performance, size, weight and power should be considered. These requirements, along with the availability of existing off-the-shelf solutions and desired system flexibility, should help drive design partitioning. Freescale's latest packaging technologies, low-power microcontrollers, sensors and RF technologies allow for an innovative design to meet the requirements of implantable devices.

To optimize or meet the device specifications for any of these parameters, a custom integrated circuit may berequired, the design of which can expensive and time consuming. The early engagement of an experienced IC development team that can help with the design partitioning and process selection greatly increases the likelihood of success, reduces risk and potentially reduces cost.

It is the intent of the authors to follow up with additional publications that explore in greater depth the individual sections presented in this overview white paper.

About the Authors

James McDonald holds an MSEE from Boston University and a BSEE from Arizona State University. He is co-founder and president of Cactus Semiconductor, a fabless semiconductor firm that specializes in custom medical integrated circuits, including ASICs used in implantable applications. Prior to founding Cactus Semiconductor, James served as design manager with Medtronic's Semiconductor Group in Tempe, Arizona.

Steven Dean is the global medical market lead for Freescale. He has been in the semiconductor business for over 25 years, working with Texas Instruments, Analog Devices and Medtronic. Steven obtained his degree in electrical engineering from Purdue University, with postgraduate work in business.

David Niewolny is the medical segment manager with Freescale's Microcontroller Solutions Group. He has over 11 years of semiconductor industry experience ranging from operations to sales, marketing and business development. David has helped launch over 25 product lines which have been designed into home portable, diagnostic and therapy devices. His specific focus is in the area of connected (wired/wireless) medical devices. David holds an MBA from the University of Texas at Austin and a B.S. in biomedical engineering from Iowa State University.

Donnie Garcia is a systems engineer with Freescale's Microcontroller Solutions Group. He is responsible for new product introduction encompassing product definition to development tool requirements, and die size trade off and feasibility studies. As an active member of Freescale's intellectual property (IP) teams, Donnie defines IP roadmaps and IP for new products and conducts research and evaluation of competitive products.

Navjot Chhabra manages operations, research and development for Freescale's redistributed chip packaging technology within the Packaging Solutions Development organization. He has held several positions within Freescale and Motorola. As the director of interconnect at SEMATECH International he led the ultra low k and advanced metallization program. Chhabra helped launch the first consortia-backed effort on 3-D IC technology. In addition, he has held several key leadership positions in front-end IC manufacturing, process development and device integration and holds several patents in the area of process development and design.

Loris Chang is a biomedical engineering student at the University of Texas at Austin.

About Freescale Semiconductor

Freescale Semiconductor (NYSE:FSL) is a global leader in the design and manufacture of embedded semiconductors for the automotive, consumer, industrial and networking markets. The company is based in Austin, Texas, and has design, research and development, manufacturing and sales operations around the world. **freescale.com**

About Cactus Semiconductor

Cactus Semiconductor is a fabless semiconductor company that provides innovative custom analog and mixed signal integrated solutions in low power, portable and sensing applications such as medical devices and portable battery operated products. Cactus Semiconductor is a privately held company with headquarters in Chandler, AZ and also has engineering and sales support in Dallas, TX. **cactussemi.com**

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Home Page:
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e-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
1-800-521-6274
480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate,
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

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