

Integration Challenges of 0.1μm CMOS Cu/Low-k Interconnects

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Abstract

The integration challenges of a low-k dielectric ($k < 3$) to form multi-level Cu interconnects for the next generation 0.1μm CMOS technology are presented. Process improvements to overcome these challenges are highlighted which include etchfront control, resist poisoning, high aspect ratio metallization, and improved CMP planarity. The maturity of this technology has been demonstrated through high yield of a 4MB SRAM test vehicle.

Introduction

To achieve circuit speed enhancements, Motorola has utilized dual inlaid Cu interconnects for four generations, since the 0.2μm technology node (1-4). With rapidly decreasing feature sizes, low-k dielectric and passivation materials have been inserted to address the need for additional RC delay reductions. The RC reduction of low-k materials is dependent on the integration strategy, which impacts the effective k value (k-eff) of the dielectric stack. Fig. 1 shows the steady intra-level capacitance reduction achieved by introduction of low-k materials ($k < 3$) at the metal level vs. metal/via levels for 0.13μm and 0.1μm technology nodes, respectively. With feature size and k-value reduction comes integration challenges specific to low-k films including etch optimization, resist poisoning, high aspect ratio metallization and CMP planarity.

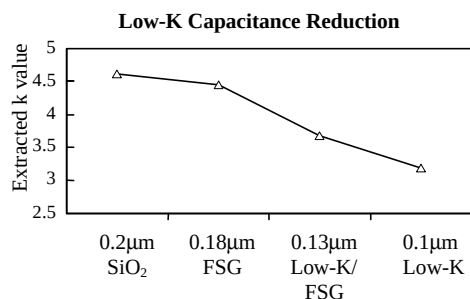


Fig 1. Low-k dielectric constant vs. intra-level k-effective capacitance reduction for 0.2μm to 0.1μm CMOS technology applications.

Table 1. Layout rules for 0.10μm vs. 0.13μm CMOS technology.

Layer	0.13 μm	0.10 μm	Shrink
Metal 1 Line/Space	0.18/0.18	0.12/0.12	33 %
Metal 2-8 Line/Space	0.21/0.21	0.14/0.14	33 %
Via Size/Space	0.18/0.24	0.13/0.15	28 %

This paper will first present the interconnect performance of an OSG based low-k/Cu multi-level backend and then will highlight unit process solutions developed to achieve successful low-k integration.

BEOL Process Integration

Key BEOL design rules supporting our 0.1μm 8LM technology platform, with a 6T SRAM cell size of 1.16μm², are shown in Table 1 (4). To pattern these dimensions, 193nm photolithography is used at critical levels. Extensive optical proximity correction (OPC), optimized resist and etch processes, and standard 248nm lithography are used for dual-inlaid levels from M2/V1 and above. Low-k materials for Cu passivation have been used to reduce k-eff, and timed etches have been developed to eliminate the use of a mid-etch stop layer. Fig 2. shows a two-dimensional SEM x-section of our 4M TDSRAM test vehicle at M3.



Fig 2. SEM x-section of interconnect structure with Cu/Low-k ($k < 3$) at all metal/via levels.

Through optimization of the low-k dielectric stack and Cu CMP processes, tight M1 sheet resistances have been achieved for both isolated lines and lines with 0.5μm wide neighbors, as shown in Fig 3. Low leakages for unpassivated M1 twin-serpentine structures are seen in Fig 4. Dual-inlaid via chain yield has been demonstrated for

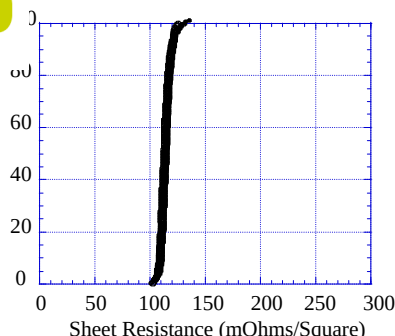


Fig 3. M1 sheet resistance of ○ isolated lines vs. ● lines with wide neighbors.

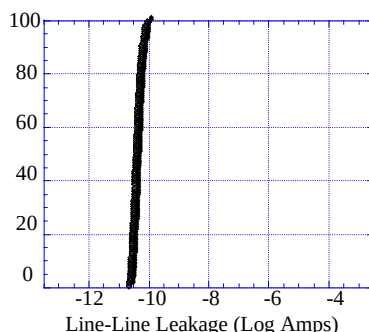


Fig 4. M1 leakage for a twin-serpentine with length of 3.9m.

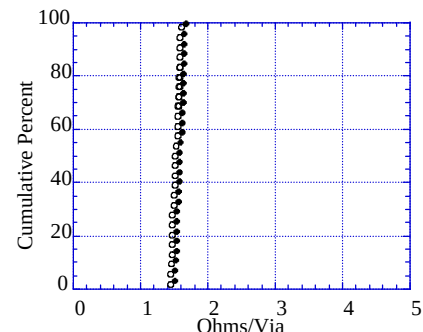


Fig 5. Via chain yield of ○ 8.6M vias and ● 600k M1-M3 stacked vias.

both 8.6M vias and stacked M1-M3 via chains, as shown in Fig 5. High 4M TDSRAM yield has been achieved by leveraging a foundation of unit process development for low-k films, as highlighted in the following sections.

Ech Process Optimization

The use of low-k dielectrics in BEOL integration has required extensive changes in both etch and ash chemistries. For example, low-k films are more susceptible to ash damage and require a shift away from standard oxidizing chemistries. This is particularly challenging for dual inlaid structures which often require aggressive processing that is more likely to harm the low-k materials.

In order to achieve the lowest integrated k value of dual inlaid structures, it is advantageous to eliminate the middle stop layer (MSL). However, trench bottom profile control becomes more difficult without a MSL to prevent continued etch during the etch stop layer (ESL) open and to prevent damage during the ash. Fig 6 shows fully etched SEM cross-sections of a via chain structure. Etch process A shows less corner erosion at the via/trench bottom intersection compared to process B. However, even etch A shows erosion as a result of the aggressive ESL etch used to reduce defectivity.

Fig 7 shows two different ash processes on the same low-k material. Both SEM samples were prepared at the same time under identical conditions to allow a qualitative comparison. Stain delineation is used to highlight etch damage, as shown by arrows in Fig 7. While not a substitute for more quantitative measurements, stain delineation easily demonstrates the reduction in low-k resist A, as quantified by defect metrology tools. The use of an alternate resist has also eliminated resist poisoning with the VFSL integration damage between process A and process B. These results, coupled with suitable tests for defect control, were used to develop a low-k compatible ash process.

Resist/Integration Optimization

Resist poisoning associated with low-k films is well known and is a function of the dielectric stack and resist

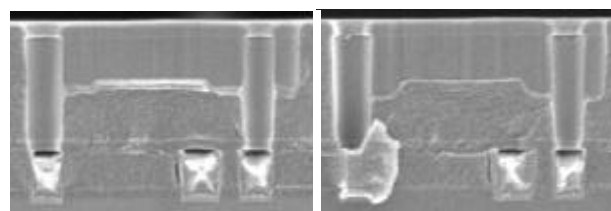


Fig 6. SEM cross sections comparing trench bottom profiles for etch process A (left) and etch process B (right) for fully etched, no MSL wafers. Sample preparation artifacts are seen on the wafers.

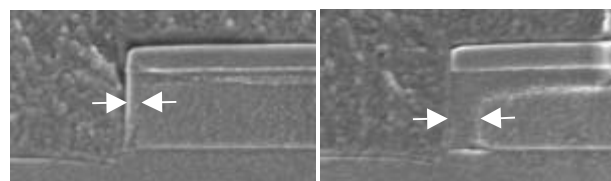


Fig 7. Qualitative ash damage for low-k on SEM cross sections of wide trench features. Ash A (left) shows less damage from wet stain preparation than ash B (right).

selection (5). We have shown elimination of via poisoning with a TFVL based low-k integration compared with VFSL for resist A, as quantified by defect metrology tools. The use of an alternate resist has also eliminated resist poisoning with the VFSL integration.

Metals Process Optimization

Ionized PVD Tantalum (nitride) based barriers have served the industry well since the 0.22μm Cu technology node. However, PVD barriers can show less than 10% step coverage for high aspect ratios vias. Tighter geometry along with low-k integration challenges have driven investigation of Ti, Ta, and W based barrier materials in addition to alternate deposition techniques (6). Fig 8 shows improved PVD barrier sidewall coverage through process optimization along with a reduced bottom thickness to reduce the via resistance. Fig 9A shows the via resistance reduction of a 14M via chain with ALD, CVD vs. PVD

ers. For ultra low-k (ULK) materials with larger pore size, PVD barriers may not be able to provide continuous coverage. Although CVD and ALD barriers can provide ultra-thin (<5nm) conformal coverage, many new integration challenges associated with these barriers must be resolved before wide acceptance with low-k and ULK materials is seen. Some of these challenges include absorption and diffusion of deposition gases into the ULK, preclean compatibility, acceptable EM, seed and CMP performance, metrology availability, and cost of ownership improvement.

CMP Optimization

Development of CMP processes with low defectivity for low-k materials poses a significant challenge because of their reduced hardness and modulus. The use of a cap material with good low-k adhesion and minimal low-k damage improves planarity, as seen in Fig 10. For ULK materials ($k < 2.5$), increased cap adhesion greatly improves interline leakage. This may result from reduced delamination and microcracks in the cap layer. Improvement in the incoming Cu plate uniformity, shown in Fig 11, can also significantly impact CMP planarity.

To increase device yield, low-k compatible CMP post-polish cleaning chemistries have also been developed. This new process and in-house formulation drastically reduce slurry precipitates and prevent photo-voltaic dendritic corrosion. Improved Cu surface passivation is observed as well.

Conclusion

Successful integration of low-k ($k < 3$)/Cu interconnects for the 0.1 μ m CMOS technology has been demonstrated. Unit process development in photo, etch, metals and CMP has overcome low-k integration challenges to deliver a robust backend for next generation low power and high performance products.

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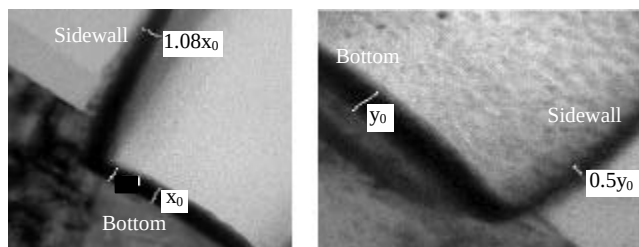


Fig 8. Improved relative PVD barrier sidewall coverage and reduced bottom thickness of process A (left) vs. process B (right). Scale is normalized to bottom thickness.

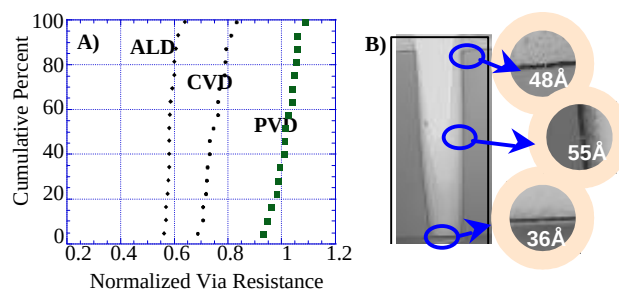


Fig 9. A) Via chain yield (M4-V3-M5) of 14M vias. Significant via resistance reduction is observed using ALD and CVD vs. PVD barrier. B) High aspect ratio via shows CVD barrier coverage with site specific barrier thicknesses.

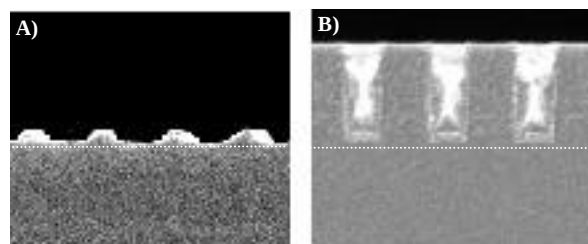


Fig 10. Effect of dielectric stack on erosion using standard Cu CMP processing. A) Full ILD loss observed for uncapped low-k material. B) ILD preserved for capped low-k material.

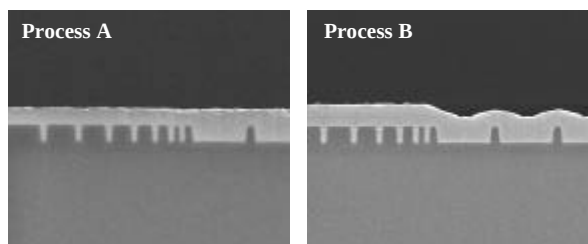


Fig 11. Improved planarity observed from alternate Cu plating techniques.

References

- (1) S. Venkatesan, et al. IEDM, 1997.
- (2) P. Gilbert, et al. IEDM, 1998.
- (3) A. H. Perera, et al. IEDM, 2000.
- (4) S. Parihar, et al. IEDM, 2001.
- (5) J. Wetzel, et al. IEDM, 2001.
- (6) S.M. Rossnagel and H. Kim, IITC, 2001.