Design Implications of Low-K

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ABSTRACT

The aggressive technology migration of the last 10 years is presented. The circuit-level electrical characteristics of interest (performance, power, area, noise) that drive the definition of the back-end of line (BEOL) architecture features (material, width, pitch, space) are discussed. The paper finishes with a portrayal of the system, circuit, and technology options that may be needed in the 65nm to 45nm technology nodes to maintain scalability.

INTRODUCTION

Technology migration beyond the 0.25um node has caused a paradigm shift. The BEOL metallization becomes the fundamental roadblock to true scaling. Transistor improvements are used to overcome the limitations imposed by the metallization. This is evidenced by the ever increasing disparity between the transistor gate delay and the BEOL RC delays (Fig. 1) [1]. Furthermore, the interconnect capacitance is a disproportionately higher percentage of the total capacitance.

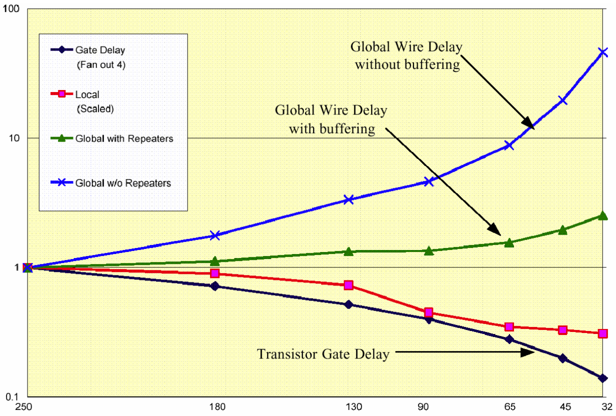
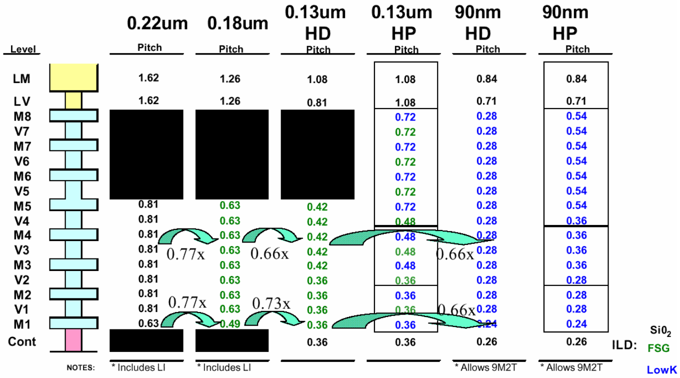


Fig. 1. ITRS portrayal of BEOL delay and Gate Delay vs. Technology



Level	0.22um Pitch	0.18um Pitch	0.13um HD Pitch	0.13um HP Pitch	90nm HD Pitch	90nm HP Pitch
LM	1.62	1.26	1.08	1.08	0.84	0.84
LV	1.62	1.26	0.81	1.08	0.71	0.71
M8				0.72	0.28	0.54
V7				0.72	0.28	0.54
M7				0.72	0.28	0.54
V6				0.72	0.28	0.54
M6				0.72	0.28	0.54
V5				0.72	0.28	0.54
M5	0.81	0.63	0.42	0.72	0.28	0.54
V4	0.81	0.63	0.42	0.48	0.28	0.36
M4	0.81	0.63	0.42	0.48	0.28	0.36
V3	0.81	0.63	0.42	0.48	0.28	0.36
M3	0.81	0.63	0.42	0.48	0.28	0.36
V2	0.81	0.63	0.36	0.36	0.28	0.28
M2	0.81	0.63	0.36	0.36	0.28	0.28
V1	0.81	0.63	0.36	0.36	0.28	0.28
M1	0.63	0.49	0.36	0.36	0.24	0.24
Cont			0.36	0.36	0.26	0.26
NOTES:	* Includes LI	* Includes LI			* Allows 9M2T	* Allows 9M2T

Fig. 2. Comparison of Motorola's Metallization Scaling

BEOL SCALING AND LOW-K TECHNOLOGY RESULTS

Fig.2 shows Motorola's BEOL scaling [2].The metal dielectrics contain a low-k material to provide the low capacitance. In Fig. 3, the extracted K of the dielectric stack is plotted vs. the material [3]. At the 130nm node this yields a high density metallization with an effective K of about 3.6. The high density BEOL is further improved in the 90nm technology to have an effective K of about 3.0. Fig. 4 shows that the use of Low-K dielectrics allows for an RC reduction close to 20% [4]. Other features of this metallization technology are discussed elsewhere [2].

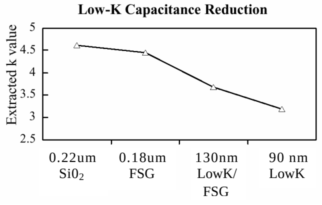


Fig. 3. Extracted K vs. Integration

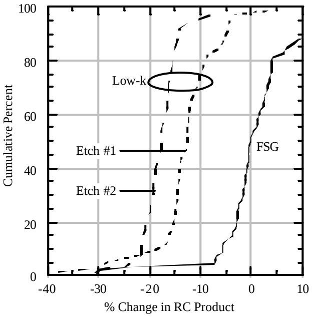


Fig. 4. Improvement in RC delay

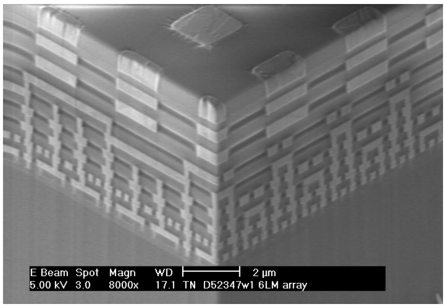


Fig. 5: 130nm Dual Inlaid High Performance BEOL 9LM cross-section

CIRCUIT LEVEL ASSESSMENT FOR LOW-K SPECIFICATION:

The tight pitch BEOL definition is driven by low-power and small area designs that are optimized for number of die per wafer at minimal number of wiring levels. However, high performance designs, such as multi-GHz microprocessors, need a hierarchical routing scheme to optimize the interconnect for different goals. In Fig. 6, a 9-metal level representation of the high performance BEOL shows that there are 4 distinctive metallization applications: local routing driven by low capacitance needs; intermediate routing for optimal power and RC product; upper routing for highest interconnect performance; and a last metal needed for power distribution, clock routing, and C4 escape.

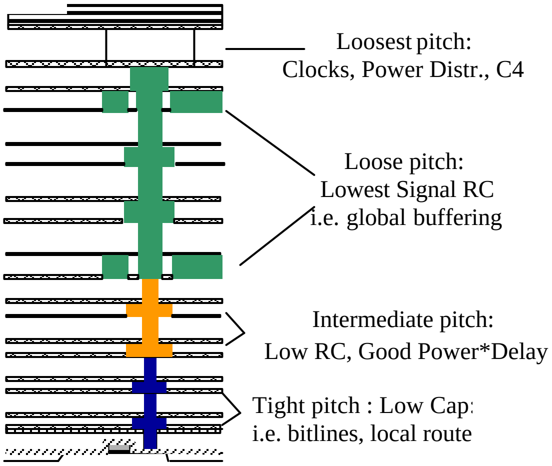


Fig. 6. High Performance Dual Inlaid BEOL Modules

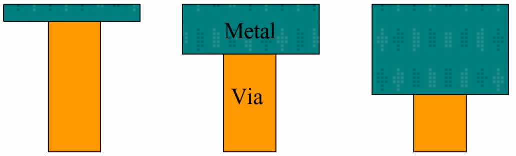


Fig. 7. Metal Options Design Space

Circuit path sensitivity to RC

A primary goal of the hierarchical BEOL is to improve the RC delay (i.e. ps/mm). At a given pitch, there is a range of metal and via thicknesses that are within the manufacturing window (Fig. 7). Technologists and designers need to fully comprehend the different optimization points for an optimal BEOL definition. Fig. 8 shows the performance in ps/mm of buffered wires at a given distance for 2 options in each module. The delay of the intermediate pitch metals is noticeably larger than that of the loose pitch wires. Furthermore, simultaneous switching noise can increase the buffered delay anywhere from 10% to 20%.

Buffer Switching Power

Switching power is usually approximated based on the metal capacitance being switched. However, buffers that drive long wires typically use low-Vt devices to improve performance. The signal edge rate has a large influence in the cross-over current seen inside buffers, to the point that it can overwhelm the switching metal power itself. This increase in current can cause electromigration violations inside the drivers. Simultaneous switching of signals can increase edge rates (due to capacitive coupling), causing the total power to increase by at least a factor of 2 (Fig. 9a). An approach to deal with this problem is to limit the wiring distances based on a maximum edge-rate. (Fig. 9b) Clearly, any low-K solution that minimizes this capacitive component helps power, area, and performance!

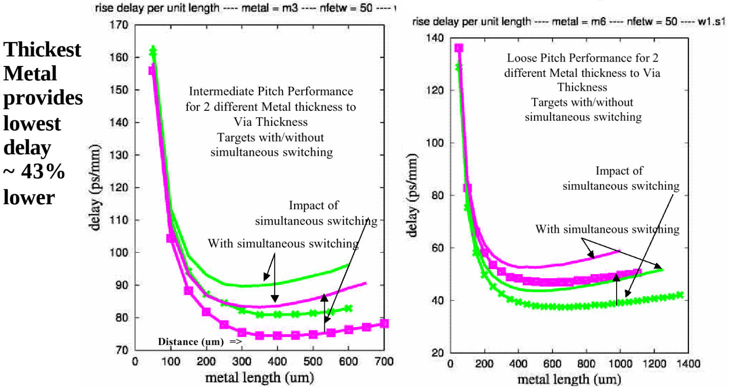


Fig. 8. Intermediate (left) and Loose (right) pitch metal buffered RC performance for two BEOL options at minimum width/pitch

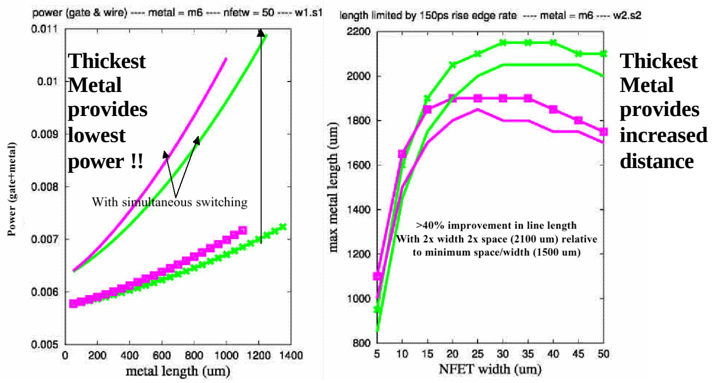


Fig. 9. a) Switching Power b) Maximum Distance at fixed edge rate

Noise coupling and Clock Skew

Fig. 10 shows the peak noise simulated for a range of M6 and M3 options. M3 can have anywhere from 2X to 3X the amount of noise seen at the M6 level with equally sized drivers, even though the wire thickness is 0.7x that of M6. This implies that the resistance of M3 is shielding the driver from the noise and thus more resultant noise is seen at the far end receiver. For a fixed noise budget, the alternative BEOL options (thickness of metal/via) can result in larger than 3X maximum wiring distance differences on a design! At M6, the thickest wires produce the largest noise levels. It should be pointed out that *inductive* noise coupling is an issue for the thicker wire options as well and needs proper handling during design. The intermediate BEOL modules are critical for custom circuits. Clock skew across a 64-bit adder that spans 800um of wire is anywhere from 70ps to 130ps over a range of BEOL metal/via thickness options [2].

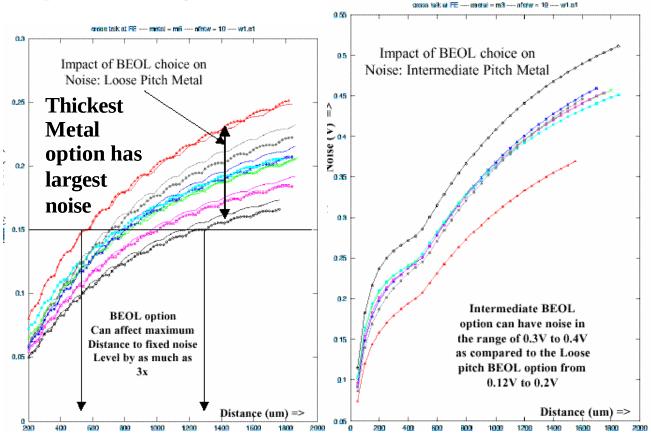


Fig. 10. a) M6 b) M3 Noise as a function of Metal Height/Via Height

Dynamic Circuit sizing Strategy

Dynamic circuits are used extensively in speed critical paths of high performance microprocessors. Sizing of dynamic gates is strongly influenced by both transistor characteristics as well as BEOL characteristics [5]. A typical dynamic cell used for establishing the sizing strategy for dynamic gates is shown in Fig. 11. The dynamic node, dyn, has process-dependent leakage mechanisms modeled. As noise from chip level signals couples into the signal IN during the evaluate cycle, transistor I11 turns partially ON, thus causing node dyn to droop. At this point pmos halflatch keeper transistor I1, sources current to maintain node dyn at Vdd level. The BEOL characteristics dictate the peak noise and noise pulse width seen by the dynamic gate.

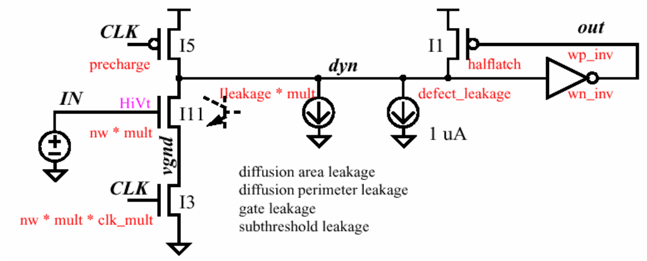


Fig. 11. Dynamic gate structure used to size “halflatch” keeper I1

Table 1 shows the characteristics of the AC noise for one given BEOL option. Circuit analysis using SPICE is done to determine the size of the halflatch as a function of the distance to any given input. At long distances, the AC noise can reach as much as 043V. This level of noise causes a dramatic size increase in the halflatch to maintain the dynamic node from switching. Just as important, a large halflatch means a loss in performance since when you do need to switch the dynamic node, the nmos pulldown devices have to overcome the halflatch current.

Table 1. AC noise stimulus characteristics and corresponding performance implications for one M3 BEOL option

Distance (Tracks)	DC noise height (mv)	AC noise height (mv)	AC noise width (ps)	AC Noise Ratio	Delay Relative to short wire
50	0	96	12	1.00	1.00
200	13	251	15	2.61	1.03
400	25	360	25	3.75	1.05
800	50	439	52	4.57	1.14

Composite plots showing the performance and size implications for the halflatch device to maintain a noise droop of no more than 10% of Vdd are generated. At a fanout of 1, the difference in halflatch size between a 50 tracks distance (0.096V peak noise) and 800 tracks distance (0.439V peak noise) is a factor of 5, with a corresponding performance degradation of 14%. Referring back to Figs. 10a and 10b, it can be appreciated that the choice of BEOL characteristics is thus a first order effect for dynamic circuit sizing.

FUTURE BEYOND 90nm

At Keff levels of 2.5 at the 90nm-65nm technology there are serious concerns about the scalability of BEOL technology. Low-K materials with Keff <= 1.8 pose substantial manufacturing challenges. Furthermore, Cu resistivity is increasing due to grain-boundary scattering effects. The question then becomes: what are the alternatives? The answers fall into many categories: technology-driven, circuit level, and micro-architecture driven choices. On the technology end of things, insertion of 3D chip topologies that cut down on wiring distances 30%-50% [6,7] . Air gaps will address effective capacitance reduction, whereas novel structures such as multi-thickness intra-level interconnects could address RC problems. Utilization of on-chip optical interconnect technology in targeted applications is envisioned. Micro-architecture driven solutions that exploit parallelism to allow running at lower frequencies yet maintain high instructions per cycle. Also, localized high frequency clocked domains with globally asynchronous communication is a possibility. At the circuit level, small signal signaling on chip may be required to speed up transmission over long wires.

CONCLUSION

The circuit-level electrical characteristics of interest (performance, power, area, noise, and skew) that drive the BEOL architecture definition are described. Designers and technologists need to pay careful consideration to the circuit level implications of BEOL choices (resistivity, thickness, Keff, width, and pitch) which influence the characteristics of a design.

ACKNOWLEDGEMENTS

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