Freescale Semiconductor
Solution Guide

IPDSLAM8360EWP
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Using the PowerQUICC™ II Pro MPC8360E to Build an Intelligent IP-DSLAM Line Card

The connected world has traditionally relied on ATM to deliver circuit switched capability from Central Offices (COs) into Wide Area Networks (WANs) or Internet Service Provider networks. However, with the potential to offer multiple revenue streams from a single IP packet network, triple play systems comprised of voice, video, and data are becoming a reality with next generation IP-packet networks. Many solutions being deployed by network manufacturers are beginning the migration from traditional circuit switched ATM-based networks into Ethernet, IP packet switched architectures.

As a result, traditional ATM-based, circuit switched line cards are becoming more intelligent as line card architectures move from a centralized ATM-based to a de-centralized, packet switched/IP-based architecture. This added intelligence, in addition to the high-speed triple play services that an increasing number of connected users now expect, requires significant increases in the data rates, bandwidths and port density of the DSLAM (Digital Subscriber Line Access Multiplexer) equipment. Also, while DSL technologies have increased available bandwidths with the deployment of ADSL to ADSL2+ and VDSL to VDSL2 line rates, network equipment manufacturers face an increasingly competitive marketplace. Success in this market can only be met by aggressively reducing the overall DSLAM line card cost per port and giving users future proof solutions which can deliver a rich feature set of services.

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1 Design Challenges

As a result of this change in the way users communicate and the competitive business environment facing many telecommunication equipment manufacturers, the specific design challenges facing a successful IP-DSLAM solution include:

- Technology migration from legacy based ATM Circuit-switched to Ethernet packet-switched solutions
  - At the data plane, solutions must handle ATM to IP interworking
- Increasing port density on line cards – typically 24 to 96 ports
- Dramatic bandwidth increases due to demand for high performance services / standards e.g. ADSL2/+, VDSL for triple play”
  - Managing QoS to ensure prioitization of latency sensitive traffic to meet service level agreements
  - Multiple QoS dictates the need for different hierarchical IP or ATM traffic scheduling and shaping capability
- Intelligence moving from edge of network – centralized to decentralized architectures
  - All signaling now being performed at a packet level by the line card
  - DSLAM architectures converging with edge router architectures
- Challenge of managing / maintaining VLAN Quality of Service (QoS) and Service Level Agreements (SLA) when migrating from circuit switched to packet switched technologies
- Ensure the security / confidentiality of subscribers information
- Provide the ability to add new features and functions through software based on market and subscriber demands

Figure 1 illustrates interworking scenarios that a typical IP-DSLAM must support.

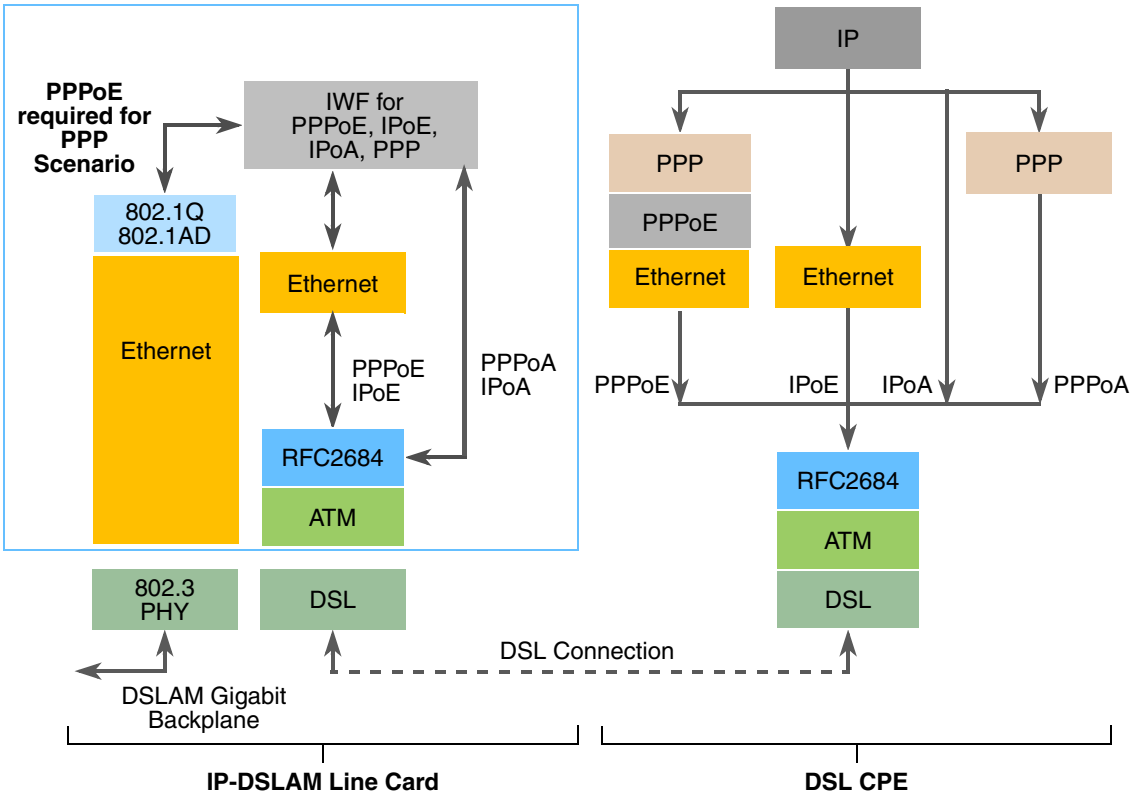

Figure 1. IP-DSLAM Protocol Interworking

Figure 1 illustrates a typical connection between an IP-DSLAM and the customer's premise equipment. The IP-DSLAM has to support and inter-work between both ATM and Ethernet – ATM for the DSL connection to the CPE and Gigabit Ethernet for the backplane uplink. The IP-DSLAM must also be able to handle packet routing using either IP or PPP (for transmitting datagrams over serial point-to-point links). Thus, for both IP-DSLAM and CPE systems, compliance to the multi-protocol encapsulation over ATM (RFC 2684) is required.

Because all connected users share the same common IP-DSLAM, protecting the privacy of each subscriber's data is a highly critical issue. This dictates the use of Virtual LANs (VLAN) using the 802.1Q standard—allowing complete subnet separation and isolation for each connected user. Preventing users from accessing the databases of other tenants is another design requirement and this can be achieved by using port filtering techniques such as IP/MAC filtering, data encryption, and IP access control. Finally, providing and coordinating such data services between other VLANs/LANs in a bridged network environment requires compliance to the 802.1ad Provider Bridge standard.

2 Freescale Semiconductor Solutions

In the competitive IP-DSLAM market, highly integrated, cost-effective and scalable system solutions are required. With these system requirements in mind, Freescale is pleased to introduce the latest addition to its popular PowerQUICC family of microprocessors—the PowerQUICC II Pro MPC8360E.

The MPC8360E incorporates the e300, 603e core which includes 32 Kbytes of L1 instruction and data caches, 32-bit PCI bridge, four DMA channels, USB support, dual 32-bit DDR memory controller, a double precision floating point unit and on-board memory management units. A block diagram of the MPC8360E is shown in Figure 2.

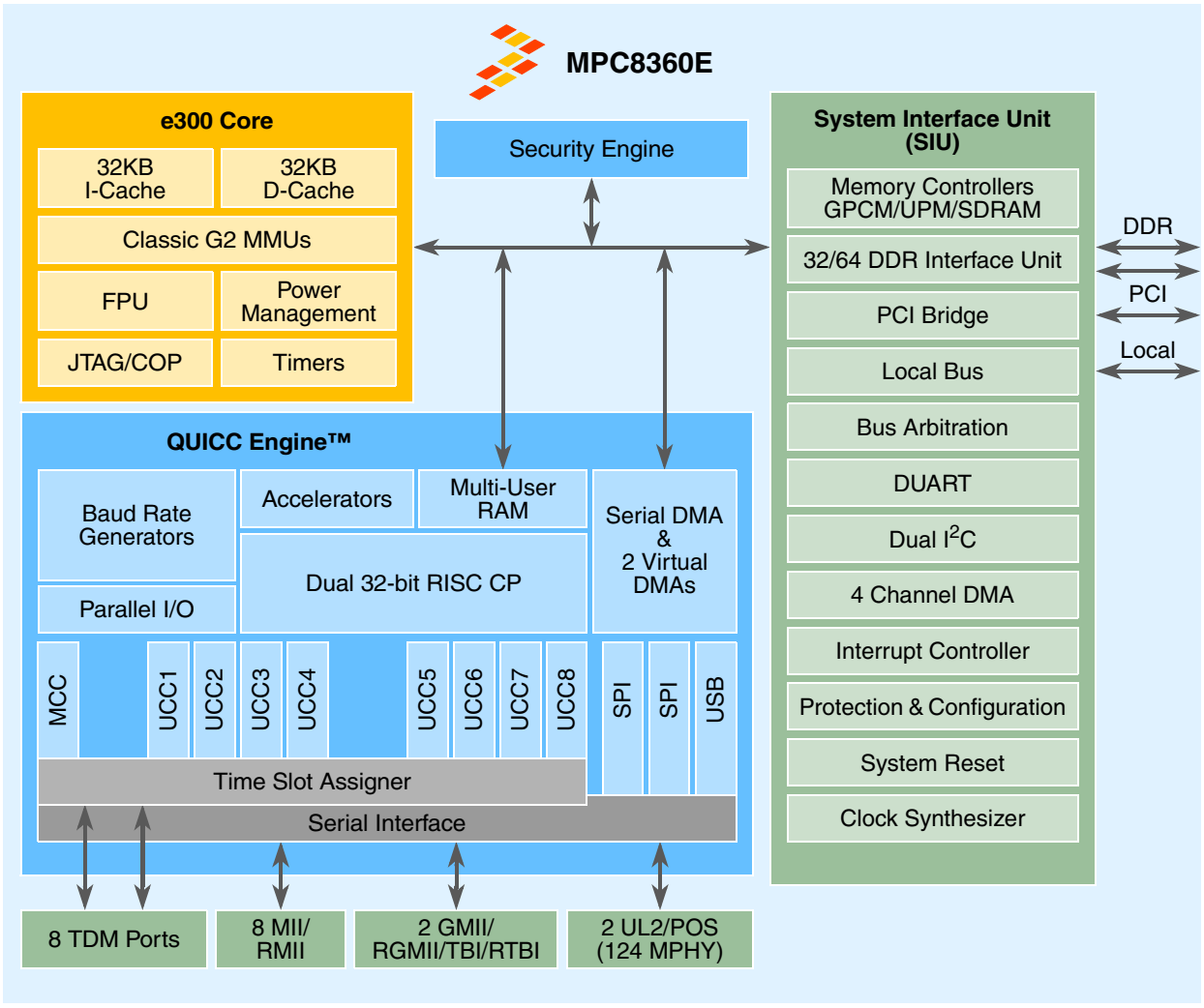

Figure 2. MPC8360E Block Diagram

A new communications complex—the QUICC™ Engine—forms the heart of the networking capability of the MPC8360E. The QUICC Engine contains several peripheral controllers and integrates two 32-bit RISC controllers. Each RISC controller can control multiple peripherals and work together to provide increased aggregated system bandwidth for higher throughput applications. Protocol support is provided by the main workhorses of the device—the unified communication controllers (UCCs) and multi-channel communication controller (MCC).

Each of the eight UCCs can support a variety of communication protocols: 10/100/1000 Mbps Ethernet through a Media-Independent Interface, ATM / POS PHY support up to OC-12 speeds, Serial ATM, Multi-PHY ATM, HDLC, UART, Multi-Link/Class PPP, BISYNC and 64 TDM channels. Each MCC is capable of supporting up to 256 TDM channels in either transparent or HDLC channel modes and multiplexing almost any combination of sub-groups into a single or multiple TDM stream. Inverse Multiplexing over ATM is supported and allows ATM traffic to be distributed across multiple E1/T1 circuits. This allows service providers to lease the exact bandwidth that subscriber's request.

In addition, the QUICC Engine can also support two UTOPIA level 2 or two POS interfaces, each interface capable of supporting 124 Multi-PHY, or up to two, 128 Multi-PHY interfaces using extended address mode. The QUICC Engine also features an integrated 8-port, L2 Ethernet switch which can provide 4 priority levels on each port,

VLAN functionality, IGMP snooping, network auto-negotiation function, store-and-forward switching and packet-error filtering. Enhanced interworking features within the QUICC Engine helps offload the main CPU. The QUICC Engine can provide ATM-to-ATM switching, Ethernet to ATM switching with L3 / L4 support and PPP interworking.

The MPC8360E's security engine allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, AES, SHA-1, MD-5, and ARC-4 algorithms. It includes a public key accelerator and an on-chip random number generator.

In summary, the MPC8360E provides IP-DSLAM vendors with a highly integrated, fully programmable communications processor that allows reuse of existing legacy PowerQUICC II and III software drivers and microcode packages. This helps ensure that a low cost system solution can be quickly developed and will offer flexibility to accommodate new standards and evolving system requirements.

2.1 The PowerQUICC II Pro MPC8360E

The PowerQUICC II Pro MPC8360E is a high performance, highly integrated communication processor solution that offers the following.

2.1.1 MPC8360E Features

- High-performance, low power (< 5W typical power dissipation), and cost-effective communications processor
- The MPC8360E QUICC Engine offers a future proof solution for next generation designs by supporting programmable protocol termination, network interface termination, and interworking features to meet evolving protocol standards
- Single platform architecture supports the convergence of IP packet networks and ATM networks, including interworking between these networks
- Simplified network interface card design with a cost-effective single chip data plane/control plane solution for ATM or IP packet processing (or both). This reduced component count, board power consumption and board real estate.
- Universal network interface card design for multiple applications, which lowers costs and reduces time-to-market
- Built-in proprietary, hardware accelerators that accelerate data plane traffic, such as interworking, and control plane packet snooping, such as IGMP, VLAN tagging, DHCP, and so on
- DDR memory controller—one 64-bit or 2x32-bit interfaces that split data and control plane traffic at up to 333 MHz
- e300 PowerPC core (enhanced version of 603e core with 32K bytes of Level 1 Instruction and 32 Kbytes of Level 1 Data caches)
- 32-bit PCI interface
- 32-bit Local Bus interface
- USB
- Integrated 8-port L2 Ethernet switch
  - 8 connection ports of 10/100 Mbps MII/RMII & one CPU internal port
  - Each port supports four priority levels
  - Priority levels used with VLAN tags or IP TOS field to implement QoS

  - QoS types of traffic, such as voice, video, and data
- A security engine provides termination or encrypted plane traffic
- High degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration
- Seamless connection to PowerQUICC III family devices for increased control (CPU) application processing requirements

2.1.1.1 Protocols

- ATM SAR up to 622Mbps (OC-12) full duplex, with ATM traffic shaping (ATF TM4.1) for up to 64K ATM connections
- Support for ATM AAL1 structured and unstructured Circuit Emulation Service (CES 2.0)
- Support for IMA and ATM Transmission Convergence sub-layer
- ATM OAM handling features compatible with ITU-T I.610
- PPP, Multi-Link (ML-PPP), Multi-Class (MC-PPP) and PPP mux in accordance with the following RFCs: 1661, 1662, 1990, 2686 and 3153
- IP termination support for IPv4 and IPv6 packets including TOS, TTL and header checksum processing
- L2 Ethernet switching using MAC address or IEEE 802.1P/Q VLAN tags
- Support for ATM (AAL2/AAL5) to Ethernet (IP) interworking
- Extensive support for ATM statistics and Ethernet RMON/MIB statistics.
- Support for 256 channels or HDLC/Transparent or 128 channels of SS#7

2.1.1.2 Serial Interfaces

- Support for two UL2 / POS-PHY interfaces with 124 Multi-PHY addresses each.
- Support for two 1000Mbps Ethernet interfaces using GMII or RGMII, TBI, RTBI.
- Support for up to eight 10/100Mbps Ethernet interfaces using MII or RMII
- Support for up to eight T1 / E1 / J1 / E3 or DS-3 serial interfaces
- Support for dual UART, I²C and SPI interfaces.

System scalability is also made available through the number of UCCs and MCCs. The initial implementation offers eight UCCs and one MCC, however as a result of the system-on-a-chip design methodology used for the QUICC Engine, these numbers can be scaled to support an optimized mix of communications channels. The flexible architecture of the QUICC Engine allows customers to customize their own application protocol and filtering requirements, allowing Freescale to add more RISC engines and/or UCCs on future family derivatives.

2.2 Development Environment

Development tools, hardware platforms, software building blocks and application-specific software solutions are available from Freescale and our Freescale Alliance Program, including third party protocol and signaling stack suppliers, real time operating systems support and a variety of applications software support. All of this builds upon the existing industry standard PowerQUICC family support program.

2.2.1 Software Development Tools

To simplify and accelerate the development process, Freescale will provide a user-friendly, integrated development environment (IDE), which includes a compiler, instruction set simulator and debugger for the e300 PowerPC core.

2.2.2 Application Development System (ADS)

Freescale provides an ADS board as a reference platform and programming development environment for the MPC8360E with a complete Linux Board Support Package. The ADS board will support on-board DDR SDRAM memory, a PCI interface, and a debug port and can be configured with optional daughter cards supporting protocols such as OC-3 or OC-12 ATM, 8xT1/E1 and Ethernet (10/100/1000Base T).

Also available is a complete development system based around the AdvancedTCA (ATCA) form factor chassis with a choice of AMC cards that can be operate stand alone, or as modular inserts into the main processor baseboard. This allows maximum flexibility for prototyping wireless network interface, control and base band applications using Freescale silicon solutions.

2.2.3 Modular Software Building Blocks

The QUICC Engine will be supported by a complete set of configurable device API drivers and initialization software. Figure 3 shows the wealth of software protocols that the QUICC Engine with the e300 PowerPC™ core is able to provide.

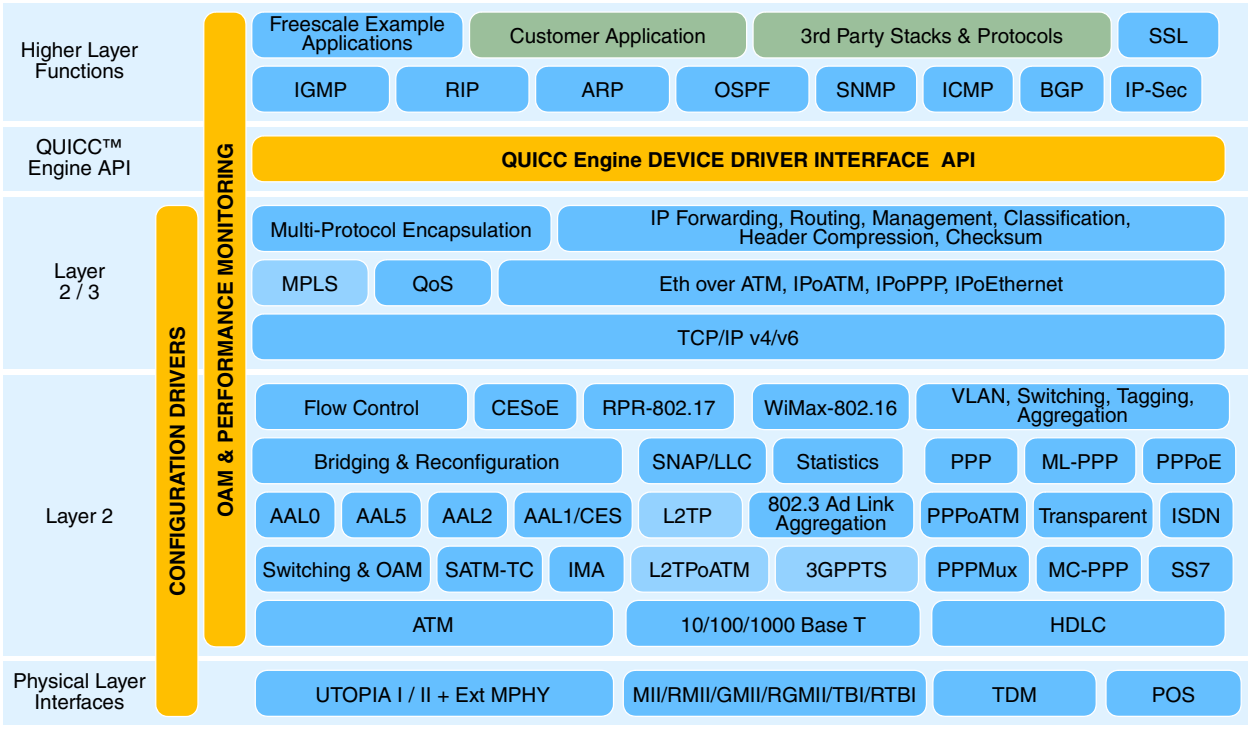

Figure 3. Software Protocol Support for the QUICC Engine

3 IP-DSLAM Application Example

The internal features and protocols supported by the MPC8360E allow a wide range of network solutions to be developed. Figure 4 illustrates a typical central office IP-DSLAM application that facilitates the convergence of both packet and circuit switched networks.

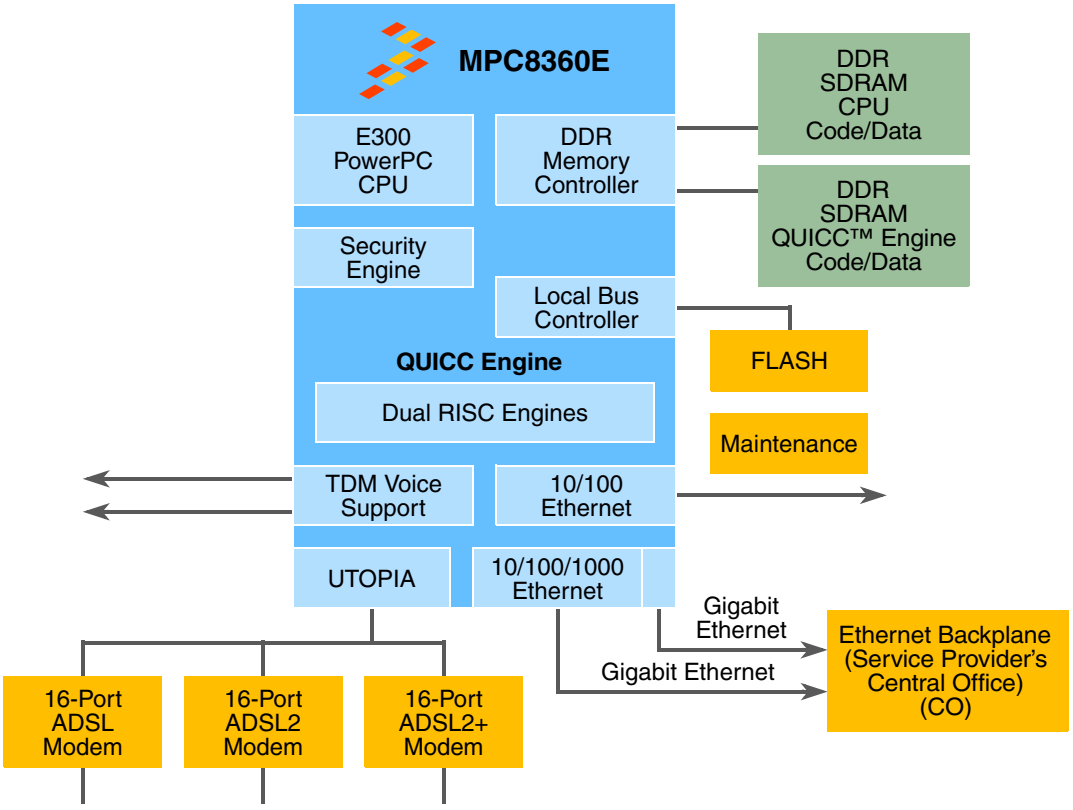

Figure 4. Freescale MPC8360E IP-DSLAM Example

As shown at the bottom of the Figure 4, subscribers connect to the IP-DSLAM via the xDSL PHYs and the integrated UTOPIA interface on the MPC8360E. Here, different speed xDSL flavors can be supported, such as ADSL, ADSL2+, VDSL, and so on.

The uplink connection to the Ethernet backplane or service provider's central office can be made using one of the two available Gigabit Ethernet interfaces. Again, both Gigabit Ethernet MACs are fully integrated within the MPC8360E to minimize system footprint and simplify board layout. Additional Ethernet ports can be used for maintenance.

In this type of application, the MPC8360E uses its internal interworking features to offload the e300 CPU. ATM-Ethernet interworking is used to transfer data from the ATM-based DSL MTU subscriber inputs, through the RISC cores within the QUICC Engine and out through the Gigabit Ethernet on the uplink port. The MCCs within the QUICC Engine can also provide optional TDM voice stream support to allow a wider range of services to be provided, such as Voice over IP (VoIP).

The main system memory is provided by the DDR interface, which can either support one 64-bit or two 32-bit interfaces. This dual DDR architecture allows equipment providers to partition system parameters and data in an extremely efficient way. This helps ensure that data does not get blocked as the data plane can be decoupled between the QUICC Engine/DDR memory and control plane transactions. The local bus can be used for SDRAM or on-board

FLASH Eprom. The remaining unused UCCs can be configured as system terminals in order to allow some external I/O mechanism for debug and control.

4 Summary

The PowerQUICC II Pro MPC8360E with the new QUICC Engine is a significant step forward in performance, integration, and cost-effectiveness for a wide variety of applications. For flexible, high performance, IP-DSLAM line cards, the MPC8360E offers a comprehensive feature set that enables cost effective solutions with an unrivalled level of versatility to evolve as both standards and the system requirements change.

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