

Microeconomics of Overlay Control at the 65nm Technology Node

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Abstract – ITRS working groups have identified overlay control as a technology roadblock with no known solutions at the 65nm node and beyond. The most serious problems are total measurement uncertainty, CMP process robustness, and device correlation. A systematic root-cause analysis of pattern placement error (PPE) at Motorola’s Dan Noble Center has determined that current box-in-box overlay targets cause deficiencies in all three categories. A proposed solution utilizes advanced imaging targets that are grating-based and can be segmented with features that are similar to those in the device. In the case of poly-to-STI overlay using 193nm lithography tools, these targets show a 40% decrease in total measurement uncertainty.

THE OVERLAY CONTROL PROBLEM

As critical dimensions in semiconductor manufacturing continue to decrease, process control windows are shrinking commensurately. One necessary condition for smaller design rules is the control of edge placement error (EPE). In the factory, we measure EPE as two separate components: critical dimension error (CDE) and pattern placement error (PPE). Both are affected by other process errors, such as lithographic defocus, that may or may not be measured directly¹. In this work, we focus on the first of four key obstacles to PPE control as described below:

- **Hidden error²**. Some systematic variations may not be measurable with the current generation of metrology tools. For example, overlay metrology that uses traditional box-in-box targets may not reflect the PPE of actual device features in the presence of lens aberration, CMP distortions, or mask fabrication errors.
- **Unsampled error³**. Assuming the PPE is measurable, sparse and super-sparse sample plans may still fail to capture actual statistical distributions. If the mean of the sample distribution is shifted, false inputs will defeat APC systems resulting in costly yield loss, with insufficient historical data for root-cause analysis.
- **Unmodeled error⁴**. Measured PPE may depend on variables such as scan direction, stage direction, film uniformity, and wafer strain resulting from thermal processes. These systematic process shifts are not comprehended by the simple translation, rotation, magnification, and skew models typically used for overlay analysis and correction.

- **Uncorrectable error⁵**. Even accurately modeled error may not be amenable to cost-effective correction. For example, reticle PPE and cross-field lens distortions could require fabrication of a new mask. In addition, complex cross-wafer effects could require that grid corrections be made on a field-by-field basis.

While recognizing all four obstacles to overlay control, this work primarily addresses the issue of “hidden error” in overlay metrology and the consequences for manufacturing. Most hidden error is derived from three sources:

- **Reticle-induced error⁶**. Overlay mark fidelity (OMF) can be affected by reticle fabrication (Fig. 1).
- **Process-induced error⁷**. Overlay mark fidelity (OMF) on wafers is affected by process, such as CMP (Fig. 2).
- **Aberration-induced error⁸**. A scanner lens may image the mark and small device features differently (Fig. 3).

All of these sources of error can combine to reduce device correlation and decrease the yield-relevance of the overlay measurement.

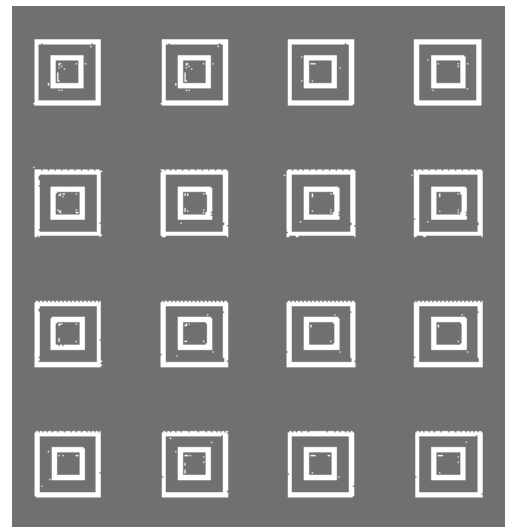


Figure 1. This reticle image of a 4x4 array of traditional box-in-box overlay marks shows damage to the structures. Studies at IMEC demonstrated that more robust, grating-based overlay marks can improve reticle OMF by 30%.

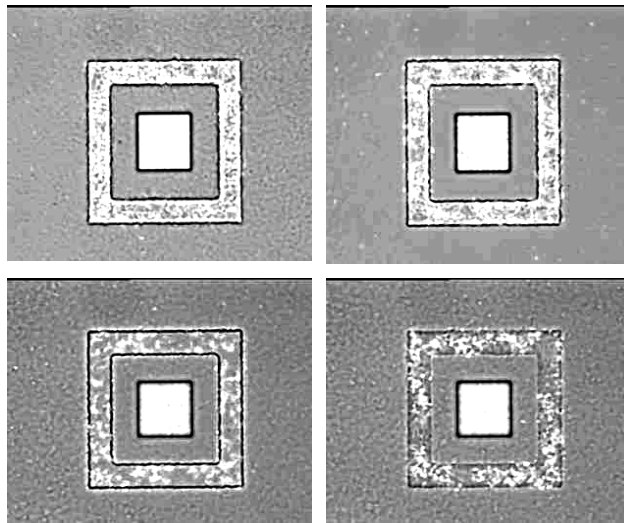


Figure 2. Traditional box-in-box overlay marks show CMP process damage at different locations on the same wafer. Studies at *Motorola* demonstrated that robust, grating-based overlay marks can improve process OMF by 34-67%.

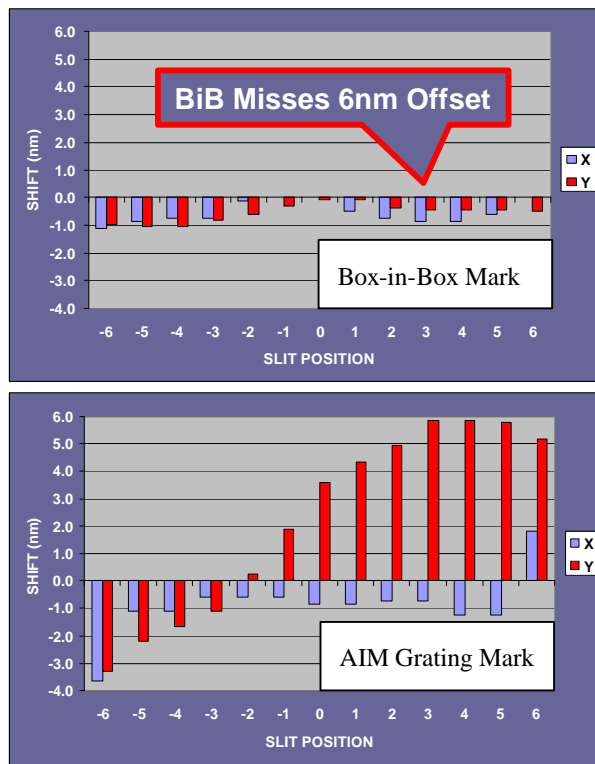


Figure 3. Example of a PROLITH simulation showing the inaccurate response of traditional box-in-box overlay marks in the presence of lens aberration. Grating marks that are segmented with device-like features show much better device correlation as a function of scanner slit position. Studies at *Renasas* independently validated similar shifts by comparing AIM results with SEM-based measurements.

A GRATING-BASED CONTROL SOLUTION

Our proposed solution to the overlay control problem at 65nm and beyond utilizes advanced imaging targets that are grating-based and can be segmented with features that are similar to those in the device. In the case of poly-to-STI overlay using 193nm lithography tools, these targets show a 40% decrease in total measurement uncertainty. The grating targets also improve reticle OMF, process OMF, and device correlation. As a result, the potential for overlay-related yield-loss due to *inaccurate* APC corrections or *undetected* PPE can be dramatically reduced. This paradigm shift is essential since overlay yield models predict revenue losses in millions of dollars per year per factory if no action is taken. The savings in rework alone could be more than 1% of production. Since these targets are compatible with the current bright-field overlay technology, the implementation cost is relatively low. Some results of the Motorola analysis at 130nm design rules are summarized in Table 1, below:

Table 1: Benefits	% Improvement Using AIM Target	
METRIC	Poly to STI	VIA to Metal
Metrology Precision	59	63
Overlay Mark Fidelity	67	34
Tool-Induced Shift	53	65
Total Uncertainty	40	32
Model Residuals	30	-

If no action is taken, we predict significant overlay control challenges going forward. Overlay process windows are narrowing and the yield entitlement at zero nominal error is falling due to poor correlation of box-in-box targets with in-device overlay. Narrow process windows and falling entitlement will combine to create a yield-loss explosion at the 65nm node, as shown in Figures 4 and 5. Two primary mechanisms for overlay-related yield-loss are a shift in the mean PPE and an increase in the width of the PPE distribution. Predictive models, calibrated using available factory data, show high sensitivity to both types of error.

The yield-loss distribution⁹ is the product of the PPE distribution (E) and a calibrated Taguchi yield loss function (y) that represents device yield as a function of overlay error¹⁰. The economic impact of PPE can be estimated by integrating over the yield-loss distribution:

$$Y_{overlay} \cong \int_{-\infty}^{\infty} y(x) \cdot E(x, \mathbf{s}) \cdot dx$$

Solving the integral equation for contours of constant yield (Y), as shown in Figure 6, we can predict that first-pass overlay yield losses are likely to exceed 3% at the 65nm node. Clearly, substantial tightening of the ITRS overlay control requirements is required to guarantee acceptable yield for future technology generations. *Beyond 65nm, control windows could be reduced by a factor of two from current ITRS levels.*

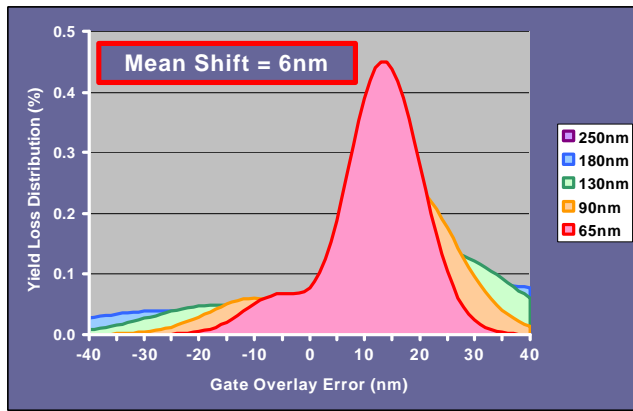


Figure 4: Overlay yield-loss distribution resulting from a 6nm mean shift. Product of yield error curve and shifted Gaussian error distribution derived from ITRS specifications for the 250nm to 65nm nodes.

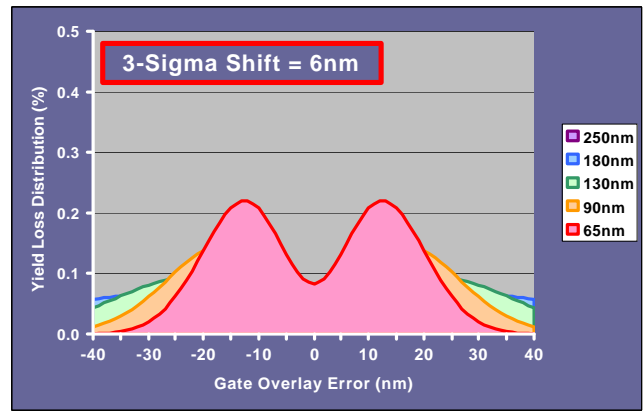


Figure 5: Overlay yield-loss distribution resulting from a 6nm loss of control. Product of yield error curve and Gaussian error distributions derived from ITRS specifications for the 250nm to 65nm nodes.

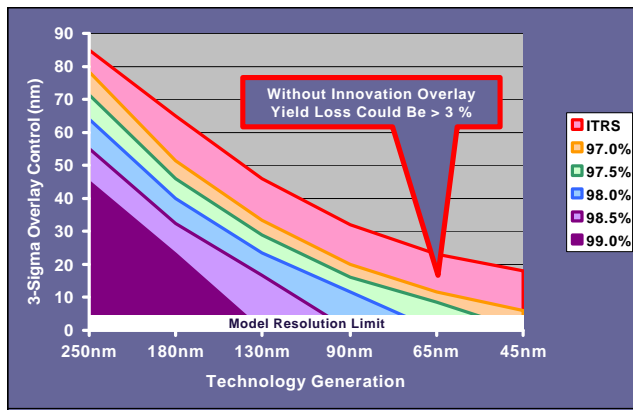


Figure 6: Contours of constant integrated yield-loss showing 3-sigma overlay control requirements compared to the ITRS requirements at each node. Overlay control must tighten to assure yields.

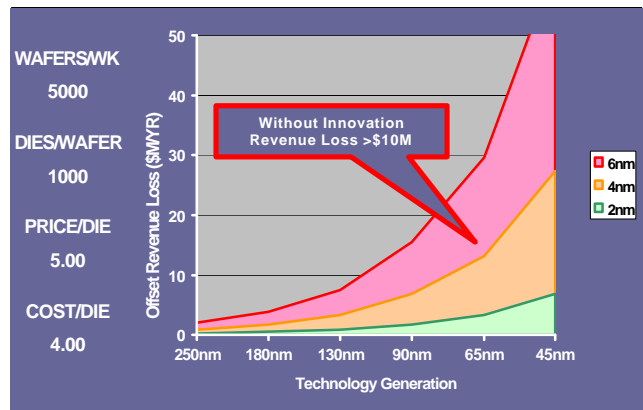


Figure 7: Revenue loss model for 400MHz 256Mb DDR SDRAM with constant device overlay offsets. At 6nm, losses in a large factory could be as much as \$30M per year. The timeframe is February, 2003.

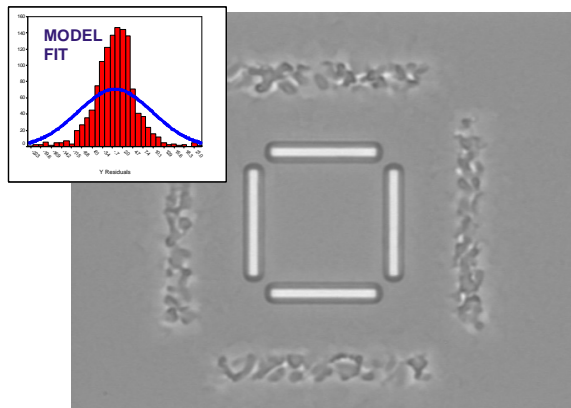


Figure 8: Traditional box-in-box targets have large open areas and are sensitive to CMP-induced distortion and process noise. They typically exhibit low device correlation and high model residuals.

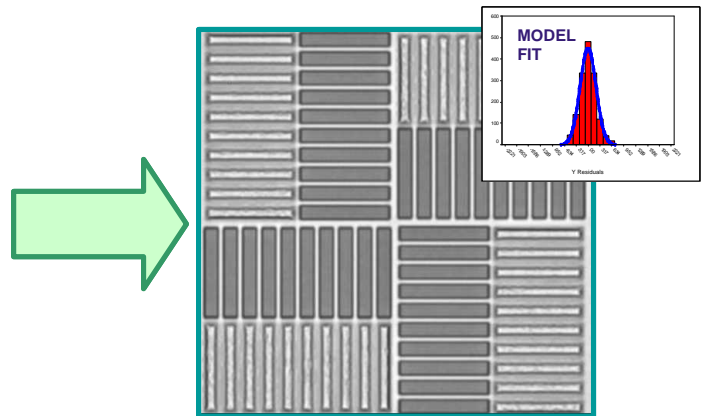


Figure 9: Dense grating targets have low sensitivity to CMP and process noise. Fine segmentation of the individual bars can improve device correlation and decrease model residuals.

A second way to quantify the economic impact of PPE is to examine revenue losses associated with a specific PPE at each technology node. Revenue is lost when undetected PPE results in failure at electrical test or when inaccurately measured PPE causes unnecessary rework or false APC corrections. In Figure 7, we consider the example of a large DRAM factory producing 5000 wafers per week with 1000 dies per wafer selling at \$5 per die. At the 130nm node, a PPE of 6nm could result in \$7M in revenue loss per year; but, *at the 65nm node, the same PPE quadruples the revenue loss to nearly \$30M per year.*

CONCLUSIONS AND RECOMMENDATIONS

Qualitatively, our conclusions align with the ITRS. We predict significant overlay control failures if new metrology solutions are not implemented at the 65nm node. In addition,

- Our economic models predict that overlay control failures could result in tens of millions of dollars in lost profit per factory per year.
- The relationship between overlay-related yield loss and shrinking design rules is non-linear and increases rapidly near the 65nm node, creating a technological barrier to profitability.
- We recommend overcoming this barrier by making a transition from traditional box-in-box to the more robust and accurate grating-based overlay metrology, as shown in Figures 8-9.
- When used in conjunction with state-of-the-art optics and algorithms, grating-based overlay measurement reduces total measurement uncertainty (TMU) while dramatically improving reticle OMF, process OMF, and device correlation.
- With hardware and software upgrades, grating-based metrology is compatible with current-generation brightfield overlay tools, so that incremental cost and implementation risk are minimized. Economic models predict that *annualized incremental ROI can be greater than 10 to 1 for the 65nm node and beyond.*

Our results show that advanced image metrology (AIM) can enable overlay control at the 65 and 45nm nodes. In addition, an AIM grating mark may be significantly smaller than a conventional box-in-box target. Given the premium on scribe line space, the small target size provides additional incentive for adoption in manufacturing.

Finally, since ability to predict device overlay is becoming a key requirement for future technology generations, new overlay technologies must enable measurement of device-

like structures in actual layer stacks. We anticipate that these requirements are likely to be addressed before the industry adopts alternative technologies.

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