AN1801/D
(Motorola Order Number)

4/1999
REV. 0

Application Note

Performance Differences between the MPC8240 and the MPC106

Top Changwatchai and Roy Jenevein
risc10@email.sps.mot.com

This paper discusses some of the major performance differences between the MPC8240's memory and PCI interfaces and those of the MPC106. This document compares the MPC8240 (rev. 1.0) the MPC106 (rev. 4.0). It contains the following:

- Part 1"Architectural Differences," discusses architectural differences between the two parts which impact performance.
  - — The MPC8240 offers faster memory and PCI buses and features PCI data-streaming capabilities.
  - — The MPC106 supports an external L2 cache, but this may result in lower memory bus speed.
- Part 2"Simulation," presents results from an analytical model used to compare various system configurations which highlight these architectural differences.

Part 1 Architectural Differences

This section discusses the differences in memory, L2 cache, and the PCI bus interface between the MPC8240 and the MPC106.

1.1 Memory

Both the MPC8240 and the MPC106 support three types of dynamic RAM (DRAM)—fast page mode (FPM), extended data out (EDO), and synchronous DRAM (SDRAM). Of the three, SDRAM typically provides the best bus bandwidth utilization. The MPC106 supports an 83-MHz SDRAM bus (66 MHz if an L2 cache is present), while the MPC8240 supports a 100-MHz SDRAM bus.

Access latency can be reduced (thereby increasing bus efficiency) if more open pages of memory can be maintained. The MPC106 can maintain 2 open pages, while the MPC8240 can maintain 4 open pages at once.

DRAM devices are accessed with a multiplexed address scheme—each unit of data is accessed by first selecting its row address (also known as "opening a page") and then selecting its column address. This unit of data is then transferred on the memory bus in a "beat." Transferring data in bursts (multiple-beat transfers) can increase bus efficiency and lower data access latency. During a burst transfer, the page and column are accessed for the first beat (just as for a single-beat transfer). For subsequent beats in the burst, the page is then kept open, with just the column address changing. Because the page does not have to be reopened during a burst, these subsequent beats will have much lower latency. For example, a typical SDRAM may have an 8-1-1-1 access latency, which essentially means 8 bus clocks to transfer the first beat of data, and 1 bus clock to transfer each subsequent beat in the burst[1].

Allowing pages to remain open between bursts can also result in lower latency. If a memory access hits in an already open page, then its first beat will be accessed more quickly. Again, the MPC106 can maintain 2 open pages at once, while the MPC8240 can maintain 4. Typical access latencies are presented in Table 1.

Table 1. Typical SDRAM Access Latencies

	Access Closed Page (miss)	Access Open Page (hit)
"fast" SDRAM	8-1-1-1	6-1-1-1
"slow" SDRAM	10-1-1-1	7-1-1-1

On the other hand, access latencies may be higher due to several factors, such as closing an already open page, or handling error correction code (ECC). If the maximum number of supported open pages are open when an access misses, then one page must first be closed before the new one is opened. The access time for the first beat will thereby be increased by about two bus cycles. Supporting more open pages, as the MPC8240 does, reduces the frequency of this occurrence.

The MPC106 includes ECC support for FPM and EDO. It does not support ECC for SDRAM, but it does allow an external device to provide this support. The MPC8240 supports ECC for FPM, EDO, and SDRAM. When ECC is enabled, access latency to memory is increased. For SDRAM ECC, the latency per beat is increased by one bus cycle.

The analytical model is conservative and does not include the effect of open pages, and it assumes that ECC is not used.

[1] Technically, these access latency numbers refer to the timing of the TS_ (transfer start) and TA_ (transfer acknowledge) signals on the 60x bus. TS_ signals the beginning of the bus transaction, and each TA_ signals that a data beat transfer completed successfully. The first number is the latency of the first data beat, and refers to the number of bus clocks (inclusive) from TS_ to the first TA_. Subsequent numbers refer to the number of bus clocks to transfer successive beats of the burst. Thus 8-1-1-1 means if TS_ is asserted in clock 1, then TA_'s are asserted in clocks 8, 9, 10, and 11.

1.2 L2 Cache

The MPC106 provides support for an external, lookaside L2 cache, the MPC8240 does not. An L2 cache can reduce data access latency by providing faster access to cached data. However, because the L2 cache shares the processor bus with memory, adding an L2 can introduce timing constraints which may lower the supported bus speed. Plus, the L2 tag RAM cannot run faster than 66 MHz so, as mentioned earlier, an MPC106 with L2 can support a 66-MHz SDRAM bus, as opposed to the MPC8240 (with no L2) which can support a 100-MHz SDRAM bus.

In addition, the speed-up due to having an L2 can be lowered by cache maintenance overhead, such as L2 castouts.

The analytical model includes the effect of an L2 cache, but it does not take the cache size as a parameter. Instead, it takes the cache miss rate directly as a parameter.

1.3 PCI Bus Interface

Both the MPC8240 and the MPC106 implement a 32-bit PCI bus interface, which provides a bridge between the 60x processor bus, memory, and the PCI bus. The MPC8240 offers two improvements—faster PCI bus and PCI data-streaming capabilities.

1.3.1 Bus Speed

The MPC106 supports a 33-MHz PCI bus, whereas the MPC8240 supports a 66-MHz PCI bus. Assuming the PCI devices can support this speed, PCI accesses should proceed twice as fast.

1.3.2 Data Streaming

For identical PCI bus configurations, the MPC8240's streaming capabilities allow higher PCI data throughput than the MPC106. The MPC8240 has two main streaming features not present in the MPC106—as a PCI target, it can support data bursts larger than 32 bytes; and as a PCI master, it can support transactions larger than 32 bytes through its on-chip dual-channel DMA engine. By streaming, the MPC8240 can utilize PCI bus bandwidth more efficiently than the MPC106 with greater potential data throughput.

1.3.2.1 No Forced Disconnects Every 32 Bytes

When acting as a non-DMA PCI bus master, both the MPC106 and the MPC8240 limit transaction size to 32 bytes[1]. When acting as a target, the MPC106 also limits transactions to 32 bytes, by issuing a PCI disconnect after up to 32 bytes are transferred. To continue transferring data, the mastering device must start a new transaction. The MPC8240, on the other hand, does not have this 32-byte limit; that is, it has the capability to transfer data as long as data can be supplied[2].

As a target, the MPC8240 is able to avoid the 32-byte limit on transaction size because it has two internal 32-byte buffers for reads and two buffers for writes[3]. Thus, while one buffer is being filled from the source (for example, memory), the other buffer can be written to the destination (for example, the requesting PCI device).

[1] The PCI specification does not have this limit on transaction size. PCI transaction sizes are realistically limited by internal buffers of the PCI devices, or by other device requests and the PCI master latency timer.
[2] Again, in practice transaction size is limited by the buffer sizes of the PCI devices. The MPC8240 does initiate a disconnect when a transaction crosses a 4096-byte page boundary, to limit the risk of prefetching into improper memory address spaces.
[3] The MPC106 also has two write buffers (only one read buffer), but the internal state machine still forces a disconnect every 32 bytes as a PCI target.

Each disconnect causes a delay before the next transaction is started; these delays can reduce data throughput. This disconnect penalty includes sending the disconnect signal, transmitting the new address (since the PCI multiplexes its address/data bus), allowing PCI bus turnaround and bus arbitration, and initiating the new transaction. The penalty may be increased if there is contention due to other PCI devices, or if the bus is not parked.

The minimum penalty for a disconnect for a PCI write is three PCI bus clocks—two before $\overline{\text{FRAME}}$ is asserted, plus one to transmit the new address. However, this doesn't allow other devices to take the bus, so depending on the PCI device the actual penalty is probably higher. Also, PCI reads incur a higher penalty than writes, for two reasons: first, there must be a one-cycle turnaround since the address and data are transmitted in different directions; second, after the new address is transmitted to the MPC106, there is some latency while the address is passed on to the memory device and data read into the MPC106. As data becomes available on the MPC106, it can then be transferred to the requesting PCI device.

Results from the analytical model are presented for a minimum disconnect penalty of 5 clocks, and for a more typical disconnect penalty of 8 clocks.

As a target, the MPC106 does support fast back-to-back transactions by the same master, in which the master starts a new transaction immediately, without an idle state. Theoretically, fast back-to-back PCI writes can incur a single clock penalty between writes (just to transmit the new address)[1]. This assumes that the MPC106 does not issue a disconnect (transactions must be 32 bytes or smaller). If transactions are disconnected, then a disconnect penalty applies as discussed above.

1.3.2.2 DMA Controller

The MPC8240 also has a software-programmed dual-channel DMA controller, which supports four types of data transfer: PCI to PCI, PCI to memory, memory to PCI, and memory to memory. For PCI to memory and memory to PCI transactions, data can be streamed continuously. The MPC8240 will not interrupt data transfer as long as there is data left to transfer and there are no errors on the PCI or memory buses, and no other intervening transaction occurs, including CPU memory accesses and memory refresh events.

How efficiently these data streaming features can be utilized depends on several factors such as:

- the transaction size that each PCI device can support,
- how large each transaction is, and if the data can be supplied quickly enough to fill the bus,
- whether PCI data accesses tend to be to contiguous addresses,
- how well software makes use of the DMA controller.

To fully exploit these features, software should be written with these factors in mind.

Part 2 Simulation

An analytical model was used to explore expected performance of synthetic workloads on current and potential MPC8240 and MPC603e + MPC106 system configurations. This section presents the results of this ongoing research and highlights several of the performance implications.

2.1 System Configurations

Several system configurations were compared using the analytical model, which takes system parameters as input and uses a set of formulas to calculate expected run time as output. Table 2 shows the MPC8240 system configurations modeled, while Table 3 shows the MPC603e + MPC106 configurations. These tables also present the run times for the various configurations (lower run time means higher performance), as well

[1] PCI reads incur a greater penalty, as mentioned earlier.

as the normalized rates of execution (higher rate means higher performance). The rates are normalized to configuration K-3a, an MPC8240 with 266-MHz processor clock, 66-MHz memory bus clock, and 33-MHz PCI bus clock (see Table 2).

The MPC8240 configurations assume that software has been modified to take advantage of PCI data streaming and DMA features. Other than that, the only differences between the two types of configurations are noted in the tables.

The analytical model assumes that memory timing is 8-x-x-x, or 8 bus clocks to transfer the first (critical) data beat. The model does not take into account the effect of open pages and the timing of subsequent data beats in the burst, since it is assumed that the timing of the rest of the system will mainly depend on the critical data beat. However, this assumption may not be accurate, particularly for bulk memory transfers. The effect of open pages for some applications can be significant and should be explored further, especially if high data throughput is important.

Two PCI disconnect penalties are modeled: a minimum realistic penalty at 5 clocks, and a more typical one at 8 clocks. However, both of these disconnect penalties are conservative, minimizing the advantage of PCI streaming. A higher penalty would favor the MPC8240 and highlight its PCI data streaming capabilities.

Several factors would increase the PCI disconnect penalty, such as non-parked bus, any delay due to internal signal latency, or any PCI bus contention. The actual disconnect penalty is highly dependent on the workload and transaction types, system configuration, and PCI devices. For example, a disconnect may trigger a device driver interrupt which could take many cycles to resolve.

Behavior parameters for the analytical model were obtained using a logic analyzer on a 266-MHz system and time-stamping all PCI bus activity. The application was a host processor issuing PCI transactions to a 2-D accelerator card to generate 3-D graphics. This provided the necessary data size and rates over the PCI bus along with computation load factors[1].

[1] Based on sample run on test platform: 1,000,000,000 instructions causing 27,838 pages to be written (4096 bytes each), resulting in roughly 10% bus utilization (see later figures where this is varied). To take advantage of PCI streaming, software would need to set up the MPC8240’s DMA processor, or command a PCI device to master the transaction.

Table 2 . Performance of MPC8240 System Configurations

Name	Processor Clock	60x/Memory Bus Clock	PCI Bus Clock	Relative Performance (Run time in seconds, Rate Normalized to Config. K-3a)			
	(MHz)	(MHz)	(MHz)	PCI disc. = 5 clocks		PCI disc. = 8 clocks	
				Run time	Rate	Run time	Rate
K-1a	300	100 (3:1)	33	8.92	1.290	8.96	1.289
K-1b			66	8.46	1.361	8.48	1.362
K-2a	266	90 (3:1)	30	10.05	1.145	10.09	1.145
K-2b			60	9.53	1.208	9.58	1.206
K-3a	266	66 (4:1)	33	11.51	1.000	11.55	1.000
K-3b			66	11.05	1.042	11.07	1.043
K-4a	250	100 (5:2)	33	9.69	1.188	9.73	1.187
K-4b			66	9.23	1.247	9.25	1.249
K-5a	250	83 (3:1)	33	10.52	1.094	10.56	1.094
K-5b			66	10.06	1.144	10.08	1.146
K-6a	200	66 (3:1)	33	12.92	0.891	12.96	0.891
K-6b			66	12.46	0.924	12.48	0.925

Lower run time means higher performance. Normalized rate is inverse of run time, so higher rate means higher performance

MPC8240 configurations feature PCI data streaming, 32-bit PCI bus, and no L2 cache

PCI target disconnects occur every 256 bytes (representative buffer size for PCI device)

No 250 MHz parts are currently available, so the 250 MHz configurations are 266 MHz parts run at the lower frequency

Configuration K-1 does not correspond to an announced part and is used for comparative purposes only

The MPC8240 configurations in Table 2 feature various processor speed/memory bus speed combinations. Each combination is modeled with 33 MHz PCI bus and 66 MHz PCI bus. For the synthetic workload, the resulting run time was computed for each of the two PCI disconnect penalties (5 and 8 clocks). The rate of execution was calculated by taking the inverse of the run time and normalizing to configuration K-3a[1].

[1] For example, take K-6a. For PCI disconnect = 5, this configuration's run time is 12.92 seconds, as opposed to 11.51 seconds for K-3a. Dividing 1/12.92 by 1/11.51 yields 0.891. For PCI disconnect = 8, dividing 1/12.96 by 1/11.55 yields 0.891.

Table 3. Performance of MPC603e + MPC106 System Configurations

Name	Processor Clock	60x/Memory Bus Clock	L2 Cache Present?	Relative Performance (Run time in seconds, Rate Normalized to Config. K-3a)			
	(MHz)	(MHz)		PCI disc. = 5 clocks		PCI disc. = 8 clocks	
				Run time	Rate	Run time	Rate
G-1	300	100 (3:1)	-	9.39	1.226	9.71	1.189
G-2a	300	66 (9:2)	-	11.47	1.003	11.79	0.980
G-2b			Yes	8.60	1.338	8.92	1.295
G-3a	266	66 (4:1)	-	11.98	0.961	12.30	0.939
G-3b			Yes	9.07	1.269	9.39	1.230
G-4	250	100 (5:2)	-	10.16	1.133	10.48	1.102
G-5	250	83 (3:1)	-	10.99	1.047	11.31	1.021
G-6a	250	63 (4:1)	-	12.65	0.910	12.97	0.891
G-6b			Yes	9.57	1.203	9.89	1.168
G-7a	200	66 (3:1)	-	13.39	0.860	13.71	0.842
G-7b			Yes	10.42	1.105	10.75	1.074

Lower run time means higher performance. Normalized rate is inverse of run time, so higher rate means higher performance

MPC603e + MPC106 configurations feature 33 MHz, 32-bit PCI bus

L2 cache timing is 3-1-1-1

PCI target disconnects occur every 32 bytes

Configurations G-1, G-4, and G-5 will not support an L2 cache because 60x bus is greater than 66 MHz

No 250 MHz parts are currently available, so the 250 MHz configurations are 266 MHz parts run at the lower frequency

Configurations G-1 and G-4 do not correspond to announced parts and are used for comparative purposes only

The MPC603e + MPC106 configurations in Table 3 are similar to the MPC8240 configurations in Table 2, except that the PCI bus speed is fixed at 33 MHz. In addition, the configurations with 66 MHz or lower memory bus speed are modeled with an optional L2 cache. Again, the run time was computed for the two PCI disconnect penalties, and the rate of execution was calculated by taking the inverse of the run time and normalizing to configuration K-3a (from Table 2)[1].

The results in Table 2 and Table 3 are presented graphically in Figure 1 and Figure 2. Figure 1 presents the normalized performance (rates of execution) for PCI disconnect = 5, and Figure 2 presents the normalized performance for PCI disconnect = 8. For each of these figures, the left half represents the MPC8240 configurations (Table 2), and the right half represents the MPC603e + MPC106 configurations (Table 3). Each MPC8240 configuration (K-1 through K-6) features two bars representing the 33-MHz PCI (a) and 66-MHz PCI (b) versions (66 MHz is longer). Each MPC603e + MPC106 configuration (G-1 through G-7) presents the no-L2 cache ("a") and, where possible, the with-L2 cache ("b") versions.

For example, in Figure 1, the configuration K-3a features a 266-MHz processor clock, 66-MHz memory bus

[1] For example, take G-3a. For PCI disconnect = 5, its run time is 11.98 seconds (for K-3a it is 11.51). Dividing 1/11.98 by 1/11.51 yields 0.961. For PCI disconnect = 8, dividing 1/12.30 by 1/11.55 yields 0.939.

clock, and 33-MHz PCI clock, and its bar has length 1.000. Configuration K-3b is the same except for a 66-MHz PCI clock, and its bar has length 1.042.

Longer bars mean higher performance. Note that the Y-axis (performance improvement) is centered around the normalized configuration (value = 1), so a bar that is twice as long in these figures does not mean the configuration runs twice as fast. For example, in Figure 1, G-7b runs about 10% faster than K-3a, and G-7a runs about 15% slower than K-3a. G-7b, by adding an L2 cache, runs about 30% faster than G-7a.

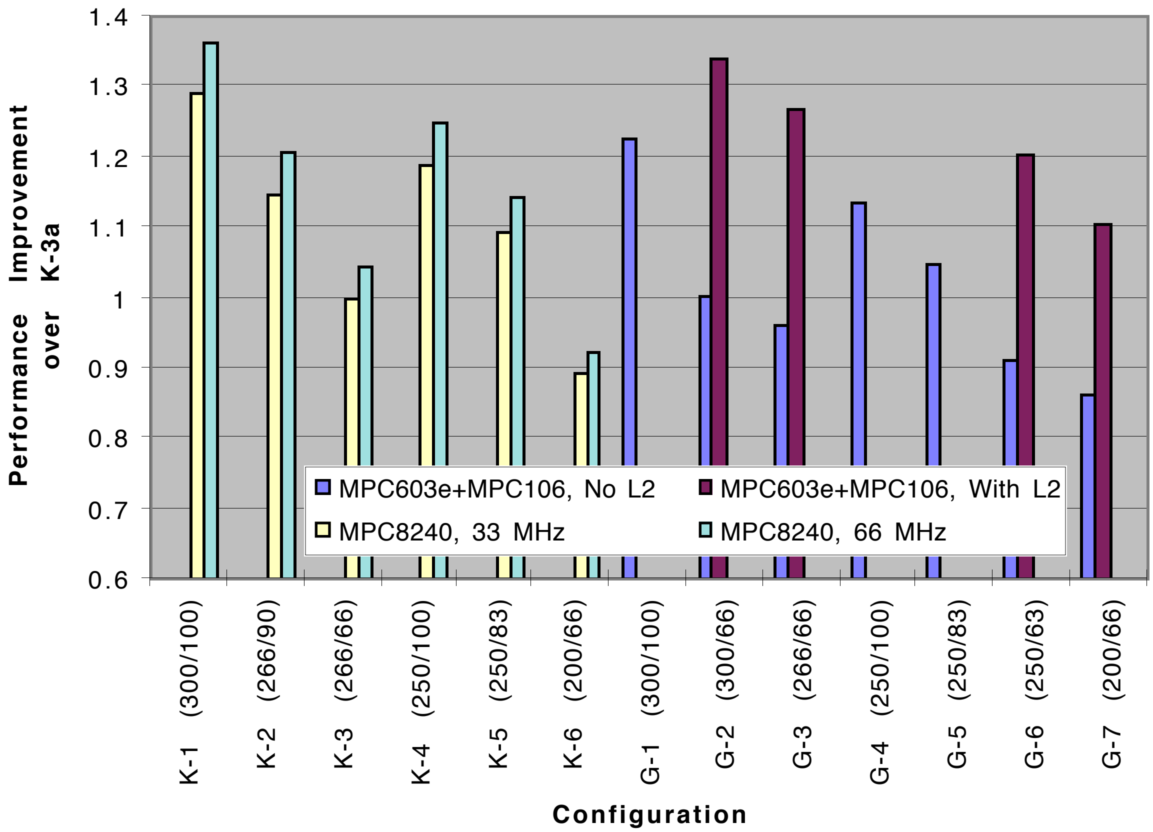

Figure 1. Relative System Performance for PCI Disconnect = 5 (Normalized to Configuration K-3a)

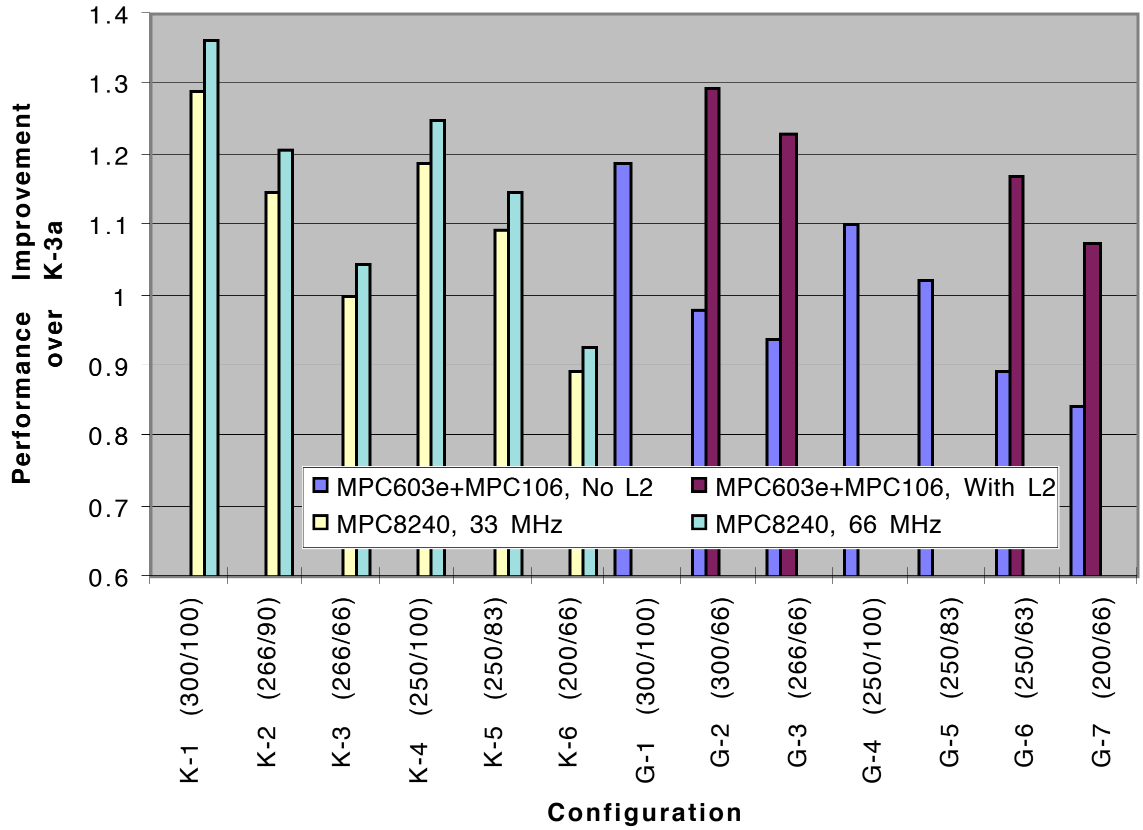

Figure 2. Relative System Performance for PCI Disconnect = 8 (Normalized to Configuration K-3a)

Several items should be noted from this data:

- The workload modeled is memory-bound, not compute-bound, so changing memory bus speed, PCI bus speed, and L2 configuration has more effect than changing core processor speed. For example, moving from K-1 to K-4 (processor 300 MHz -> 250 MHz) does not have as much impact as moving from K-2 to K-3 (memory 90 MHz -> 66 MHz). Similarly, moving from G-2 to G-7 (processor 300 MHz -> 200 MHz) has less effect than moving from G-1 to G-2 (memory 100 MHz -> 66 MHz).
- In addition, the workload modeled utilizes the memory bus more than the PCI bus, so varying the memory speed has more effect than varying the PCI bus speed (for the MPC8240 configurations). This is also why adding an L2 cache for the MPC603e + MPC106 configurations has a much larger impact than moving from 33 MHz to 66 MHz PCI for the MPC8240 configurations.
- On the other hand, the benefit of adding an L2 cache is reduced when one considers the fact that it limits memory bus speed. For example, compare K-4 with G-6b. Both are the fastest configurations modeled for a 250 MHz processor. Even with an L2 cache, G-6b is just comparable in speed to K-4 with PCI disconnect = 5. The MPC8240 with 66 MHz PCI (K-4b) is slightly faster. And with PCI disconnect = 8, even the MPC8240 with 33 MHz PCI (K-4a) beats G-6b. Comparing the fastest 266 MHz processor configurations (K-2 and G-3b) does show the MPC603e + MPC106+L2 configuration leading. The cost and increased board space of adding an L2, however, must be balanced against simply using an MPC8240.
- For the MPC8240 configurations, changing PCI disconnect penalty has little effect on relative performance (since PCI data streaming minimizes the effect of the disconnect penalty), so the MPC8240 bars are very similar between Figure 1 and Figure 2. For the MPC603e + MPC106

configurations, changing PCI disconnect penalty has a greater effect, with higher disconnect penalty favoring MPC8240 configurations (so the Figure 2 MPC603e + MPC106 bars are shorter than those in Figure 1).

The remaining figures present data only for PCI disconnect = 5, the most conservative case.

2.2 PCI Transaction Size

One factor influencing the effectiveness of PCI data streaming for the MPC8240 configurations is the typical transaction size. This transaction size is determined by the PCI devices and the PCI address access pattern. Recall that Table 2 assumed a disconnect every 256 bytes. Figure 3 shows how varying the MPC8240 PCI transaction size affects the performance improvement of the MPC8240 over the MPC603e + MPC106 combination, for PCI disconnect = 5.

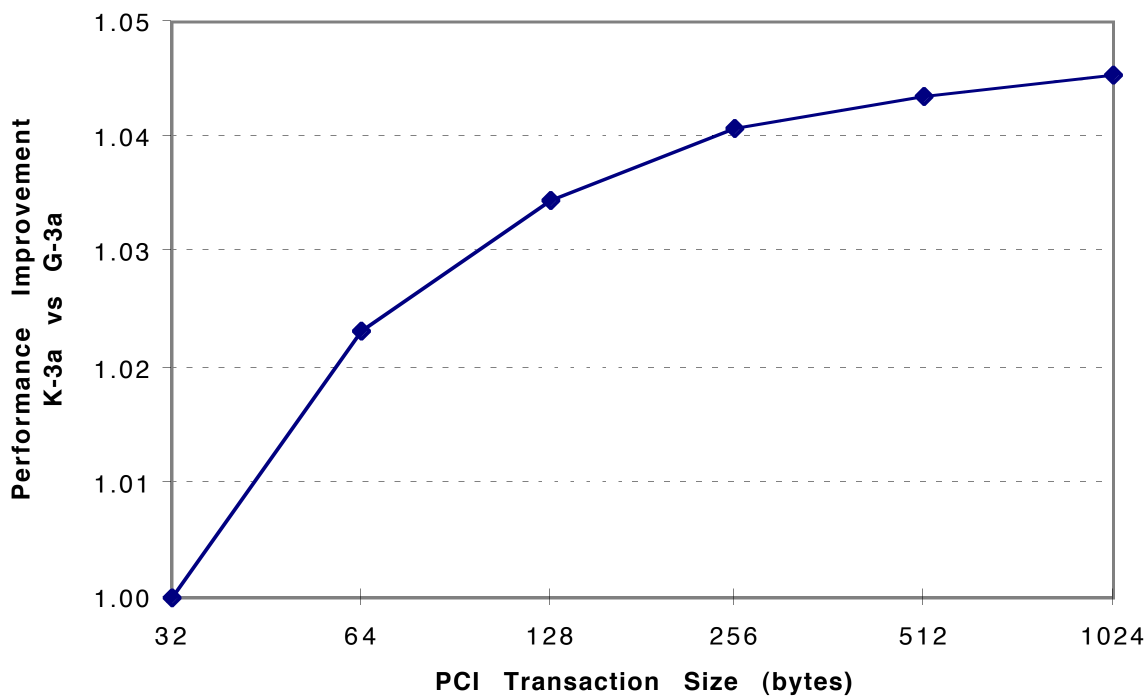

Figure 3. Effect of Varying PCI Transaction Size on Performance Improvement (Configuration K-3a over Configuration G-3a)

Note that most of the speedup occurs by the 256-byte mark, which is close to full streaming (no disconnects at all). Very little additional performance improvement is achieved for larger PCI device buffer sizes.

2.3 PCI Bus Utilization

Another factor influencing the effectiveness of PCI streaming is the amount of traffic that is streamed on the PCI bus. Bus utilization is increased by raising the number of page writes relative to the number of workload instructions executed, thereby increasing the ratio of PCI traffic to computation. Figure 4 shows how increasing bus utilization will increase performance improvement due to streaming, for K-3a and K-3b over G-3a, and PCI disconnect = 5.

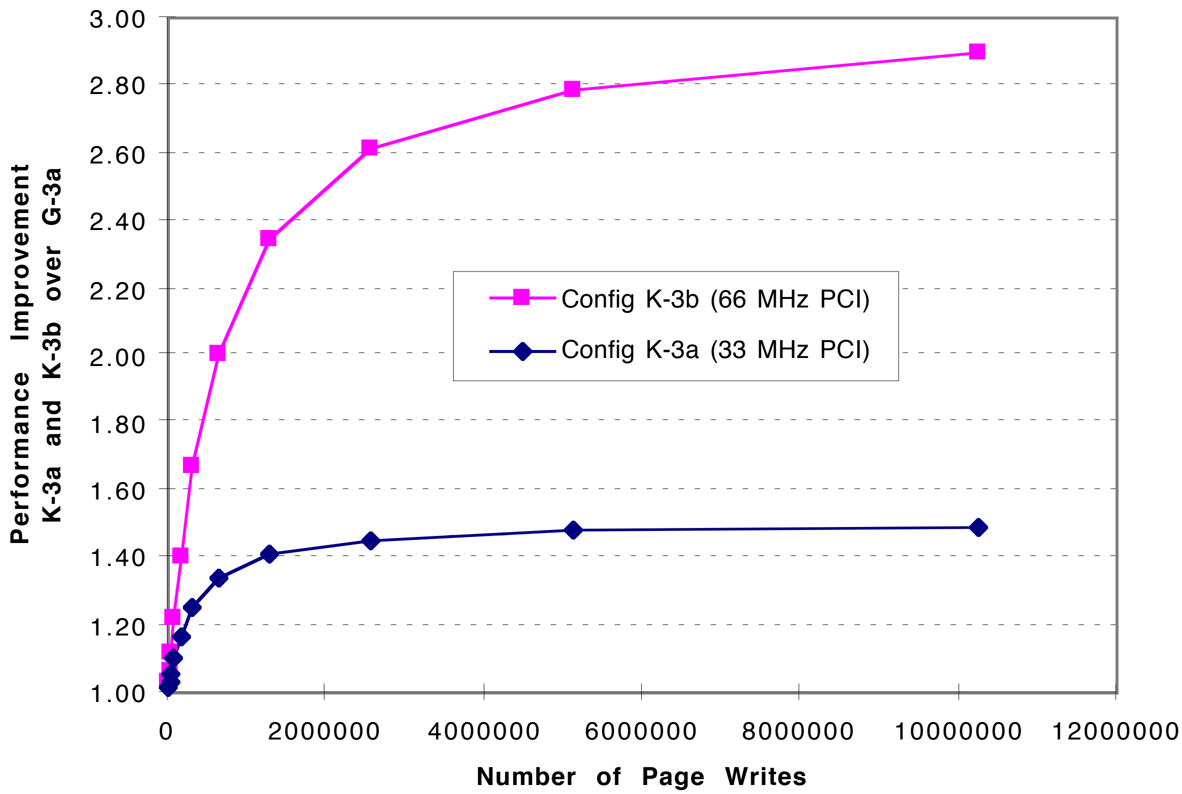

Figure 4. Effect of Varying PCI Bus Utilization (Number of Page Writes) on Performance Improvement (Configurations K-3a and K-3b over Configuration G-3a)

As the PCI bus traffic increases, performance improvement due to PCI data streaming increases as well. Note that as the PCI bus becomes saturated, performance improvement levels off.

Figure 5 presents the same data in a different way. It is identical to Figure 4, except that the X-axis is scaled differently. The number of page writes is converted to the bus utilization for configuration G-3a. Note that these bus utilization numbers do not represent bus utilization figures for configurations K-3a or K-3b.

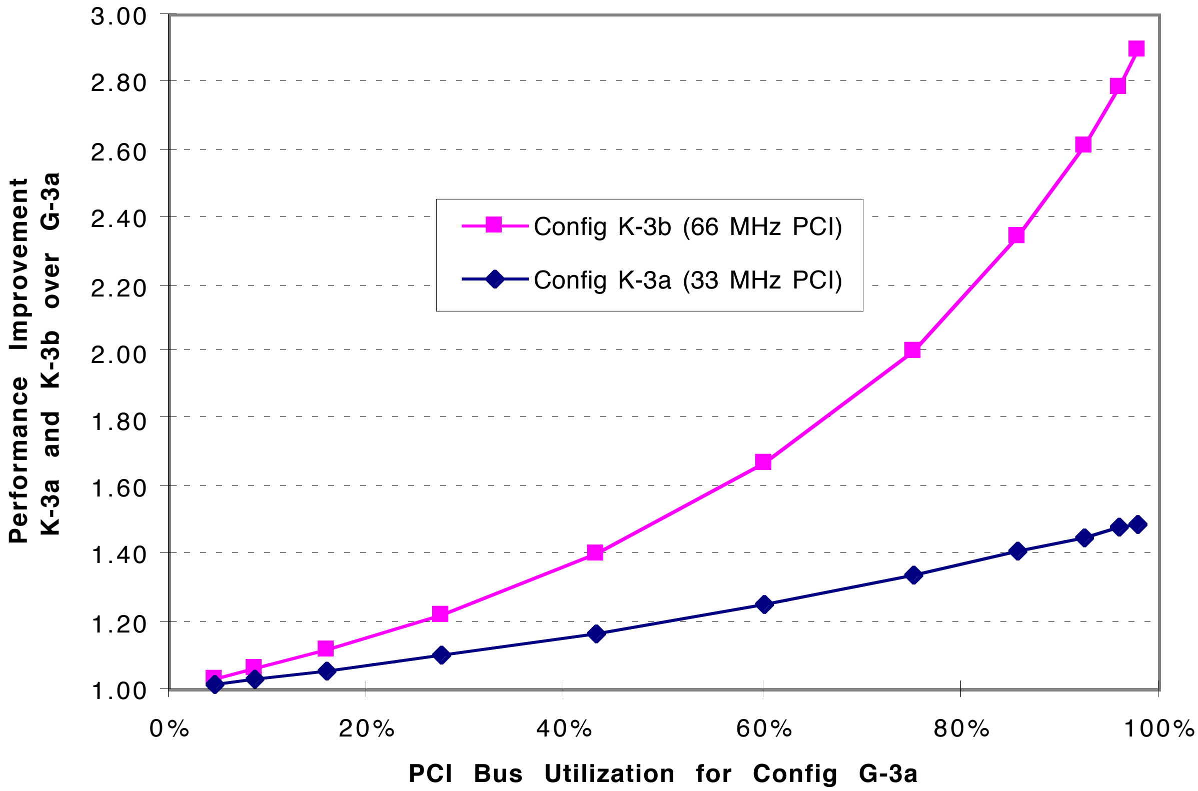

Figure 5. Effect of Varying PCI Bus Utilization on Performance Improvement (Configurations K-3a and K-3b over Configuration G-3a)

As shown in Figure 5, the workloads simulated in Table 2 and Table 3, which are based on observed tests, have a low average bus utilization, and therefore show little improvement due to streaming. However, as the number of page writes increases, performance improvement also increases. For 33 MHz PCI, performance improvement increases linearly, while performance improvement increases even faster for 66 MHz PCI.

Figure 6 and Figure 7 illustrate this in another way, by showing the data transfer rate for comparable configurations K-3a, K-3b, and G-3a, as the number of PCI page writes varies, for PCI disconnect = 5.

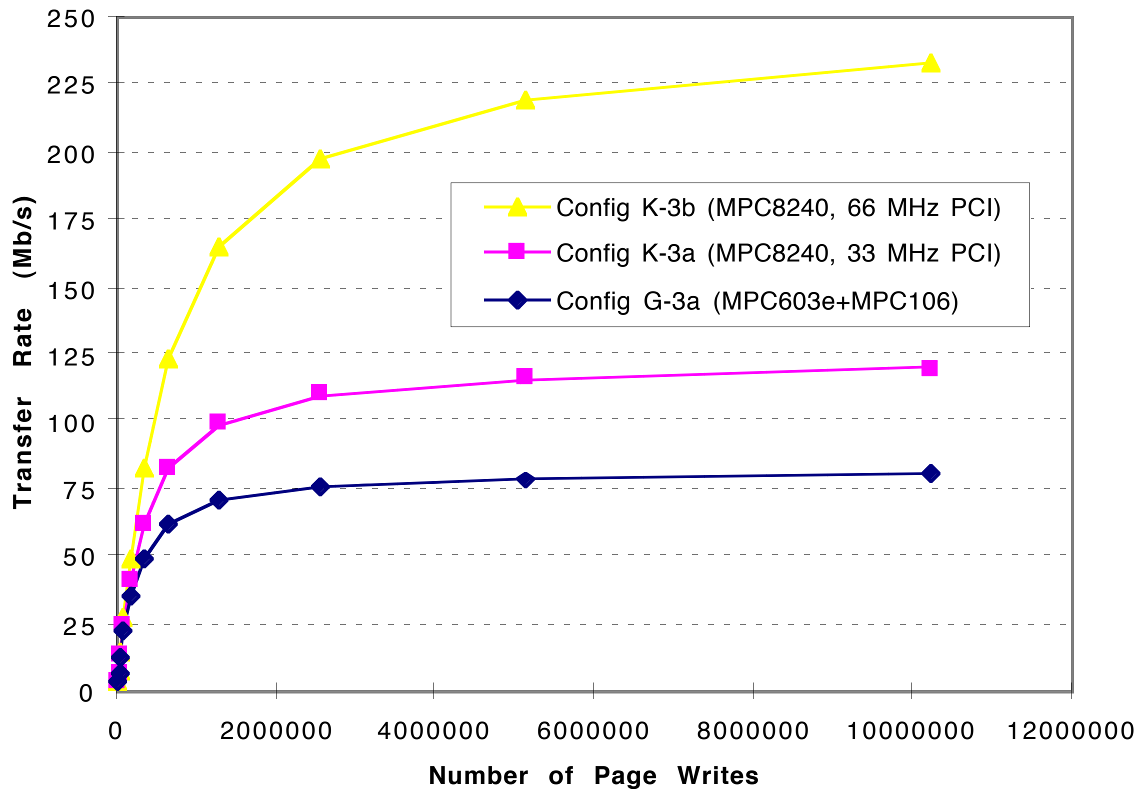

Figure 6. Effect of Varying PCI Bus Utilization (Number of Page Writes) on Data Transfer Rate (Configurations K-3a and K-3b over Configuration G-3a)

Figure 6 shows the maximum transfer rate approached asymptotically as the number of page writes increases. For an MPC603e + MPC106 system, up to 81 Mb/s can be transferred, whereas for the MPC8240 the maximum transfer rate is 122 Mbytes per second for 33 MHz PCI, and 244 Mb/s for 66 MHz PCI.

The theoretical maximum transfer rate using the analytical model, as PCI bus utilization approaches 100%, is:

Bus speed × Bus size × t/(t+d)

where

Bus speed = 33 MHz

Bus size = 32 bits (4 bytes)

t is the number of bus clocks between disconnects

d is the disconnect penalty = 5 PCI bus clocks

The MPC8240 has t = 64 (256-byte transaction size÷4 bytes/beat). Without PCI streaming, the MPC106 has t = 8 (32-byte transaction size). The theoretical maximum transfer rates are therefore:

MPC8240 - 66	66 × 4 × 64/69 = 244 Mb/s
MPC8240 - 33	33 × 4 × 64/69 = 122 Mb/s
MPC106	33 × 4 × 8/13 = 81 Mb/s

This assumes no contention from other PCI devices.

These numbers do not take into account any other system considerations, such as concurrent memory accesses from the CPU or other internal delays.

Figure 7 is identical to Figure 6, except that the X-axis is scaled differently. The number of page writes is converted to the bus utilization for configuration G-3a. Note that these bus utilization numbers do not represent bus utilization figures for configurations K-3a or K-3b.

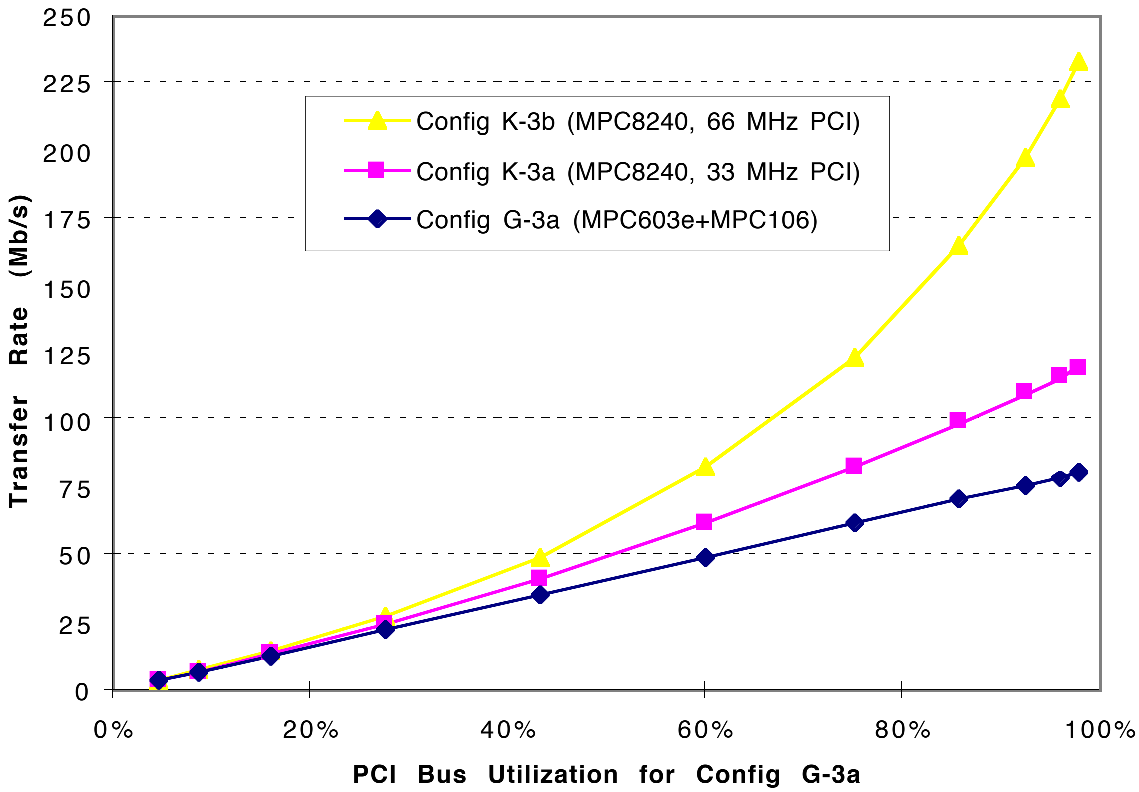

Figure 7. Effect of Varying PCI Bus Utilization on Data Transfer Rate (Configurations K-3a and K-3b over Configuration G-3a)

Figure 7 also shows the maximum transfer rate as PCI bus utilization for G-3a approaches 100%. For periods of low PCI bus activity, there may be little improvement due to PCI streaming. However, for periods with high PCI bus activity, there should be marked improvement in the data transfer rate (as shown by the widening gap between the K-3a and K-3b configurations and the G-3a configuration, since the disconnect penalty begins to have more of an impact on throughput.

Part 3 Conclusion

Although the MPC8240 and an MPC603e + MPC106 combination are similar in many respects, architectural differences between the two can lead to measurable performance differences. The MPC8240 supports higher memory and PCI bus speeds, as well as PCI data streaming, while the MPC106 supports an L2 cache.

For the workloads modeled, the MPC8240 in general can provide better performance for comparable system configurations, particularly if there is heavy PCI bus traffic. The performance of an MPC106 system can be significantly improved by adding an L2 cache, making it comparable in speed to an MPC8240 system, though at a higher cost.

Motorola Literature Distribution Centers:

USA/EUROPE: Motorola Literature Distribution; P.O. Box 5405; Denver, Colorado 80217; Tel.: 1-800-441-2447 or 1-303-675-2140;
World Wide Web Address: http://ldc.nmd.com/

JAPAN: Nippon Motorola Ltd SPD, Strategic Planning Office 4-32-1, Nishi-Gotanda Shinagawa-ku, Tokyo 141, Japan Tel.: 81-3-5487-8488

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd Silicon Harbour Centre 2, Dai King Street Tai Po Industrial Estate Tai Po, New Territories, Hong Kong

Mfax™: RMFAX0@email.sps.mot.com; TOUCHTONE 1-602-244-6609; US & Canada ONLY (800) 774-1848;
World Wide Web Address: http://sps.motorola.com/mfax

INTERNET: http://motorola.com/sps

Technical Information: Motorola Inc. SPS Customer Support Center 1-800-521-6274; electronic mail address: crc@wmkmail.sps.mot.com.

Document Comments: FAX (512) 895-2638, Attn: RISC Applications Engineering.

World Wide Web Addresses: http://www.motorola.com/PowerPC
http://www.motorola.com/netcomm
http://www.motorola.com/HPESD

MOTOROLA