

Power Architecture™ Demystified

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1 Introduction

Formerly only found in high-end automotive application areas such as powertrain and braking, Freescale has succeeded in producing scaled Power Architecture™ cores for a complete spectrum of automotive applications ranging into the body electronics space. This document demystifies what Freescale Power Architecture offers to users more familiar with other Freescale microcontrollers or competitors' solutions more commonly associated with the automotive body electronics application space.

2 History

Power Architecture (formerly known as PowerPC) is a RISC microprocessor architecture created by the 1991 Apple-IBM-Motorola alliance, known as AIM. Originally intended for personal computers, Power Architecture CPUs have become popular embedded and

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high-performance processors and are extremely common in automotive powertrain applications in the MPC5XX family and more recently the MPC55XX family.

3 Power Architecture

The Power Architecture standard specifies a common instruction set architecture (ISA), (allowing anyone to design and fabricate Power Architecture processors) that run the same code. The Power Architecture specifies both 32-bit and 64-bit data paths. Some implementations are 32-bit, and higher-performance implementations are 64-bit. A Power Architecture core has 32 general-purpose (integer) registers (32- or 64-bit) and 32 floating point (IEEE standard 64-bit) registers.

The Power Architecture is a reduced instruction set computer (RISC) architecture, because most instructions execute in a single cycle and typically perform a single operation, such as loading storage to a register, or storing a register to memory.

The Power Architecture is divided into three levels, or books. By segmenting the architecture in this way, code compatibility can be maintained across implementations while leaving room for implementations to choose levels of complexity for price/performance trade-offs. The levels are:

- **Book I. User instruction set architecture**
 Defines the base set of user instructions and registers common to all power implementations. These are non-privileged instructions used by most programs.
- **Book II. Virtual environment architecture**
 Defines additional user-level functionality outside the normal application software requirements, such as cache management, atomic operations, and user-level timer support. Although these operations are also non-privileged, a program typically accesses the function via an operating system call.
- **Book III. Operating environment architecture**
 Defines the privileged operations required and used at the operating system level. These include functions for memory management, exception vector processing, privileged register access, and privileged timer access. Direct hardware support for a variety of system services and capabilities are specified in Book III.

More recently, Freescale was instrumental in the development of:

- **Book VLE—Variable length encoded instruction architecture**
 This defines alternative instructions and definitions intended for higher instruction density and reduced memory requirements.

Because of the development of the original Power Architecture, deviations have focused on specific market segments. Today, there are two active branches of the Power Architecture family tree, Power AS Architecture and Power Book E Architecture. The Power AS Architecture is defined by IBM to meet the special needs of its server product family. The Power Book E Architecture, referred to as Book E, is a collaboration between IBM and Freescale for special requirements of the embedded market. Major differences from the original Power Architecture adopted in Power AS and extensions adopted in Book E reside mainly in the area of Book III.

4 Power.org

The Power.org consortium announced in 2004, is a premier open organization for developing, enabling, and promoting Power Architecture technology and specifications.

The Power.org community's objectives are:

- Develop open standards and specifications
- Validate implementations
- Drive adoption of Power Architecture technology
- Enable a complete design and manufacturing infrastructure that resolves many of the technology and business issues hindering hardware development and innovation.

Within Power.org, the Power Architecture advisory council (PAAC), consisting of IBM and Freescale Semiconductor, is responsible for managing the architectural roadmap and alignment for Power Architecture technology. The goal is to provide a seamless, compatible instruction set architecture designed to accommodate platforms scaling from low-cost, high-volume devices to high-performance applications such as automotive powertrain and transmission systems.

5 Freescale Processor Cores

Freescale Semiconductor has introduced an advanced line of 32-bit microcontrollers, the MPC55XX Family, to the mass market. Containing a Power Architecture core, the MPC55XX families of microcontrollers provide the functionality and flexibility necessary for a wide range of automotive and industrial control applications.

All of the MPC55XX family microcontrollers feature cores from the Freescale e200z processor family. This is a set of CPU cores that implement low-cost versions of the Power Architecture that are Book E compliant. The e200z processors are designed for deeply embedded control applications that require low-cost solutions rather than maximum performance. Freescale processors also feature the VLE capability allowing more compact code to be developed at a minimal impact on performance.

Table 1. MPC55XX Core Comparison

MPC55XX Families	MPC560X	MPC5516E/G/S	MPC5533, MPC5534	MPC5565, MPC5567	MPC5566
Core	Power e200z0	Power e200z1	Power e200z3	Power e200z6	Power e200z6
VLE	Yes	Yes	Yes	Yes	Yes
SIMD	No	No	Yes	Yes	Yes
Floating point	No	No	Single precision	Single precision	Single precision
Floating pointing MAC	No	No	Yes	Yes	Yes
Integer MACs	No	No	Yes	Yes	Yes
MMU size (TLBs)	N/A	8	16	32	32

Table 1. MPC55XX Core Comparison (continued)

MPC55XX Families	MPC560X	MPC5516E/G/S	MPC5533, MPC5534	MPC5565, MPC5567	MPC5566
Address bus width	32	32	32	32	32
Data bus width	32	64	64	64	64
Cache size	N/A	N/A	N/A	2 way x 4 Kbytes	8 way x 4 Kbytes
Debug port	Nexus 2+	Nexus 2+	Nexus 3+	Nexus 3+	Nexus 3+

Table 1 shows a comparison of all of the e200z cores currently being offered by Freescale, and the microcontroller devices they can be found on. An explanation of terms is found in Appendix A.

5.1 e200z1 Core

The first members of the e200z family of cores are targeted at higher end automotive applications areas such as powertrain. They contain many advanced features, such as a cache and floating point units and DSP capabilities.

More recently, Freescale has produced smaller cores aimed at lower-end automotive body applications. Although these cores offer less performance and features than the earlier cores, they continue to offer performance greater than most competitive 32-bit cores. This allows a migration upwards in performance if an application requires more throughput at a later development stage.

The main e200z core targeted at the automotive body space is the e200z1.

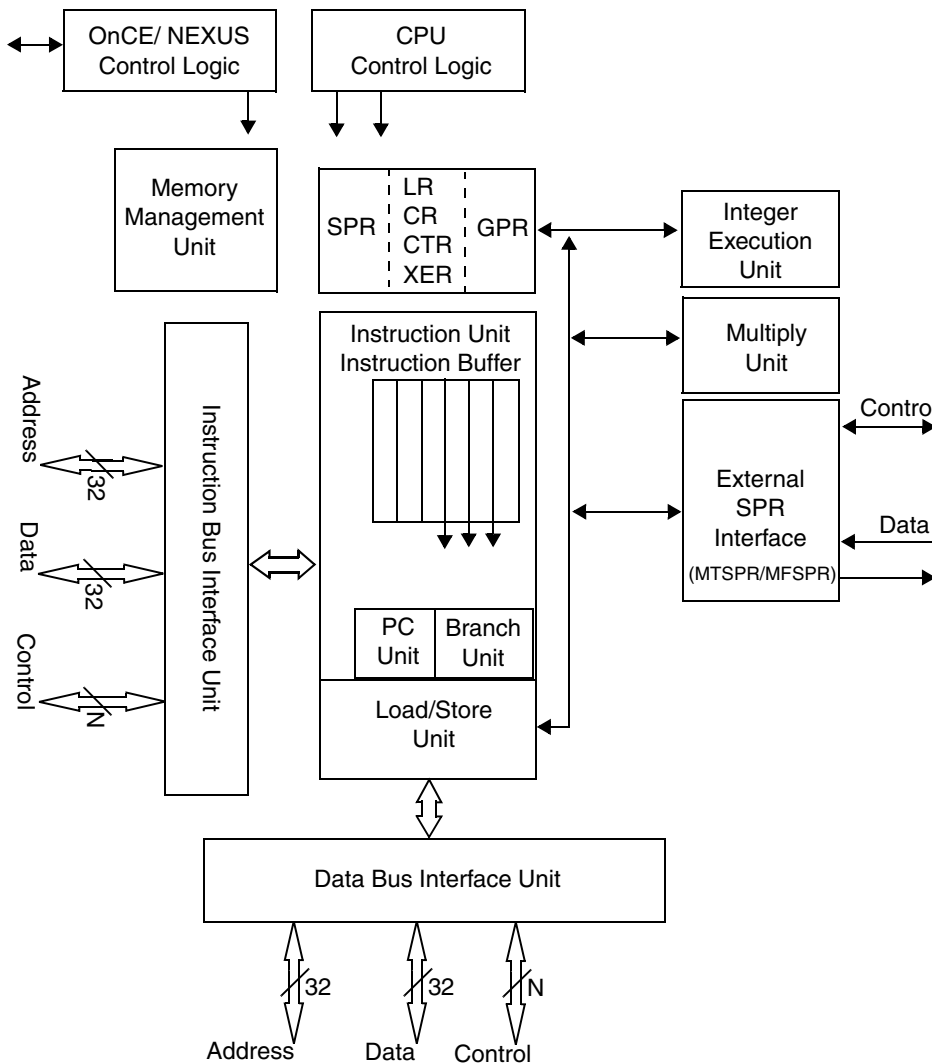


Figure 1. e200z1 Core Block Diagram

The e200z1 core integrates an integer execution unit, branch control unit, instruction fetch and load/store units, and a multi-ported register file capable of sustaining three read and two write operations per clock. Most integer instructions execute in a single clock cycle. Branch target pre-fetching is performed by the branch unit to allow single-cycle branches in the case of a successful prediction.

The core is a single-issue, 32-bit Power Architecture, embedded category compliant design with 32 x 32-bit general-purpose registers (GPRs). Power Architecture floating point category instructions are not supported in hardware, but are trapped and may be emulated by software. All arithmetic instructions that execute in the e200 cores operate on data in the GPRs.

In the Power Architecture base instruction set, the core also implements the variable-length encoding (VLE) category, providing improved code density.

VLE and regular power code can be mixed freely in an application on a flash page size access basis. Benchmarking has shown that with typical code, VLE code is generally around 30% smaller than regular power code suffering only around a 5% performance reduction.

5.2 Nexus Debug

All of the Freescale e200z cores feature a Nexus debug interface of some degree. The Nexus interface is an open industry standard that provides a general-purpose interface for the software development and debug of embedded processors. The functionality and feature set provided by Nexus is defined by certain class levels as described below.

The Nexus standard class 1 is essentially a standard JTAG interface. This provides:

- Standard interface
- High speed
- Run control
- Flexible breakpoint and watch-point set-up

Class 2 adds:

- Full duplex communication
- Real-time non-intrusive program trace

Class 2+ adds:

- Read/write access to memory locations while CPU is running

Class 3+ adds:

- Real-time non-intrusive data trace.

As seen in [Table 1](#), the higher end e200z cores feature Nexus level 3+, whereas the lower-end cores such as the e200z1 feature a more cost-effective but still a powerful Nexus level 2+ and still enables users to perform real-time instruction trace in addition to the standard static functions defined in level 1 of the Nexus standard.

5.3 MPC5510 Family

The first family of Freescale microcontrollers to feature the lower-end e200z cores targeted at the automotive body electronics market is the MPC5510 family.

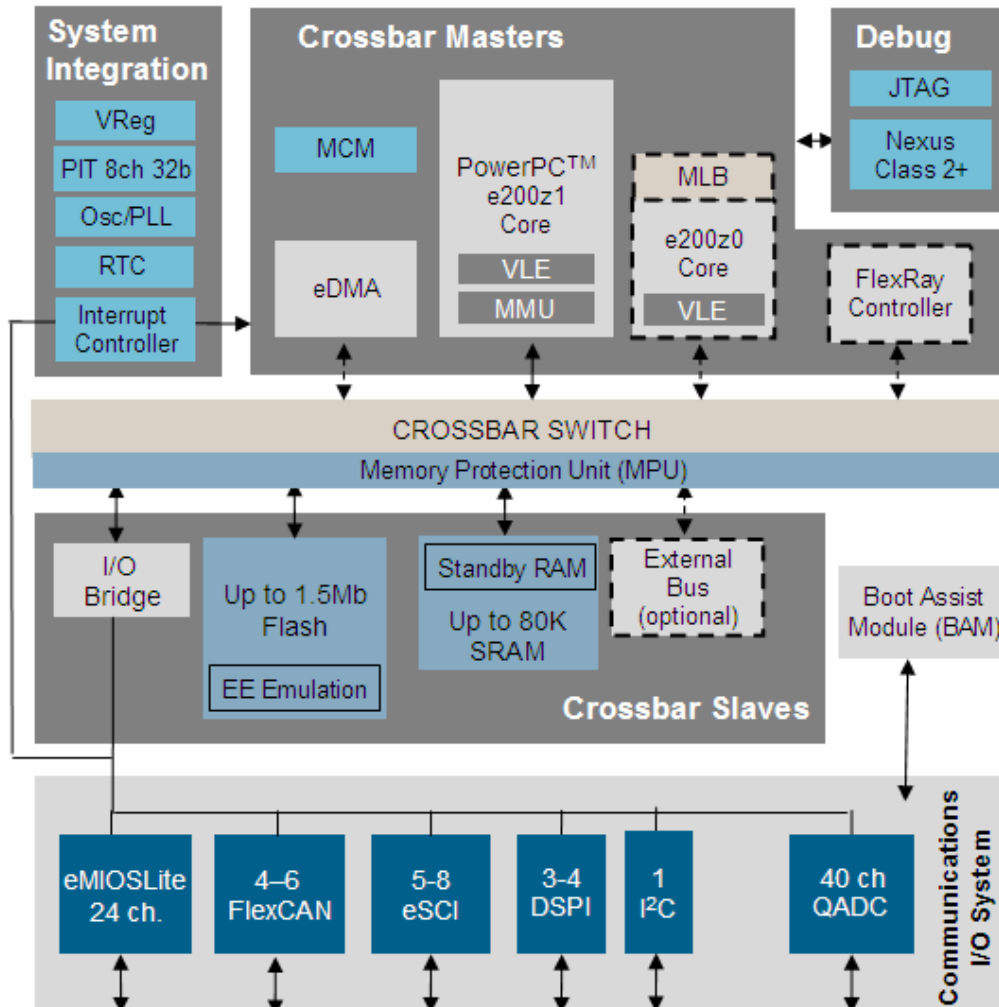


Figure 2. MPC5510 Family Architecture

Figure 2 shows a typical family member architecture and a typical mix of peripheral modules.

5.4 Key Architecture Points

Some key architectural points are discussed in the following subsections.

5.4.1 Standard Platform

All microcontrollers built with an e200z core are built on a version of Freescale's standard product platform. This effectively allows a production of core agnostic design implementation. This enables maximum re-use and allows for fast derivative products.

5.4.2 eDMA

The eDMA on the MPC5510 family provides a powerful method of transferring data between I/O, peripherals, and on-chip memory. After set up, if required, the data transfers can occur totally automatically without any intervention from the core, leaving more processing bandwidth available to perform other tasks. The eDMA on the MPC5510 family is a 16-channel implementation that includes a DMA multiplexer. This allows total flexibility to assign the 16 channels to any of the DMA-enabled peripherals as required.

5.4.3 Crossbar Switch

The on-chip memory system is interconnected through a module called the crossbar switch. This provides appropriate routing of address, data, and control signals between devices called bus masters and peripherals called bus slaves. A bus master can initiate a bus transaction by outputting address and control signals, a slave can only respond to control signals. Essentially, the crossbar switch acts like a bus multiplexer that routes data movement between different masters and slaves.

Key points that make the crossbar switch important in the architecture are:

- The crossbar switch supports multiple concurrent transfers between mutually exclusive master-slave paths. For example, the core can fetch instructions from program memory in the same cycles that the eDMA is writing variables to RAM.
- The crossbar switch contains programmable prioritization hardware to arbitrate transfers initiated by two or more bus masters to the same slave.

This scheme allows for an efficient, highly parallel architecture, enabling maximum throughput to be achieved.

6 e200z0 Core

Another powerful feature of the MPC5516 family is the presence of an optional second core, the e200z0, acting as an I/O processor. This core is a reduced version of the main e200z1 core that runs only VLE instructions. Due to a virtual dual-port flash access scheme, the main core and the e200z0 simultaneously execute code from program memory. This second core is intended to manage I/O processing or gateway functions between communication networks, but can be used for any task assigned to the main core to reduce loading on the main core and provide additional throughput capability.

7 Conclusion

The MPC55xx family of microcontrollers from Freescale feature highly efficient Power Architecture e200z cores. These efficient devices feature parallel processing, excellent code density, sophisticated peripherals and multiple package and memory options.

Furthermore, the MPC5510 family offers the low-power features essential in meeting the requirements of the highly power-sensitive body electronics market, offering performance that exceeds many competitive offers.

Appendix A Explanation of Terminology

Variable length encoding (VLE)

VLE is an extension to the existing 32-bit Power Architecture Book E instruction set designed to allow more compact code densities to be achieved with a minimal impact on performance. The instruction set comprises both 16-bit and 32-bit instructions. VLE and regular power code can be mixed freely in an application. Benchmarking has shown that with typical code, VLE code is generally around 30% smaller than regular Power Architecture code and suffers around a 5% performance reduction.

Multiply accumulate unit (MAC)

A MAC-unit consists of a multiplier implemented in combinational logic followed by an adder and an accumulator register that stores the result if clocked.

Single instruction multiple data (SIMD)

Closely associated with the signal processing engine (SPE) that provides a number of DSP type functions. SIMD instructions can operate on multiple sets of input data and generate multiple output results.

Memory management unit (MMU)

MMUs are often used to implement a virtual memory system that makes a unit appear to have more physical RAM memory than it actually does. Additionally, MMUs are used to partition and protect physical memory so that each task may execute and access data only to those memory locations that are allocated to it. If any task tried to access another code or data space, the MMU generally generates an exception and prevents the errant task from corrupting data or execution of the other task.

Translation lookaside buffer (TLB)

A TLB is essentially an element within the MMU that contains the translation information for a particular area of memory. The MMU uses the TLB information to translate a 32-bit effective address to a 32-bit real address. To generate the real address, the effective address is first split into a page number and an offset into the page. The bits that define the page number are then compared in parallel with every valid TLB entry. If a hit occurs on a single entry, the contents of the entry are then concatenated with the page offset of the original effective address to produce the real address.

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