

QorIQ Communications Platforms

QorIQ Advanced Multiprocessing (AMP) Series



freescale.com

QorIQ Advanced Multiprocessing (AMP) Series Delivers More than Moore

Overview

Moore's Law states that the number of transistors that can be placed inexpensively on an integrated circuit doubles approximately every two years. Today's network bandwidth challenges Moore's Law—traffic doubles every 12 months as the demand for social media and rich content grows. This insatiable appetite for connectivity will continue to push the industry for solutions that deliver performance beyond Moore's Law, providing improved efficiency and lower operating costs.

Freescale's QorIQ communications platforms provide developers with a series of multicore processors based on high-performance Power Architecture® cores. These solutions meet the processing requirements of modern infrastructure applications that need robust real-time point to point communication. QorIQ processors provide an evolutionary step up that preserves legacy investments on earlier generation PowerQUICC communications processors. The workhorse of the QorIQ P series is the P4080 processor with eight integrated e500mc cores, operating at frequencies up to 1.5 GHz, combined with high-performance data path acceleration (DPAA) logic, and network and peripheral bus interfaces in a 45 nm implementation. Freescale's new QorIQ Advanced Multiprocessing (AMP) series pushes the compute and energy performance envelope beyond the P4080 processor such that its performance capacity exceeds that which Moore's Law predicts.

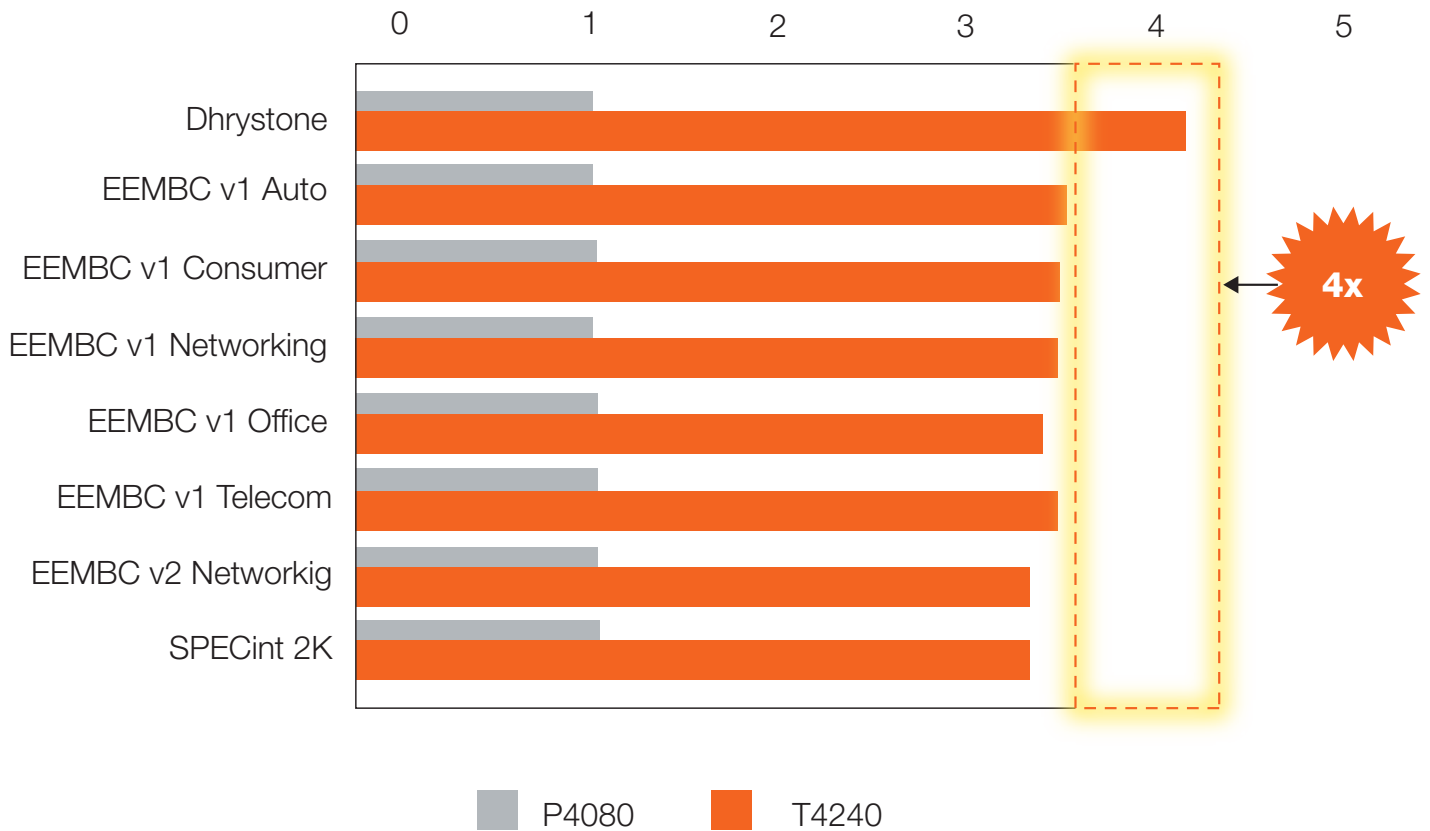
By taking advantage of multiple innovations that work together, QorIQ AMP processors are able to improve software developer productivity while delivering a better than four times improvement* in application and core processing performance and also delivering a better than two times improvement in power efficiency.

Key innovations that enable an improvement in application and core processing performance more than four times that of the P4080 device include a new advanced multi-threaded e6500 core as well as improvements in the high-performance memory, interconnects and application-specific accelerators—all implemented in a 28 nm process.

Energy efficiency is improved to more than twice that of previous-generation QorIQ devices through advanced power management, such as the inclusion of cascading power management for core and system power management, special attention to multicore clustering optimizations and aggressive use of hardware acceleration.

Freescale's new QorIQ AMP series pushes the compute and energy performance envelope beyond the P4080 processor such that its performance capacity exceeds that which Moore's Law predicts.

Application Performance: P4080 and T4240 Processors



QorIQ P4080 Processor

The new advanced multi-threaded e6500 core is based on a 64-bit architecture sporting larger L1 caches and a 2x 2-way superscalar execution engine that can operate at up to 2.0 GHz—a 1.3x frequency improvement over the e500mc in the P4080.

The 64-bit instruction set architecture (ISA) is Power Architecture V2.06-compliant and includes 22 new debug features. Register settings allow developers to use 32- or 64-bit mode. A hybrid 32-bit mode supports e500 legacy software and a smooth transition to the 64-bit architecture. The e6500 core supports a dual-thread capability that enables each core to act as two virtual cores. Each thread is supported with a separate front end, branch unit and load/store unit (LSU) share execution units (AltiVec technology).

Each e6500 core can address up to 1 TB of memory space and supports up to a 512 KB L2 cache. The first product released in the AMP series will be the T4240, which

comprises of 12 dual-threaded cores (24 virtual cores) where each dual-threaded e6500 core can be clustered in groups of four cores that share a common 2 MB L2 cache. The CoreNet cache-coherent fabric scales to support up to eight multiple clusters in a single system.

Optimizations in the memory architecture yield a 2.4x improvement in the memory bandwidth and a 1.6x improvement for the double data rate (DDR) clock frequency over previous-generation QorIQ processors.

The e6500 core includes several features to support hardware-assisted virtualization, such as an extra privilege level for hypervisor support. Hardware support for logical to real address translation (LRAT) considerably reduces hypervisor overhead. A new logical partition ID field enables developers to identify partitions for virtual to real address translation. I/O MMU-like capabilities were added to the system to prevent data

corruption for DMA or I/O. Network bound interfaces are virtualized, and virtualization of hardware blocks is supported via the QMan for best effort virtualization.

The e6500 core includes a 192 GFLOPS AltiVec execution unit that is able to improve the performance of algorithms such as the Scheduler Algorithm by a factor of four over a C-optimized implementation on the P4080. AltiVec technology is a vector or single instruction multiple data (SIMD) architecture that allows the simultaneous processing of multiple data items in parallel.

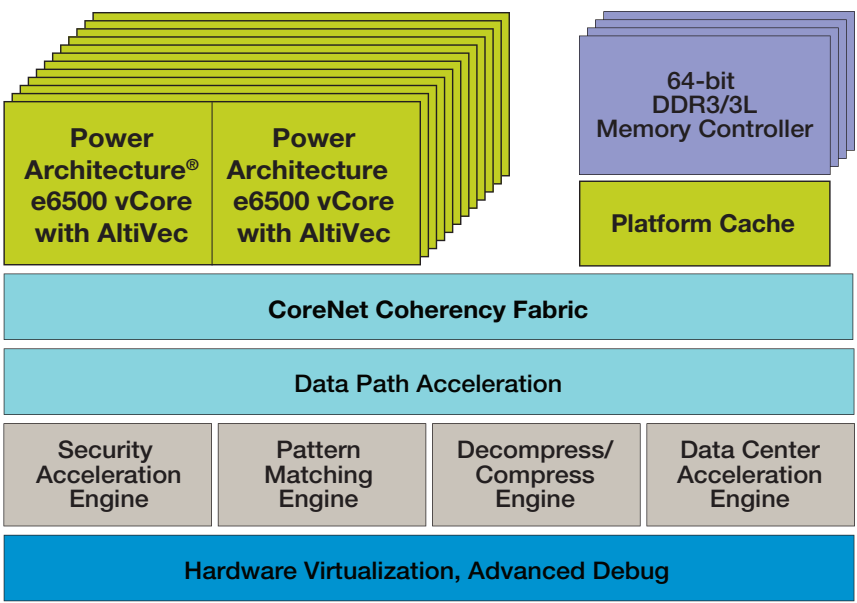
The QorIQ AMP series includes additional application-specific accelerators such as a security engine (SEC), pattern matching engine (PME), DPAA, data flow acceleration and a hardware decompress/compress engine (DCE) that can improve HTTP compress by a factor of four.

The QorIQ AMP processors push beyond a 2x improvement in power efficiency over previous-generation QorIQ devices. Implementing the AMP processors in a 28 nm process yields a 50 percent power savings. The cascading power management architecture enables reduced energy consumption under light network loads and automatically returns to full function when network loads increase. Developers can also dynamically set and change core operating frequencies for each cluster of cores.

The cascading power management architecture supports a state retention power gating (SRPG) “fast on, fast off” technique that allows the voltage supply to be reduced to zero for the majority of a block’s logic gates while maintaining the supply for the state elements of that block to support fast wake up times. As these processors do not have to save/restore processor state to memory, they have a greater than 10x improvement in their wake up response time.

QorIQ AMP processors build on the architecture powering existing QorIQ processors, and maintain software code compatibility with the existing QorIQ P series, QorIQ Qonverge and PowerQUICC processors. On-chip, in-silicon debugging support includes deep inspection debug that provides visibility at the core, accelerator and fabric level of the processor. Full system trace includes change of flow, process and originator trace integrated with instrumented OS trace. A developer has complete control of event configuration to monitor, trigger, timestamp and count thousands of core/ SoC events and user-defined messages. The debug architecture enables tracking core interactions with advanced cross-triggering. Built-in security mechanisms prevent debug interface intrusions. The debugging system also supports configurable black box recording for post-mortem debug. Development is supported by Freescale’s CodeWarrior tools and VortiQa software, as well as third-party tools from Enea®, QNX®, Mentor Embedded, Green Hills® and Wind River.

QorIQ AMP Series Architecture



QorIQ T4240 Processor

The QorIQ T4240 is the first AMP series device scheduled for release early in 2012, and targets data plane, metro carrier edge routers, aerospace and defense, as well as access gateway applications. Additional AMP devices are planned for release each quarter thereafter. The T4240 processor integrates twelve e6500 cores into a single device—organized into three processor clusters of four cores each. The 24 virtual cores operate at up to 1.8 GHz and support processing for 40 Gbps of packet throughput.

System performance for the 12-core (24 virtual core) QorIQ AMP T4240 processor is rated at up to four times that of the previous generation eight-core P4080 device. The L2 cache is six times larger. The T4240 processor delivers a 3x improvement in data path acceleration and a 2x improvement in throughput for the CoreNet fabric, security engine, OCEAN and data flow acceleration blocks. The data decompression/compression accelerator (20 Gbps) and Interlaken Look-aside (80 Gbps) are not available on the P4080 and are new with the T4240 processor.

Summary

Smaller process implementations demonstrate that technology scaling continues to deliver benefits. At 28 nm, QorIQ processors experience 50 percent lower power to retain constant processing performance while enjoying a 40 percent silicon area reduction over 45 nm implementations. Freescale’s experience with 28 nm process technology continues to foreshadow that next-generation application performance will be achieved through a combination of smaller process nodes and the use of more processing engines—in the form of more cores and accelerators. This combination will be able to deliver an application performance improvement of up to 4x at the new process node, exceeding the limitation of Moore’s Law.

*Per benchmarks such as Dhrystone and EEMBC
 **Based on an encryption function running on the SEC accelerator

How to Reach Us:

Home Page:

freescale.com

QorIQ AMP Series Information:

freescale.com/QorIQAMPseries

e-mail:

support@freescale.com

USA/Europe or Locations Not Listed:

Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
1-800-521-6274
480-768-2130
support@freescale.com

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate,
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor
Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447
303-675-2140
Fax: 303-675 2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright license granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

To learn more about the QorIQ AMP series, visit

freescale.com/QorIQAMPseries

Freescale, the Freescale logo, CodeWarrior, PowerQUICC and QorIQ are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. VortiQa is a trademark of Freescale Semiconductor, Inc. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org. All other product or service names are the property of their respective owners. © 2011 Freescale Semiconductor, Inc.

Document Number: QORIQAMPWP / REV 0