AEC-Q100F Qualification Results Summary

Objective: **To qualify NPI 9S08DZ60 M74K in a 64 LQFP Package**

Freescale PN: 9S08DZ60 Part Name: Longhorn		Customer Name(s): Multiple PN(s):			Plan or Results: Results Revision # & Date: 1.6 29 April 2008 (See Revision History in Notes)
Technology: 0.25um Embedded Flash Package: 64 LQFP 10x10 Package code (8426)		Design Engr: Phone #: Rubens Takiguti			QUARTZ Tracking #: 81898
Fab / Assembly / Final Test Sites: FSL-ATMC/FSL-TJN-FM/FSL-TJN-FM		Product Engr: Phone #: Todd Flynn and David Rosas			(Signature/Date shown below may be electronic)
Maskset#: Rev#: 0/1M74K		Prod. Package Engr: Phone #: Matt Zapico			PPE Approval (for DIM/BOM results) Signature & Date: Matt Zapico
Die Size (in mm) W x L x T 3.3900x3.3660		NPI PRQE: Phone #: Valerie Kim			NPI PRQE Approval Signature & Date: Valerie Kim
Part Operating Temp. Grade: Grade 1 -40°C to +125°C		Trace/DateCode:	Lot A YZME00269C00	Lot B THWD00049W00	Lot C ME002UUR00
					CAB Approval 08180192M Signature & Date: April 29, 2008

Example: TESTS HIGHLIGHTED IN YELLOW WERE PERFORMED FOR THIS STUDY

This testing is performed by Freescale Reliability Lab (ATX RAL) unless otherwise noted in the Comments.

GROUP A - ACCELERATED ENVIRONMENTAL STRESS TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments
PC	JESD22-A113 J-STD-020	**Preconditioning (PC) :** PC required for SMDs only. MSL 3 @ 260°C, +5/-0°C	TEST @ RH	All surface mount devices prior to THB, HAST, AC, and TC and as required per test conditions.			Lot A 0/77	DZ60 M05C Package Qualification 0/693
HAST	JESD22-A101 A110	**Highly Accelerated Stress Test (HAST):** PC before HAST (for SMDs only): Required HAST = 130°C/85%RH for 96 hrs. *Timed RO of 48hrs. MAX*	TEST @ RH	77	1	77	Lot A 0/77	DZ60 M05C Package Qualification 0/231
AC	JESD22-A102 A118	**Autoclave (AC):** PC before AC (for SMDs only): Required AC = 121°C/100%RH/15 psig for 96 hrs *Timed RO of 2-48hrs. MAX*	TEST @ R	77	0	0	Pass	DZ60 M05C Package Qualification 0/231
TC	JESD22-A104 AEC Q100-Appendix 3	**Temperature Cycle (TC):** PC before TC (for SMDs only): Required TC = -65°C to 150°C for 500 cycles. WBP after TC on 5 devices from 1 lot; 2 bonds per corner and one mid-bond per side on each device. Record which pins were used.	TEST @ HC WBP =/> 3 grams	77	0	0	Pass	DZ60 M05C Package Qualification 0/231 WBP 0/5
HTSL	JESD22-A103	**High Temperature Storage Life (HTSL):** 150°C for 1008 hrs or 175°C for 504hrs (Devices incorporating NVM shall receive 'NVM endurance preconditioning'(EDR) prior to this test, and special NVM test sequencing after this test; see AEC-Q100 for details) *Timed RO = 96hrs. MAX*	TEST @ RHC	77	0	0	Pass	Refer to EDR

TEST GROUP B - ACCELERATED LIFETIME SIMULATION TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments

HTOL	AEC Q100-005	**High Temperature Operating Life (HTOL):** Ta = 125°C for 1008 hrs (Devices incorporating NVM shall receive 'NVM endurance preconditioning'(EDR) prior to this test, and special NVM test sequencing after this test; see AEC-Q100 for details) **Timed RO of 96hrs. MAX**	TEST @ RHC	77	3	231	HTOL @125C for 168 hrs Lot A 0/77 Lot B 0/77 Lot C 0/77	DZ60 M05C Die Qualification @125C @1008 hrs 0/231
ELFR	AEC Q100-008	**Early Life Failure Rate ELFR):** Ta = 125°C for 48 hrs ***Timed RO of 48 hrs MAX***	TEST @ RHC	800	0	0	Pass	DZ60 M05C Die Qualification 0/2400 Generic Data 9S12C32 0/844
EDR	AEC Q100-005	**NVM Endurance, Data Retention, and Operational Life (EDR):** (also known as NVM Endurance Preconditioning) Spec Cycling @ 125 C DRB **@ 175 C for 504 hrs** ***Timed RO of 48hrs. MAX***	TEST @ RHC	77	1	77	WE @125C & DRB @175C for 504 hrs Lot B 0/77	DZ60 M05C Die Qualification @150C for 1008 hrs 0/231
EDR	AEC Q100-005	**NVM Endurance, Data Retention, and Operational Life (EDR):** (also known as NVM Endurance Preconditioning) Spec Cycling @ -40 C DRB **@ 175 C for 504 hrs** ***Timed RO of 48hrs. MAX***	TEST @ RHC	77	1	77	WE @-40C & DRB @175C for 504 hrs Lot B 0/77	DZ60 M05C Die Qualification @150C for 1008 hrs 0/231

TEST GROUP C - PACKAGE ASSEMBLY INTEGRITY TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments
WBS	AEC Q100-001	**Wire Bond shear (WBS)**	Cpk = or > 1.67	30 bonds from minimum 5 units	1	5	0/5 Cpk > 1.67	Performed by Assembly Site during qual lot builds
WBP	MilStd883- 2011	**Wire Bond Pull (WBP):** Cond. C or D	Cpk = or > 1.67	30 bonds from minimum 5 units	1	5	0/5 Cpk > 1.67	Performed by Assembly Site during qual lot builds
SD	JESD22- B102	**Solderability (SD):** 8hr.(1 hr. for Au-plated leads) Steam age prior to test. **If production burn-in is done, samples must also undergo burn-in prior to SD.**	>95% lead coverage of critical areas	15	0	0	Pass	**Production Burn In is required prior to SD.** DZ60 M05C Package Qualification Passed @KLM post production burn-in 0/15
PD	JESD22- B100	**Physical Dimensions(PD):** PD per FSL 98A drawing	Cpk = or > 1.67	10	0	0	Pass	Performed by Assembly Site during qual lot builds DZ60 M05C Package Qualification 0/30
DIM & BOM		**Dimensional (DIM):** PPE to verify PD results against valid 98A drawing. **BOM Verification (BOM):** PPE to verify qual lot ERF BOM is accurate.					DIM: Complete BOM: Complete	Complete

TEST GROUP E - ELECTRICAL VERIFICATION TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments
TEST	Freescale 48A	**Pre- and Post Functional / Parametrics (TEST):** Test software shall meet requirements of AEC-Q100-007. Testing performed to the limits of device specification in temperature and limit value.	0 Fails	All	All	All	See Results Summary	Final test TJN

HBM	AEC-Q100-002	**ElectroStatic Discharge/ Human Body Model Classification (HBM):** Test @ 250/500/1000/1500/2000 Volts See AEC-Q100-002 for classification levels.	TEST @ RH 2KV min.	3 units per Voltage level	1	15	Lot C 0/3 @250V, 0/3 @500V, 0/3 @1000V, 0/3 @1500V, 0/3 @2000V	Levels below 2000V require customer approval.
CDM	AEC-Q100-011	**ElectroStatic Discharge/ Charged Device Model Classification (CDM):** Test @ 250/500/750 Volts See AEC-Q100-011 for classification levels. ***Timed RO of 96hrs MAX.***	TEST @ RH Corner pins =/> 750V; All other pins =/> 500V	3 units per Voltage level	1	9	Lot C 0/3 @250V, 0/3 @500V, 0/3 @750V all pins	Levels below 750V for corner pins and below 500V for all other pins require customer approval.
LU	JESD78 plus AEC-Q100-004	**Latch-up (LU):** Test per JEDEC JESD78 with the AEC-Q100-004 requirements. Ta= Maximum operating temperature Vsupply = Maximum operating voltage	TEST @ RH	6	1	6	Lot C 0/6	
ED	AEC-Q100-009, Freescale 48A spec	**Electrical Distribution (ED)**	TEST @ RHC Cpk = or > 1.67	30	3	90	Complete	
FG	AEC-Q100-007	**Fault Grading (FG)**	FG shall be = or > 90% for qual units				FG% > 95% w/iddq	
GL	AEC-Q100-006	**Electro-Thermally Induced Gate Leakage (GL):** 155°C, 2.0 min, +400/-400 V *Timed RO of 96 hrs MAX.* *For all failures, perform unbiased bake (4hrs/125°C, or 2hrs/150°C) and retest; recovered units are GL failures.*	TEST @ R	6	0	0	Pass	DZ60 M05C Die Qualification 0/6
EMC	SAE J1752/3 - Radiated Emissions	**Electromagnetic Compatibility (EMC)** (see AEC Q100 Appendix 5 for test applicability; done on case-by-case basis per customer/Freescale agreement)	<40dBuV 150KHz - 1GHz	1	0	0	N/A	DZ60 M05C Die Qualification 0/1

Generic Data List:

Quartz #	Mask Set	Product-Qual Description / Part Number(s)	Critical Parameter	Critical Parameter	Die Size	Mold Compound/ Die attach	CAB Number	CAB Date
29851	M34C	9S12C32	TJN	ATMC	3.906x3.189	MC HITACHI 9200HF10M	2006	25 Jan 2006
58658/78839/90001	1/3M05C	DZ60	TJN	ATMC	3.390x3.366	MC HITACHI 9200HF10M	2007 39 39398	26 Sep 2007

Revision	Revision Date	Description	Author
1.0	16-Apr-07	1st draft	V. Kim
1.1	17-Jul-07	2nd draft (die qual added)	V. Kim
1.2	1-Aug-07	Peer Review	V. Kim
1.3	9-Jan-08	Updated HTOL duration	V. Kim
1.4	7-Apr-08	Updated qual results	V. Kim
1.5	25-Apr-08	Finalized with qual results and peer reviewed	V. Kim
1.6	29-Apr-08	Update format	V. Kim

AEC-Q100F Qualification Results Summary

Objective: **To qualify NPI 9S08DZ60 M74K in a 48 LQFP Package**								
Freescale PN: 9S08DZ60 Part Name: Longhorn		Customer Name(s): Multiple PN(s):					Plan or Results: Revision # & Date:	Results 1.1 29 April 2008 (See Revision History in Notes)
Technology: 0.25um Embedded Flash Package: 48 LQFP 7x7 Package Code (6089)		Design Engr: Phone #: Rubens Takiguti					QUARTZ Tracking #:	TBD
Fab / Assembly / Final Test Sites: FSL-ATMC/FSL-TJN-FM/FSL-TJN-FM		Product Engr: Phone #: Todd Flynn and David Rosas						(Signature/Date shown below may be electronic)
Maskset#: Rev#: 0/1M74K		Prod. Package Engr: Phone #: Matt Zapico					PPE Approval (for DIM/BOM results) Signature & Date:	Matt Zapico
Die Size (in mm) W x L x T 3.3900x3.3660		NPI PRQE: Phone #: Valerie Kim					NPI PRQE Approval Signature & Date:	Valerie Kim
Part Operating Temp. Grade: Grade 1	-40°C to +125°C	Trace/DateCode:	LOT A	LOT B	LOT C		CAB Approval Signature & Date:	08180192M April 29, 2008

Example: TESTS HIGHLIGHTED IN YELLOW WERE PERFORMED FOR THIS STUDY

This testing is performed by Freescale Reliability Lab (ATX RAL) unless otherwise noted in the Comments.

GROUP A - ACCELERATED ENVIRONMENTAL STRESS TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments
PC	JESD22-A113 J-STD-020	**Preconditioning (PC) :** PC required for SMDs only. MSL 3 @ 260°C, +5/-0°C	TEST @ RH	All surface mount devices prior to THB, HAST, AC, and TC and as required per test conditions.			Pass	Generic Data 9S12C32 0/693
HAST	JESD22-A101 A110	**Highly Accelerated Stress Test (HAST):** PC before HAST (for SMDs only): Required HAST = 130°C/85%RH for 96 hrs. *Timed RO of 48hrs. MAX*	TEST @ RH	77	0	0	Pass	Generic Data 9S12C32 0/231
AC	JESD22-A102 A118	**Autoclave (AC):** PC before AC (for SMDs only): Required AC = 121°C/100%RH/15 psig for 96 hrs *Timed RO of 2-48hrs. MAX*	TEST @ R	77	0	0	Pass	Generic Data 9S12C32 0/231
TC	JESD22-A104 AEC Q100-Appendix 3	**Temperature Cycle (TC):** PC before TC (for SMDs only): Required TC = -65°C to 150°C for 500 cycles. WBP after TC on 5 devices from 1 lot; 2 bonds per corner and one mid-bond per side on each device. Record which pins were used.	TEST @ HC WBP =/> 3 grams	77	0	0	Pass	Generic Data 9S12C32 0/231 WBP 0/5
HTSL	JESD22-A103	**High Temperature Storage Life (HTSL):** 150°C for 1008 hrs or 175°C for 504hrs (Devices incorporating NVM shall receive 'NVM endurance preconditioning'(EDR) prior to this test, and special NVM test sequencing after this test; see AEC-Q100 for details) *Timed RO = 96hrs. MAX*	TEST @ RHC	77	0	0	Pass	See EDR

TEST GROUP B - ACCELERATED LIFETIME SIMULATION TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments
HTOL	AEC Q100-005	**High Temperature Operating Life (HTOL):** Ta = 125°C for 1008 hrs (Devices incorporating NVM shall receive 'NVM endurance preconditioning'(EDR) prior to this test, and special NVM test sequencing after this test; see AEC-Q100 for details) *Timed RO of 96hrs. MAX*	TEST @ RHC	77	0	0	Pass	See 64 LQFP DZ60 Qual Data

ELFR	AEC Q100-008	**Early Life Failure Rate ELFR):** Ta = 125°C for 48 hrs ***Timed RO of 48 hrs MAX***	TEST @ RHC	800	0	0	Pass	See 64 LQFP DZ60 Qual Data
EDR	AEC Q100-005	**NVM Endurance, Data Retention, and Operational Life (EDR):** (also known as NVM Endurance Preconditioning) W/E Cycling @ 125 C DRB @ 175 C for 504 hrs Page Mode ***Timed RO of 48hrs. MAX***	TEST @ RHC	77	0	0	Pass	See 64 LQFP DZ60 Qual Data
EDR	AEC Q100-005	**NVM Endurance, Data Retention, and Operational Life (EDR):** (also known as NVM Endurance Preconditioning) W/E Cycling @ -40 C DRB @ 175 C for 504 hrs Page Mode ***Timed RO of 48hrs. MAX***	TEST @ RHC	77	0	0	Pass	See 64 LQFP DZ60 Qual Data

TEST GROUP C - PACKAGE ASSEMBLY INTEGRITY TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments
WBS	AEC Q100-001	**Wire Bond shear (WBS)**	Cpk = or > 1.67	30 bonds from minimum 5 units	0	0	Pass	Performed by Assembly Site during qual lot builds DZ60 M05C Package Qualification 0/5
WBP	MilStd883-2011	**Wire Bond Pull (WBP):** Cond. C or D	Cpk = or > 1.67	30 bonds from minimum 5 units	0	0	Pass	Performed by Assembly Site during qual lot builds DZ60 M05C Package Qualification 0/5
SD	JESD22-B102	**Solderability (SD):** 8hr.(1 hr. for Au-plated leads) Steam age prior to test. **If production burn-in is done, samples must also undergo burn-in prior to SD.**	>95% lead coverage of critical areas	15	0	0	Pass	Production Burn In is required prior to SD. DZ60 M05C Package Qualification 0/15 @KLM post production burn-in
PD	JESD22-B100	**Physical Dimensions(PD):** PD per FSL 98A drawing	Cpk = or > 1.67	10	0	0	Pass	Performed by Assembly Site during qual lot builds DZ60 M05C Package Qualification 0/30 Cpk > 1.67
DIM & BOM		**Dimensional (DIM):** PPE to verify PD results against valid 98A drawing. **BOM Verification (BOM):** PPE to verify qual lot ERF BOM is accurate.					DIM: Complete BOM: Complete	Complete

TEST GROUP E - ELECTRICAL VERIFICATION TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments
TEST	Freescale 48A	**Pre- and Post Functional / Parametrics (TEST):** Test software shall meet requirements of AEC-Q100-007. Testing performed to the limits of device	0 Fails	All	All	All	See Results Summary	Final Test Site: TJN

HBM	AEC-Q100-002	**ElectroStatic Discharge/ Human Body Model Classification (HBM):** Test @ 250/500/1000/1500/2000 Volts See AEC-Q100-002 for classification levels.	TEST @ RH 2KV min.	3 units per Voltage level	0	0	Pass	DZ60 M05C Die Qualification 0/15
CDM	AEC-Q100-011	**ElectroStatic Discharge/ Charged Device Model Classification (CDM):** Test @ 250/500/750 Volts See AEC-Q100-011 for classification levels. ***Timed RO of 96hrs MAX.***	TEST @ RH Corner pins =/> 750V; All other pins =/> 500V	3 units per Voltage level	0	0	Pass	Levels below 750V for corner pins and below 500V for all other pins require customer approval. DZ60 M05C Package Qualification 0/9
LU	JESD78 plus AEC-Q100-004	**Latch-up (LU):** Test per JEDEC JESD78 with the AEC-Q100-004 requirements. Ta= Maximum operating temperature Vsupply = Maximum operating voltage	TEST @ RH	6	0	0	Pass	DZ60 M05C Die Qualification 0/6
ED	AEC-Q100-009, Freescale 48A spec	**Electrical Distribution (ED)**	TEST @ RHC Cpk = or > 1.67	30	0	0	Pass	See 64 LQFP DZ60 Qual Data
FG	AEC-Q100-007	**Fault Grading (FG)**	FG shall be = or > 90% for qual units				FG% > 95% w/iddq	

Stress Test	**Reference**	**Test Conditions**	**End Point Requirements**	**Minimum Sample Size**	**# of Lots**	**Total Units including spares**	**Results** Lot ID-(#Rej/SS) NA=Not Applicable	**Comments**
GL	AEC-Q100-006	**Electro-Thermally Induced Gate Leakage (GL):** 155°C, 2.0 min, +400/-400 V *Timed RO of 96 hrs MAX. For all failures, perform unbiased bake (4hrs/125°C, or 2hrs/150°C) and retest; recovered units are GL failures.*	TEST @ R	6	0	0	Pass	DZ60 M05C Die Qualification 0/6
EMC	SAE J1752/3 - Radiated Emissions	**Electromagnetic Compatibility (EMC)** (see AEC Q100 Appendix 5 for test applicability; done on case-by-case basis per customer/Freescale agreement)	<40dBuV 150KHz - 1GHz	1	0	0	N/A	DZ60 M05C Die Qualification 0/1

Generic Data List:

Quartz #	Mask Set	Product-Qual Description / Part Number(s)	Critical Parameter	Critical Parameter	Die Size	Mold Compound/ Die attach	CAB Number	CAB Date
29851	M34C	9S12C32 48L	TJN	ATMC	3.906x3.189	MC HITACHI 9200HF10M	2006	25 Jan 2006
58658/59996/78839	1/3M05C	DZ60	TJN	ATMC	3.390x3.366	MC HITACHI 9200HF10M	2007 39 39398	26 Sep 2007

Revision	**Revision Date**	**Description**	**Author**
1.0	16-Apr-07	1st draft	V. Kim
1.1	29-Apr-08	Updated with generic data	V. Kim

AEC-Q100F Qualification Plan/Results Summary

Objective: **To qualify NPI 9S08DZ60 M74K in a 32 LQFP Package**

Freescale PN: 9S08DZ60 Part Name: Longhorn	Customer Name(s): Multiple PN(s):		Plan or Results: Results Revision # & Date: 1.1 29 April 2008 (See Revision History in Notes)
Technology: 0.25um Embedded Flash Package: 32 LQFP 7x7 Package Code (6300)	Design Engr: Phone #: Rubens Takiguti		QUARTZ Tracking #: TBD
Fab / Assembly / Final Test Sites: FSL-ATMC/FSL-TJN-FM/FSL-TJN-FM/FSL-TJN-FM	Product Engr: Phone #: Todd Flynn and David Rosas		(Signature/Date shown below may be electronic)
Maskset#: Rev#: 0/1M74K	Prod. Package Engr: Phone #: Matt Zapico		PPE Approval (for DIM/BOM results) Signature & Date: Matt Zapico
Die Size (in mm) W x L x T 3.3900x3.3660	NPI PRQE: Phone #: Valerie Kim		NPI PRQE Approval Signature & Date: Valerie Kim
Part Operating Temp. Grade: Grade 1 -40°C to +125°C	Trace/DateCode: LOT A / LOT B / LOT C		CAB Approval Signature & Date: 08180192M April 29, 2008

Example: TESTS HIGHLIGHTED IN YELLOW WERE PERFORMED FOR THIS STUDY

This testing is performed by Freescale Reliability Lab (ATX RAL) unless otherwise noted in the Comments.

GROUP A - ACCELERATED ENVIRONMENTAL STRESS TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments
PC	JESD22-A113 J-STD-020	**Preconditioning (PC) :** PC required for SMDs only. MSL 3 @ 260°C, +5/-0°C	TEST @ RH	All surface mount devices prior to THB, HAST, AC, and TC and as required per test conditions.			Pass	See 48 LQFP DZ60 Package Qual Data.
HAST	JESD22-A101 A110	**Highly Accelerated Stress Test (HAST):** PC before HAST (for SMDs only): Required HAST = 130°C/85%RH for 96 hrs. *Timed RO of 48hrs. MAX*	TEST @ RH	77	0	0	Pass	See 48 LQFP DZ60 Package Qual Data.
AC	JESD22-A102 A118	**Autoclave (AC):** PC before AC (for SMDs only): Required AC = 121°C/100%RH/15 psig for 96 hrs *Timed RO of 2-48hrs. MAX*	TEST @ R	77	0	0	Pass	See 48 LQFP DZ60 Package Qual Data.
TC	JESD22-A104 AEC Q100-Appendix 3	**Temperature Cycle (TC):** PC before TC (for SMDs only): Required TC = -65°C to 150°C for 500 cycles. WBP after TC on 5 devices from 1 lot; 2 bonds per corner and one mid-bond per side on each device. Record which pins were used.	TEST @ HC WBP =/> 3 grams	77	0	0	Pass	See 48 LQFP DZ60 Package Qual Data.
HTSL	JESD22-A103	**High Temperature Storage Life (HTSL):** 150°C for 1008 hrs or 175°C for 504hrs (Devices incorporating NVM shall receive 'NVM endurance preconditioning'(EDR) prior to this test, and special NVM test sequencing after this test; see AEC-Q100 for details) *Timed RO = 96hrs. MAX*	TEST @ RHC	77	0	0	Pass	See EDR

TEST GROUP B - ACCELERATED LIFETIME SIMULATION TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments

HTOL	AEC Q100-005	**High Temperature Operating Life (HTOL):** Ta = 125°C for 1008 hrs (Devices incorporating NVM shall receive 'NVM endurance preconditioning'(EDR) prior to this test, and special NVM test sequencing after this test; see AEC-Q100 for details) *Timed RO of 96hrs. MAX*	TEST @ RHC	77	0	0	Pass	See 64 LQFP DZ60 Qual Data
ELFR	AEC Q100-008	**Early Life Failure Rate ELFR):** Ta = 125°C for 48 hrs ***Timed RO of 48 hrs MAX***	TEST @ RHC	800	0	0	Pass	See 64 LQFP DZ60 Qual Data
EDR	AEC Q100-005	**NVM Endurance, Data Retention, and Operational Life (EDR):** (also known as NVM Endurance Preconditioning) W/E Cycling @ 125 C DRB @ 175 C for 504 hrs Page Mode ***Timed RO of 48hrs. MAX***	TEST @ RHC	77	0	0	Pass	See 64 LQFP DZ60 Qual Data
EDR	AEC Q100-005	**NVM Endurance, Data Retention, and Operational Life (EDR):** (also known as NVM Endurance Preconditioning) W/E Cycling @ -40 C DRB @ 175 C for 504 hrs Page Mode ***Timed RO of 48hrs. MAX***	TEST @ RHC	77	0	0	Pass	See 64 LQFP DZ60 Qual Data
TEST GROUP C - PACKAGE ASSEMBLY INTEGRITY TESTS								
Stress Test	**Reference**	**Test Conditions**	**End Point Requirements**	**Minimum Sample Size**	**# of Lots**	**Total Units including spares**	**Results** Lot ID-(#Rej/SS) NA=Not Applicable	**Comments**
WBS	AEC Q100-001	**Wire Bond shear (WBS)**	Cpk = or > 1.67	30 bonds from minimum 5 units	0	0	Pass	Performed by Assembly Site during qual lot builds DZ60 M05C Package Qualification 0/5
WBP	MilStd883-2011	**Wire Bond Pull (WBP):** Cond. C or D	Cpk = or > 1.67	30 bonds from minimum 5 units	0	0	Pass	Performed by Assembly Site during qual lot builds DZ60 M05C Package Qualification 0/5
SD	JESD22-B102	**Solderability (SD):** 8hr.(1 hr. for Au-plated leads) Steam age prior to test. **If production burn-in is done, samples must also undergo burn-in prior to SD.**	>95% lead coverage of critical areas	15	0	0	Pass	Production Burn In is required prior to SD. DZ60 M05C Package Qualification 0/15 @KLM post production burn-in
PD	JESD22-B100	**Physical Dimensions(PD):** PD per FSL 98A drawing	Cpk = or > 1.67	10	0	0	Pass	Performed by Assembly Site during qual lot builds DZ60 M05C Package Qualification 0/30 Cpk > 1.67
DIM & BOM		**Dimensional (DIM):** PPE to verify PD results against valid 98A drawing. **BOM Verification (BOM):** PPE to verify qual lot ERF BOM is accurate.					DIM: Complete BOM: Complete	Complete
TEST GROUP E - ELECTRICAL VERIFICATION TESTS								

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments
TEST	Freescale 48A	**Pre- and Post Functional / Parametrics (TEST):** Test software shall meet requirements of AEC-Q100-007. Testing performed to the limits of device specification in temperature and limit value.	0 Fails	All	All	All	See Results Summary	Final Test Site: TJN
HBM	AEC-Q100-002	**ElectroStatic Discharge/ Human Body Model Classification (HBM):** Test @ 250/500/1000/1500/2000 Volts See AEC-Q100-002 for classification levels.	TEST @ RH 2KV min.	3 units per Voltage level	0	0	Pass	DZ60 M05C Die Qualification 0/15
CDM	AEC-Q100-011	**ElectroStatic Discharge/ Charged Device Model Classification (CDM):** Test @ 250/500/750 Volts See AEC-Q100-011 for classification levels. ***Timed RO of 96hrs MAX.***	TEST @ RH Corner pins =/> 750V; All other pins =/> 500V	3 units per Voltage level	0	0	Pass	Levels below 750V for corner pins and below 500V for all other pins require customer approval. 9S08DZ60 M05C 0/9
LU	JESD78 plus AEC-Q100-004	**Latch-up (LU):** Test per JEDEC JESD78 with the AEC-Q100-004 requirements. Ta= Maximum operating temperature Vsupply = Maximum operating voltage	TEST @ RH	6	0	0	Pass	DZ60 M05C Die Qualification 0/6
ED	AEC-Q100-009, Freescale 48A spec	**Electrical Distribution (ED)**	TEST @ RHC Cpk = or > 1.67	30	0	0	Pass	See 64 LQFP DZ60 Qual Data
FG	AEC-Q100-007	**Fault Grading (FG)**	FG shall be = or > 90% for qual units				FG% > 95% w/iddq	
GL	AEC-Q100-006	**Electro-Thermally Induced Gate Leakage (GL):** 155°C, 2.0 min, +400/-400 V *Timed RO of 96 hrs MAX.* *For all failures, perform unbiased bake (4hrs/125°C, or 2hrs/150°C) and retest; recovered units are GL failures.*	TEST @ R	6	0	0	Pass	DZ60 M05C Die Qualification 0/6
EMC	SAE J1752/3 - Radiated Emissions	**Electromagnetic Compatibility (EMC)** (see AEC Q100 Appendix 5 for test applicability; done on case-by-case basis per customer/Freescale agreement)	<40dBuV 10KHz - 1MHz	1	0	0	Pass	DZ60 M05C Die Qualification 0/1

Generic Data List:

Quartz #	Mask Set	Product-Qual Description / Part Number(s)	Critical Parameter	Critical Parameter	Die Size	Mold Compound/ Die attach	CAB Number	CAB Date
29851	M34C	9S12C32 48L	TJN	ATMC	3.906x3.189	MC HITACHI 9200HF10M	2006	25 Jan 2006
58658/59996/78839	1/3M05C	DZ60	TJN	ATMC	3.390x3.366	MC HITACHI 9200HF10M	2007 39 39398	26 Sep 2007

Revision	Revision Date	Description	Author
1.0	16-Apr-07	1st draft	V. Kim
1.1	29-Apr-08	Updated with generic data	V. Kim