**Objective:** To qualify NPI 9S08DZ60 M74K in a 64 LQFP Package

### Freescale PN:
- **9S08DZ60**
- **Part Name:** Longhorn

### Technology:
- 0.25um Embedded Flash

### Package:
- 64 LQFP 10x10 Package code (8426)

### Fab / Assembly:
- Final Test Sites: FSL-ATMC/FSL-TJN-FM/FSL-TJN-FM

### Customer Name(s):
- Rubens Takiguti

### Design Engr:
- Phone #: Todd Flynn and David Rosas

### NPI PRQE:
- Phone #: Matt Zapico

### Part Operating Temp. Grade:
- Grade 1 -40°C to +125°C

### Die Size (in mm):
- W x L x T = 3.3900x3.3660

### Die Size (in mm):
- W x L x T = 3.3900 x 3.3660

---

### GROUP A - ACCELERATED ENVIRONMENTAL STRESS TESTS

#### PC

- **Reference:** JESD22-A113, J-STD-020
- **Test Conditions:** Preconditioning (PC): PC required for SMDs only. MSL 3 @ 260°C, +5/-0°C
- **End Point Requirements:** TEST @ RH
- **Minimum Sample Size:** All surface mount devices prior to THB. HAST, AC, and TC
- **# of Lots:** 77
- **Total Units including spares:** 77
- **Results:** Lot A 0/77
- **Comments:** D260 M05C Package Qualification 0/693

#### HAST

- **Reference:** JESD22-A101, A110
- **Test Conditions:** Highly Accelerated Stress Test (HAST): PC before HAST (for SMDs only); Required HAST = 130°C/85%RH for 96 hrs. Timed RO of 48hrs. MAX
- **End Point Requirements:** TEST @ RH
- **Minimum Sample Size:** 77
- **# of Lots:** 1
- **Total Units including spares:** 77
- **Results:** Lot A 0/77
- **Comments:** D260 M05C Package Qualification 0/231

#### AC

- **Reference:** JESD22-A102, A118
- **Test Conditions:** Autoclave (AC): PC before AC (for SMDs only); Required AC = 121°C/100%RH/15 paig for 96 hrs. Timed RO of 2-48hrs. MAX
- **End Point Requirements:** TEST @ R
- **Minimum Sample Size:** 77
- **# of Lots:** 0
- **Total Units including spares:** 0
- **Results:** Pass
- **Comments:** D260 M05C Package Qualification 0/231

#### TC

- **Reference:** JESD22-A104, AEC-Q100, Appendix 3
- **Test Conditions:** Temperature Cycle (TC): PC before TC (for SMDs only); Required TC = -65°C to 150°C for 500 cycles. WBP after TC on 5 devices from 1 lot: 2 bonds per corner and one mid-bond per side on each device. Record which pins were used.
- **End Point Requirements:** TEST @ HC
- **Minimum Sample Size:** 77
- **# of Lots:** 0
- **Total Units including spares:** 0
- **Results:** Pass
- **Comments:** D260 M05C Package Qualification 0/231 WBP 0/S

#### HTSL

- **Reference:** JESD22-A103
- **Test Conditions:** High Temperature Storage Life (HTSL): 150°C for 1008 hrs or 175°C for 504hrs (Devices incorporating NVM shall receive ‘NVM endurance preconditioning(EDR) prior to this test, and special NVM test sequencing after this test; see AEC-Q100 for details) Timed RO = 96hrs. MAX
- **End Point Requirements:** TEST @ HRC
- **Minimum Sample Size:** 77
- **# of Lots:** 0
- **Total Units including spares:** 0
- **Results:** Pass
- **Comments:** Refer to EDR

---

**Example:** TESTS HIGHLIGHTED IN YELLOW WERE PERFORMED FOR THIS STUDY

This testing is performed by Freescale Reliability Lab (ATX RAL) unless otherwise noted in the Comments.

---

### GROUP B - ACCELERATED LIFETIME SIMULATION TESTS

<table>
<thead>
<tr>
<th>Stress Test</th>
<th>Reference</th>
<th>Test Conditions</th>
<th>End Point Requirements</th>
<th>Minimum Sample Size</th>
<th># of Lots</th>
<th>Total Units including spares</th>
<th>Results</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>PC</td>
<td></td>
<td></td>
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<td>HTSL</td>
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</tbody>
</table>

**Note:** This testing is performed by Freescale Reliability Lab (ATX RAL) unless otherwise noted in the Comments.
<table>
<thead>
<tr>
<th>Test</th>
<th>Reference</th>
<th>Test Conditions</th>
<th>End Point Requirements</th>
<th>Minimum Sample Size</th>
<th># of Lots</th>
<th>Total Units including spares</th>
<th>Results</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>HTOL</td>
<td>AEC Q100-005</td>
<td>High Temperature Operating Life (HTOL): Ta = 125°C for 1008 hrs (Devices incorporating NVM shall receive 'NVM endurance preconditioning' (EDR) prior to this test, and special NVM test sequencing after this test; see AEC-Q100 for details) Timed RO of 96hrs. MAX</td>
<td>TEST @ RHC</td>
<td>77</td>
<td>3</td>
<td>231</td>
<td>HTOL @125°C for 168 hrs Lot A 0/77 Lot B 0/77 Lot C 0/77</td>
<td>D260 M05C Die Qualification @125°C @1008 hrs 0/231</td>
</tr>
<tr>
<td>ELFR</td>
<td>AEC Q100-008</td>
<td>Early Life Failure Rate ELFR): Ta = 125°C for 48 hrs Timed RO of 48 hrs MAX</td>
<td>TEST @ RHC</td>
<td>800</td>
<td>0</td>
<td>0</td>
<td>Pass</td>
<td>D260 M05C Die Qualification 0/2400 Generic Data 9512C32 0/844</td>
</tr>
<tr>
<td>EDR</td>
<td>AEC Q100-005</td>
<td>NVM Endurance, Data Retention, and Operational Life (EDR): (also known as NVM Endurance Preconditioning) Spec Cycling @ 125°C DRB @ 175°C for 504 hrs Timed RO of 48hrs. MAX</td>
<td>TEST @ RHC</td>
<td>77</td>
<td>1</td>
<td>77</td>
<td>WE @125°C &amp; DRB @175°C for 504 hrs Lot B 0/77</td>
<td>D260 M05C Die Qualification @150°C for 1008 hrs 0/231</td>
</tr>
<tr>
<td>EDR</td>
<td>AEC Q100-005</td>
<td>NVM Endurance, Data Retention, and Operational Life (EDR): (also known as NVM Endurance Preconditioning) Spec Cycling @ -40°C DRB @ 175°C for 504 hrs Timed RO of 48hrs. MAX</td>
<td>TEST @ RHC</td>
<td>77</td>
<td>1</td>
<td>77</td>
<td>WE @-40°C &amp; DRB @175°C for 504 hrs Lot B 0/77</td>
<td>D260 M05C Die Qualification @150°C for 1008 hrs 0/231</td>
</tr>
</tbody>
</table>

**TEST GROUP C - PACKAGE ASSEMBLY INTEGRITY TESTS**

<table>
<thead>
<tr>
<th>Stress Test</th>
<th>Reference</th>
<th>Test Conditions</th>
<th>End Point Requirements</th>
<th>Minimum Sample Size</th>
<th># of Lots</th>
<th>Total Units including spares</th>
<th>Results</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>WBS</td>
<td>AEC Q100-001</td>
<td>Wire Bond shear (WBS) Cpk = or &gt; 1.67</td>
<td>30 bonds from minimum 5 units</td>
<td>1</td>
<td>5</td>
<td>D5 Cpk &gt; 1.67</td>
<td>Performed by Assembly Site during qual lot builds</td>
<td></td>
</tr>
<tr>
<td>WBP</td>
<td>MilStd883- 2011</td>
<td>Wire Bond Pull (WBP): Cond. C or D Cpk = or &gt; 1.67</td>
<td>30 bonds from minimum 5 units</td>
<td>1</td>
<td>5</td>
<td>D5 Cpk &gt; 1.67</td>
<td>Performed by Assembly Site during qual lot builds</td>
<td></td>
</tr>
<tr>
<td>SD</td>
<td>JESD22- B102</td>
<td>Solderability (SD): 8hr. (1 hr. for Au-plated leads) Steam age prior to test. If production burn-in is done, samples must also undergo burn-in prior to SD. ≥95% lead coverage of critical areas</td>
<td>15</td>
<td>0</td>
<td>0</td>
<td>Pass</td>
<td>Production Burn In is required prior to SD. D260 M05C Package Qualification Passed @KLM post production burn-in 0/15</td>
<td></td>
</tr>
<tr>
<td>PD</td>
<td>JESD22- B100</td>
<td>Physical Dimensions(PD): PD per FSL 98A drawing Cpk = or &gt; 1.67</td>
<td>10</td>
<td>0</td>
<td>0</td>
<td>Pass</td>
<td>Performed by Assembly Site during qual lot builds D260 M05C Package Qualification 0/30</td>
<td></td>
</tr>
<tr>
<td>DIM &amp; BOM</td>
<td></td>
<td>Dimensional (DIM): PPE to verify PD results against valid 98A drawing. BOM Verification (BOM): PPE to verify qual lot ERF BOM is accurate.</td>
<td></td>
<td></td>
<td></td>
<td>DIM: Complete BOM: Complete</td>
<td>Complete</td>
<td></td>
</tr>
</tbody>
</table>

**TEST GROUP E - ELECTRICAL VERIFICATION TESTS**

<table>
<thead>
<tr>
<th>Stress Test</th>
<th>Reference</th>
<th>Test Conditions</th>
<th>End Point Requirements</th>
<th>Minimum Sample Size</th>
<th># of Lots</th>
<th>Total Units including spares</th>
<th>Results</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>TEST</td>
<td>Freescale 48A</td>
<td>Pre- and Post Functional / Parametrics (TEST): Test software shall meet requirements of AEC-Q100-007. Testing performed to the limits of device specification in temperature and limit value.</td>
<td>0 Fails</td>
<td>All</td>
<td>All</td>
<td>All</td>
<td>Set Results Summary</td>
<td>Final test TJN</td>
</tr>
</tbody>
</table>
### HBM
**AEC-Q100-002**

**ElectroStatic Discharge/ Human Body Model Classification (HBM):**
- Test @ 250/500/1000/1500/2000 Volts
- See AEC-Q100-002 for classification levels.
- **TEST @ RH 2KV min.**
- 3 units per Voltage level
- 1
- Lot C @200V, @500V, @1000V, @1500V, @2000V
- Levels below 2000V require customer approval.

### CDM
**AEC-Q100-011**

**ElectroStatic Discharge/ Charged Device Model Classification (CDM):**
- Test @ 250/500/750 Volts
- See AEC-Q100-011 for classification levels.
- **Timed RO of 96hrs MAX.**
- **TEST @ RH Corner pins => 750V; All other pins => 500V**
- 3 units per Voltage level
- 1
- Lot C @250V, @500V, @750V all pins
- Levels below 750V for corner pins and below 500V for all other pins require customer approval.

### LU
**JESD78 plus AEC-Q100-004**

**Latch-up (LU):**
- Test per JEDEC JESD78 with the AEC-Q100-004 requirements.
- **Ta = Maximum operating temperature**
- **Vsupply = Maximum operating voltage**
- **TEST @ RH**
- 6
- 1
- 6
- Lot C 0/6

### ED
**AEC-Q100-009, Freescale 48A spec**

**Electrical Distribution (ED):**
- **TEST @ RH**
- Cpk = or > 1.67
- 30
- 3
- 90
- Complete

### FG
**AEC-Q100-007**

**Fault Grading (FG):**
- FG shall be = or > 90% for qual units
- FG% > 95% w/iddq

### GL
**AEC-Q100-006**

**Electro-Thermally Induced Gate Leakage (GL):**
- 155°C, 2.0 min, +400/-400 V
- **Timed RO of 96 hrs MAX.**
- For all failures, perform unbiased bake (4hrs/125°C, or 2hrs/150°C) and retest; recovered units are GL failures.
- **TEST @ R**
- 6
- 0
- 0
- Pass
- D260 M05C Die Qualification 0/8

### EMC
**SAE J1752-3 - Radiated Emissions**

**Electromagnetic Compatibility (EMC):**
- See AEC Q100 Appendix 5 for test applicability; done on case-by-case basis per customer/Freescale agreement
- **<40dBuV**
- 150KHz - 1GHz
- 1
- 0
- 0
- N/A
- D260 M05C Die Qualification 0/1

---

**Generic Data List:**

<table>
<thead>
<tr>
<th>Quartz #</th>
<th>Mask Set</th>
<th>Product Qual Description / Part Number(s)</th>
<th>Critical Parameter</th>
<th>Critical Parameter</th>
<th>Die Size</th>
<th>Mold Compound/ Die Attach</th>
<th>CAB Number</th>
<th>CAB Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>28881</td>
<td>M34C</td>
<td>9S12C32</td>
<td>UIN</td>
<td>ATMC</td>
<td>3.90x3.189</td>
<td>TN/ TR/ ACH 200H/ T0M</td>
<td>2006</td>
<td>25 Jan 2006</td>
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<table>
<thead>
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<th>Revision</th>
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<th>Description</th>
<th>Author</th>
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<td>1.0</td>
<td>16-Apr-07</td>
<td>1st draft</td>
<td>V. Kim</td>
</tr>
<tr>
<td>1.1</td>
<td>28-Feb-07</td>
<td>1st draft (die qual added)</td>
<td>V. Kim</td>
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<td>1.2</td>
<td>1-Aug-07</td>
<td>Peer Review</td>
<td>V. Kim</td>
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<td>1.3</td>
<td>1-Jul-08</td>
<td>Updated HTOL duration</td>
<td>V. Kim</td>
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<td>1.4</td>
<td>1-Jun-08</td>
<td>Updated qual results</td>
<td>V. Kim</td>
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<td>1.5</td>
<td>26-Aug-08</td>
<td>Finalized with qual results and peer reviewed</td>
<td>V. Kim</td>
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<td>1.6</td>
<td>29-Apr-08</td>
<td>Updated format</td>
<td>V. Kim</td>
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</table>
## AEC-Q100F Qualification Results Summary

To qualify NPI 9S08DZ60 M74K in a 48 LQFP Package

<table>
<thead>
<tr>
<th>Stress Test</th>
<th>Reference</th>
<th>Test Conditions</th>
<th>End Point Requirements</th>
<th>Minimum Sample Size</th>
<th># of Lots</th>
<th>Total Units including spares</th>
<th>Results</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PC</strong></td>
<td>JESD22-</td>
<td>Preconditioning (PC): PC required for SMDs only. MSL 3 @ 260°C, +5/-0°C</td>
<td>TEST @ RH</td>
<td>All surface mount devices prior to THB, HAST, AC, and TC and as required per test conditions.</td>
<td>Pass</td>
<td>Generic Data 9S12C32 0/693</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>A113 J-STD-020</td>
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</tr>
<tr>
<td><strong>HAST</strong></td>
<td>JESD22-</td>
<td>Highly Accelerated Stress Test (HAST): PC before HAST (for SMDs only): Required HAST = 130°C/85%RH for 96 hrs. Timed RO of 48hrs. MAX</td>
<td>TEST @ RH</td>
<td>77</td>
<td>0</td>
<td>0</td>
<td>Pass</td>
<td>Generic Data 9S12C32 0/231</td>
</tr>
<tr>
<td></td>
<td>A101 A110</td>
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</tr>
<tr>
<td><strong>AC</strong></td>
<td>JESD22-</td>
<td>Autoclave (AC): PC before AC (for SMDs only): Required AC = 121°C/100%RH/15 psig for 96 hrs Timed RO of 2-48hrs. MAX</td>
<td>TEST @ R</td>
<td>77</td>
<td>0</td>
<td>0</td>
<td>Pass</td>
<td>Generic Data 9S12C32 0/231</td>
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</tr>
<tr>
<td><strong>TC</strong></td>
<td>JESD22-</td>
<td>Temperature Cycle (TC): PC before TC (for SMDs only): Required TC = -65°C to 150°C for 500 cycles. WBP after TC on 5 devices from 1 lot; 2 bonds per corner and one mid-bond per side on each device. Record which pins were used.</td>
<td>TEST @ HC WBP =&gt; 3 grams</td>
<td>77</td>
<td>0</td>
<td>0</td>
<td>Pass</td>
<td>Generic Data 9S12C32 0/231 WBP 0/5</td>
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<td>A104 AEC Q100-Appendix 3</td>
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<tr>
<td><strong>HTSL</strong></td>
<td>JESD22-</td>
<td>High Temperature Storage Life (HTSL): 150°C for 1008 hrs or 175°C for 504hrs (Devices incorporating NVM shall receive 'NVM endurance preconditioning'(EDR) prior to this test, and special NVM test sequencing after this test; see AEC-Q100 for details) Timed RO = 96hrs. MAX</td>
<td>TEST @ RHC</td>
<td>77</td>
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<td>Pass</td>
<td>See EDR</td>
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</table>

### TEST GROUP B - ACCELERATED LIFETIME SIMULATION TESTS

<table>
<thead>
<tr>
<th>Stress Test</th>
<th>Reference</th>
<th>Test Conditions</th>
<th>End Point Requirements</th>
<th>Minimum Sample Size</th>
<th># of Lots</th>
<th>Total Units including spares</th>
<th>Results</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>HTOL</strong></td>
<td>AEC Q100-</td>
<td>High Temperature Operating Life (HTOL): Ta = 125°C for 1008 hrs (Devices incorporating NVM shall receive 'NVM endurance preconditioning'(EDR) prior to this test, and special NVM test sequencing after this test; see AEC-Q100 for details) Timed RO of 96hrs. MAX</td>
<td>TEST @ RHC</td>
<td>77</td>
<td>0</td>
<td>0</td>
<td>Pass</td>
<td>See 64 LQFP DZ60 Qual Data</td>
</tr>
<tr>
<td></td>
<td>005</td>
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</tr>
</tbody>
</table>
### ELFR

**AEC Q100-008**

**Early Life Failure Rate (ELFR):**

- Ta = 125°C for 48 hrs
- Timed RO of 48 hrs MAX

**TEST @ RHC**

<table>
<thead>
<tr>
<th>End Point Requirements</th>
<th>Minimum Sample Size</th>
<th># of Lots</th>
<th>Total Units including spares</th>
<th>Results</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>0</td>
<td>Pass</td>
<td>See 64 LQFP DZ60 Qual Data</td>
</tr>
</tbody>
</table>

### EDR

**AEC Q100-005**

**NVM Endurance, Data Retention, and Operational Life (EDR):**

- (also known as NVM Endurance Preconditioning)
- W/E Cycling @ 125°C for 504 hrs
- Page Mode
- Timed RO of 48 hrs MAX

**TEST @ RHC**

<table>
<thead>
<tr>
<th>End Point Requirements</th>
<th>Minimum Sample Size</th>
<th># of Lots</th>
<th>Total Units including spares</th>
<th>Results</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>0</td>
<td>Pass</td>
<td>See 64 LQFP DZ60 Qual Data</td>
</tr>
</tbody>
</table>

**AEC Q100-005**

**NVM Endurance, Data Retention, and Operational Life (EDR):**

- (also known as NVM Endurance Preconditioning)
- W/E Cycling @ -40°C for 504 hrs
- Page Mode
- Timed RO of 48 hrs MAX

**TEST @ RHC**

<table>
<thead>
<tr>
<th>End Point Requirements</th>
<th>Minimum Sample Size</th>
<th># of Lots</th>
<th>Total Units including spares</th>
<th>Results</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>0</td>
<td>Pass</td>
<td>See 64 LQFP DZ60 Qual Data</td>
</tr>
</tbody>
</table>

### TEST GROUP C - PACKAGE ASSEMBLY INTEGRITY TESTS

<table>
<thead>
<tr>
<th>Stress Test</th>
<th>Reference</th>
<th>Test Conditions</th>
<th>End Point Requirements</th>
<th>Minimum Sample Size</th>
<th># of Lots</th>
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<th>Results</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>WBS</strong></td>
<td>AEC Q100-001</td>
<td>Wire Bond shear (WBS)</td>
<td>Cpk = or &gt; 1.67</td>
<td>30 bonds from minimum 5 units</td>
<td>0</td>
<td>0</td>
<td>Pass</td>
<td>Performed by Assembly Site during qual lot builds D260 M05C Package Qualification 0/5</td>
</tr>
<tr>
<td><strong>WBP</strong></td>
<td>MILSTD883-2011</td>
<td>Wire Bond Pull (WBP): Cpk = or &gt; 1.67</td>
<td>30 bonds from minimum 5 units</td>
<td>0</td>
<td>0</td>
<td>Pass</td>
<td>Performed by Assembly Site during qual lot builds D260 M05C Package Qualification 0/5</td>
<td></td>
</tr>
<tr>
<td><strong>SD</strong></td>
<td>JESD22-B102</td>
<td>Solderability (SD): &gt;95% lead coverage of critical areas</td>
<td>15</td>
<td>0</td>
<td>0</td>
<td>Pass</td>
<td>Production Burn In is required prior to SD. D260 M05C Package Qualification 0/15 @KLM post production burn-in</td>
<td></td>
</tr>
<tr>
<td><strong>PD</strong></td>
<td>JESD22-B100</td>
<td>Physical Dimensions (PD): Cpk = or &gt; 1.67</td>
<td>10</td>
<td>0</td>
<td>0</td>
<td>Pass</td>
<td>Performed by Assembly Site during qual lot builds D260 M05C Package Qualification 0/30 Cpk &gt; 1.67</td>
<td></td>
</tr>
<tr>
<td><strong>DIM &amp; BOM</strong></td>
<td></td>
<td>Dimensional (DIM): PPE to verify PD results against valid 98A drawing. BOM Verification (BOM): PPE to verify qual lot ERF BOM is accurate.</td>
<td></td>
<td></td>
<td></td>
<td>DIM: Complete BOM: Complete</td>
<td>Complete</td>
<td></td>
</tr>
</tbody>
</table>

### TEST GROUP E - ELECTRICAL VERIFICATION TESTS

<table>
<thead>
<tr>
<th>Stress Test</th>
<th>Reference</th>
<th>Test Conditions</th>
<th>End Point Requirements</th>
<th>Minimum Sample Size</th>
<th># of Lots</th>
<th>Total Units including spares</th>
<th>Results</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>TEST</strong></td>
<td>Freescale 48A</td>
<td>Pre- and Post Functional / Parametrics (TEST): Test software shall meet requirements of AEC-Q100-007. Testing performed to the limits of device</td>
<td>0 Fails</td>
<td>All</td>
<td>All</td>
<td>All</td>
<td>See Results Summary</td>
<td>Final Test Site: TJN</td>
</tr>
</tbody>
</table>
### HBM

**AEC-Q100-002**

**ElectroStatic Discharge/ Human Body Model Classification (HBM):**
- Test @ 250/500/1000/1500/2000 Volts
- See AEC-Q100-002 for classification levels.

**Test @ RH**
- 2KV min.
- 3 units per Voltage level
- 0/0 Pass
- DZ60 M05C Die Qualification 0/15

### CDM

**AEC-Q100-011**

**ElectroStatic Discharge/ Charged Device Model Classification (CDM):**
- Test @ 250/500/750 Volts
- See AEC-Q100-011 for classification levels.
- **Timed RO of 96hrs MAX.**

**Test @ RH**
- Corner pins >= 750V; All other pins >= 500V
- 3 units per Voltage level
- 0/0 Pass
- Levels below 750V for corner pins and below 500V for all other pins require customer approval.
- DZ60 M05C Package Qualification 0/9

### LU

**JESD78 plus AEC-Q100-004**

**Latch-up (LU):**
- Test per JEDEC JESD78 with the AEC-Q100-004 requirements.
- **Tа=** Maximum operating temperature
- V_supply = Maximum operating voltage

**Test @ RH**
- 6 units
- 0/0 Pass
- DZ60 M05C Die Qualification 0/8

### ED

**AEC-Q100-009, Freescale 48A spec**

**Electrical Distribution (ED)**
- **Cpk = or > 1.67**
- 30 units
- 0/0 Pass
- See 64 LQFP DZ60 Qual Data

### FG

**AEC-Q100-007**

**Fault Grading (FG):**
- FG shall be = or > 90% for qual units
- FG% > 95% with IDDQ

### Stress Test

<table>
<thead>
<tr>
<th>Reference</th>
<th>Test Conditions</th>
<th>End Point Requirements</th>
<th>Minimum Sample Size</th>
<th># of Lots</th>
<th>Total Units including spares</th>
<th>Results</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>AEC-Q100-006</td>
<td><strong>Electro-Thermally Induced Gate Leakage (GL):</strong> 155°C, 2.0 min, +400/-400 V <strong>Timed RO of 96 hrs MAX.</strong> For all failures, perform unbiased bake (4hrs/125°C, or 2hrs/150°C) and retest; recovered units are GL failures.</td>
<td>TEST @ R</td>
<td>6</td>
<td>0</td>
<td>0</td>
<td>Pass</td>
<td>DZ60 M05C Die Qualification 0/6</td>
</tr>
<tr>
<td>SAE J1752/3</td>
<td><strong>Radiated Emissions</strong></td>
<td><strong>Electromagnetic Compatibility (EMC):</strong> see AEC Q100 Appendix 5 for test applicability; done on case-by-case basis per customer/Freescale agreement</td>
<td>&lt;40dBuV 150kHz - 1GHz</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>N/A</td>
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### Generic Data List:

<table>
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<tr>
<th>Quartz #</th>
<th>Mask Set</th>
<th>Product-qual Description / Part Number(s)</th>
<th>Critical Parameter</th>
<th>Critical Parameter</th>
<th>Critical Parameter Die Size</th>
<th>Mold Compound/Die attach</th>
<th>CAB Number</th>
<th>CAB Date</th>
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<tr>
<td>586688050678B39 B34</td>
<td>93H05C</td>
<td>DZ60</td>
<td>TJN</td>
<td>ATMC</td>
<td>4.360 x 3.366</td>
<td>MC HTACHIR 9200HF10M</td>
<td>2007</td>
<td>39 35358</td>
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<table>
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<tr>
<th>Revision</th>
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<th>Description</th>
<th>Author</th>
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<tbody>
<tr>
<td>1.0</td>
<td>16-Apr-07</td>
<td>1st draft</td>
<td>V. Kim</td>
</tr>
<tr>
<td>1.1</td>
<td>25-Apr-08</td>
<td>Updated with generic data</td>
<td>V. Kim</td>
</tr>
</tbody>
</table>

### Additional Information:

- **EMC (see AEC Q100 Appendix 5 for test applicability; done on case-by-case basis per customer/Freescale agreement):**
  - <40dBuV 150kHz - 1GHz

- **DZ60 M05C Die Qualification:**
  - 0/15, 0/15, 0/6, 0/8

- **DZ60 M05C Package Qualification:**
  - 0/9

- **Customer Approval Required:**
  - Levels below 750V for corner pins and below 500V for all other pins require customer approval.
### AEC-Q100F Qualification Plan/Results Summary

**Objective:** To qualify NPI 9S08DZ60 M74K in a 32 LQFP Package

**Freescale PN:** 9S08DZ60  
**Part Name:** Longhorn  
**Customer Name(s):** Multiple  
**PN(s):**  
**Plan or Results:** Results  
**Revision # & Date:** 1.1 29 April 2008  
*(See Revision History in Notes)*

| Technology: | 0.25um Embedded Flash  
| Package: | 32 LQFP 7x7 Package Code (6300)  
| Design Engr: | Rubens Takiguti  
| QUARTZ Tracking #: | TBD  

**Fab / Assembly / Final Test Sites:**  
FSL-ATMC/FSL-TJN-FM/FSL-TJN-FM  
**Product Engr:** Todd Flynn and David Rosas  
**PPE Approval (for DIM/BOM results):** Matt Zapico  
**Signature & Date:** Matt Zapico  
*(Signature/Date shown below may be electronic)*

| Maskset#: | 0/M74K  
| Rev#: | NPI PROE  
| Prod. Package Engr: | Valerie Kim  
| NPI PROE Approval Signature & Date: | Valerie Kim  

| Die Size (in mm): | W x L x T 3.3900x3.3660  
| Design Engr: | Rubens Takiguti  
| Phone #: | Todd Flynn and David Rosas  
| CAB Approval Signature & Date: | 08180192M  
| Signature & Date: | April 29, 2008  

**Part Operating Temp. Grade:**  
JESD22-A113  
**Grade:** 1  
**-40°C to +125°C**  
**Trace/DateCode:**  
LOT A  
LOT B  
LOT C  
**AC**  
**JESD22-A102**  
**A118**  
**Autoclave (AC):**  
PC before AC (for SMDs only): Required  
**AC = 121°C/100%RH/15 psig for 96 hrs.**  
**Timed RO of 2-48hrs. MAX**  
**TEST @ R**  
77  
0  
0  
**Pass**  
See 48 LQFP DZ60 Package Qual Data.

**TC**  
**JESD22-A104**  
**AEC-Q100 Appendix 3**  
**Temperature Cycle (TC):**  
PC before TC (for SMDs only): Required  
**TC = -65°C to 150°C for 500 cycles.**  
**WB test on 5 devices from 1 lot; 2 bonds per corner and one mid-bond per side on each device. Record which pins were used.**  
**TEST @ HC**  
WBP =/> 3 grams  
77  
0  
0  
**Pass**  
See 48 LQFP DZ60 Package Qual Data.

**HTSL**  
**JESD22-A103**  
**High Temperature Storage Life (HTSL):**  
150°C for 1008 hrs or 175°C for 504hrs (Devices incorporating NVM shall receive 'NVM endurance preconditioning'/EDR prior to this test, and special NVM test sequencing after this test; see AEC-Q100 for details)  
**Timed RO = 96hrs. MAX**  
**TEST @ RHC**  
77  
0  
0  
**Pass**  
See EDR

**Example:** TESTS HIGHLIGHTED IN YELLOW WERE PERFORMED FOR THIS STUDY

**GROUP A - ACCELERATED ENVIRONMENTAL STRESS TESTS**

<table>
<thead>
<tr>
<th>Stress Test</th>
<th>Reference</th>
<th>Test Conditions</th>
<th>End Point Requirements</th>
<th>Minimum Sample Size</th>
<th># of Lots</th>
<th>Total Units including spares</th>
<th>Results</th>
<th>Comments</th>
</tr>
</thead>
</table>
| **PC**      | JESD22- A113 J-STD-020 | Preconditioning (PC):  
PC required for SMDs only.  
MSL 3 @ 260°C, +5/-0°C  
**TEST @ RH** | All surface mount devices prior to THB, HAST, AC, and TC and as required per test conditions. | Pass | See 48 LQFP DZ60 Package Qual Data. |
| **HAST**    | JESD22- A101 A110 | Highly Accelerated Stress Test (HAST):  
PC before HAST (for SMDs only): Required  
HAST = 130°C/85%RH for 96 hrs.  
**Timed RO of 48hrs. MAX**  
**TEST @ RH** | 77 | 0 | 0 | Pass | See 48 LQFP DZ60 Package Qual Data. |
| **AC**      | JESD22- A102 A118 | Autoclave (AC):  
PC before AC (for SMDs only): Required  
**AC = 121°C/100%RH/15 psig for 96 hrs.**  
**Timed RO of 2-48hrs. MAX**  
**TEST @ R** | 77 | 0 | 0 | Pass | See 48 LQFP DZ60 Package Qual Data. |
| **TC**      | JESD22- A104 AEC-Q100 Appendix 3 | Temperature Cycle (TC):  
PC before TC (for SMDs only): Required  
**TC = -65°C to 150°C for 500 cycles.**  
**WB test on 5 devices from 1 lot; 2 bonds per corner and one mid-bond per side on each device. Record which pins were used.**  
**TEST @ HC**  
WBP =/> 3 grams  
77 | 0 | 0 | Pass | See 48 LQFP DZ60 Package Qual Data. |

**GROUP B - ACCELERATED LIFETIME SIMULATION TESTS**

<table>
<thead>
<tr>
<th>Stress Test</th>
<th>Reference</th>
<th>Test Conditions</th>
<th>End Point Requirements</th>
<th>Minimum Sample Size</th>
<th># of Lots</th>
<th>Total Units including spares</th>
<th>Results</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>TEST GROUP B - ACCELERATED LIFETIME SIMULATION TESTS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Stress Test**  
**Reference**  
**Test Conditions**  
**End Point Requirements**  
**Minimum Sample Size**  
**# of Lots**  
**Total Units including spares**  
**Results**  
**Lot ID-(#Rej/SS) NA=Not Applicable**  
**Comments**  

### Assorted Test Descriptions

**HTOL (High Temperature Operating Life)**

- **AEC Q100-005**: High Temperature Operating Life (HTOL): Ta = 125°C for 1008 hrs
- (Devices incorporating NVM shall receive 'NVM endurance preconditioning'(EDR) prior to this test, and special NVM test sequencing after this test; see AEC-Q100 for details)
- Timed RO of 96hrs. MAX

**ELFR (Early Life Failure Rate)**

- **AEC Q100-008**: Early Life Failure Rate ELFR: Ta = 125°C for 48 hrs

**EDR (NVM Endurance, Data Retention, and Operational Life)**

- **AEC Q100-005**: NVM Endurance, Data Retention, and Operational Life (EDR): (also known as NVM Endurance Preconditioning)
  - W/E Cycling @ 125 C
  - DRB @ 175 C for 504 hrs
  - Page Mode
  - Timed RO of 48hrs. MAX

**TEST GROUP C - PACKAGE ASSEMBLY INTEGRITY TESTS**

<table>
<thead>
<tr>
<th>Stress Test</th>
<th>Reference</th>
<th>Test Conditions</th>
<th>End Point Requirements</th>
<th>Minimum Sample Size</th>
<th># of Lots</th>
<th>Total Units including spares</th>
<th>Results Lot ID-(#Rej/SS) NA=Not Applicable</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>WBS</td>
<td>AEC Q100-001</td>
<td>Wire Bond shear (WBS)</td>
<td>Cpk = or &gt; 1.67</td>
<td>30 bonds from minimum 5 units</td>
<td>0</td>
<td>0</td>
<td>Pass</td>
<td>Performed by Assembly Site during qual lot builds DZ60 M05C Package Qualification 0/5</td>
</tr>
<tr>
<td>WBP</td>
<td>MilStd883-2011</td>
<td>Wire Bond Pull (WBP): Cond. C or D</td>
<td>Cpk = or &gt; 1.67</td>
<td>30 bonds from minimum 5 units</td>
<td>0</td>
<td>0</td>
<td>Pass</td>
<td>Performed by Assembly Site during qual lot builds DZ60 M05C Package Qualification 0/6</td>
</tr>
<tr>
<td>SD</td>
<td>JESD22-B102</td>
<td>Solderability (SD): 8hr,(1 hr. for Au-plated leads) Steam age prior to test. If production burn-in is done, samples must also undergo burn-in prior to SD.</td>
<td>&gt;95% lead coverage of critical areas</td>
<td>15</td>
<td>0</td>
<td>0</td>
<td>Pass</td>
<td>Production Burn In is required prior to SD. DZ60 M05C Package Qualification 0/15 @KLM post production burn-in</td>
</tr>
<tr>
<td>PD</td>
<td>JESD22-B100</td>
<td>Physical Dimensions(PD): PD per FSL 98A drawing</td>
<td>Cpk = or &gt; 1.67</td>
<td>10</td>
<td>0</td>
<td>0</td>
<td>Pass</td>
<td>Performed by Assembly Site during qual lot builds DZ60 M05C Package Qualification 0/30 Cpk &gt; 1.67</td>
</tr>
</tbody>
</table>

**DIM & BOM**

- **PPE** to verify PD results against valid 98A drawing.
- **BOM Verification (BOM)**: PPE to verify qual lot ERF BOM is accurate.

### TEST GROUP E - ELECTRICAL VERIFICATION TESTS
<table>
<thead>
<tr>
<th>Stress Test</th>
<th>Reference</th>
<th>Test Conditions</th>
<th>End Point Requirements</th>
<th>Minimum Sample Size</th>
<th># of Lots</th>
<th>Total Units including spares</th>
<th>Results</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>TEST</td>
<td>Freescale 48A</td>
<td>Pre- and Post Functional / Parametrics (TEST): Test software shall meet requirements of AEC-Q100-007. Testing performed to the limits of device specification in temperature and limit value.</td>
<td>0 Fails</td>
<td>All</td>
<td>All</td>
<td>All</td>
<td>See Results Summary</td>
<td>Final Test Site: TJN</td>
</tr>
<tr>
<td>HBM</td>
<td>AEC-Q100-002</td>
<td>ElectroStatic Discharge/ Human Body Model Classification (HBM): Test @ 250/500/1000/1500/2000 Volts. See AEC-Q100-002 for classification levels.</td>
<td>TEST @ RH 2KV min.</td>
<td>3 units per Voltage level</td>
<td>0</td>
<td>0</td>
<td>Pass</td>
<td>DZ60 M05C Die Qualification 0/15</td>
</tr>
<tr>
<td>CDM</td>
<td>AEC-Q100-011</td>
<td>ElectroStatic Discharge/ Charged Device Model Classification (CDM): Test @ 250/750 Volts. See AEC-Q100-011 for classification levels. <em>Timed RO of 96hrs MAX.</em></td>
<td>TEST @ RH Corner pins =&gt; 750V; All other pins =&gt; 500V</td>
<td>3 units per Voltage level</td>
<td>0</td>
<td>0</td>
<td>Pass</td>
<td>Levels below 750V for corner pins and below 500V for all other pins require customer approval. 9S08DZ60 M05C 0/9</td>
</tr>
<tr>
<td>LU</td>
<td>JESD78 plus AEC-Q100-004</td>
<td>Latch-up (LU): Test per JEDEC JESD78 with the AEC-Q100-004 requirements. T= Maximum operating temperature Vsupply = Maximum operating voltage</td>
<td>TEST @ RH</td>
<td>6</td>
<td>0</td>
<td>0</td>
<td>Pass</td>
<td>DZ60 M05C Die Qualification 0/6</td>
</tr>
<tr>
<td>ED</td>
<td>AEC-Q100-009, Freescale 48A spec</td>
<td>Electrical Distribution (ED): Cpk = or &gt; 1.67</td>
<td>TEST @ RH Cpk = or &gt; 1.67</td>
<td>30</td>
<td>0</td>
<td>0</td>
<td>Pass</td>
<td>See 64 LQFP DZ60 Qual Data</td>
</tr>
<tr>
<td>FG</td>
<td>AEC-Q100-007</td>
<td>Fault Grading (FG): FG shall be = or &gt; 90% for qual units</td>
<td>FG% &gt; 95% w/iddq</td>
<td>FG% &gt; 95% w/iddq</td>
<td>FG% &gt; 95% w/iddq</td>
<td>FG% &gt; 95% w/iddq</td>
<td>FG% &gt; 95% w/iddq</td>
<td>FG% &gt; 95% w/iddq</td>
</tr>
<tr>
<td>GL</td>
<td>AEC-Q100-006</td>
<td>Electro-Thermally Induced Gate Leakage (GL): 155°C, 2.0 min, +400/-400 V. Timed RO of 96 hrs MAX. For all failures, perform unbiased bake (4hrs/125°C, or 2hrs/150°C) and retest; recovered units are GL failures.</td>
<td>TEST @ R</td>
<td>6</td>
<td>0</td>
<td>0</td>
<td>Pass</td>
<td>DZ60 M05C Die Qualification 0/6</td>
</tr>
<tr>
<td>EMC</td>
<td>SAE J1752/3 - Radiated Emissions</td>
<td>Electromagnetic Compatibility (EMC): See AEC Q100 Appendix 5 for test applicability; done on case-by-case basis per customer/Freescale agreement</td>
<td>&lt;40dBuV 10KHz - 1MHz</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Pass</td>
<td>DZ60 M05C Die Qualification 0/1</td>
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**Generic Data List:**

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<th>Quartz #</th>
<th>Mask Set</th>
<th>Product-Qual Description / Part Number(s)</th>
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<th>Critical Parameter</th>
<th>Die Size</th>
<th>Mold Compound/Die attach</th>
<th>CAB Number</th>
<th>CAB Date</th>
<th>Revision Date</th>
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<td>3.90x3.189</td>
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<td>2006</td>
<td>25 Jan 2006</td>
<td>16-Apr-07</td>
<td>1st draft</td>
<td>V. Kim</td>
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<td>58658/59998/78839</td>
<td>10M05C</td>
<td>DZ60</td>
<td>TJN</td>
<td>ATMC</td>
<td>3.39x3.366</td>
<td>MC HITACHI 9200HF10M</td>
<td>2007 39 39398</td>
<td>26 Sep 2007</td>
<td>26-Apr-07</td>
<td>Updated with generic data</td>
<td>V. Kim</td>
</tr>
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<table>
<thead>
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