# Hip7 NVM Probe Flow Optimization Summary
# 28 October 2010

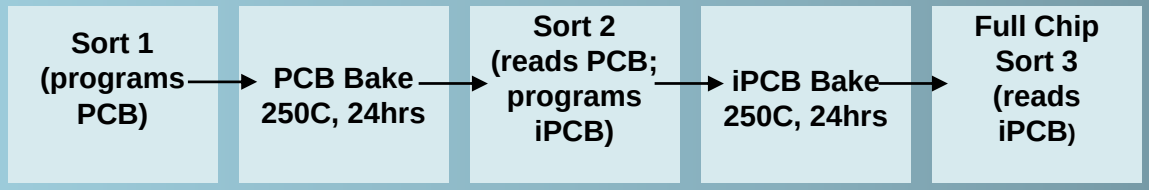
Christine Boey / D. Migl



freescale™
semiconductor

# Freescale Hip7NVM Probe Flow Optimization

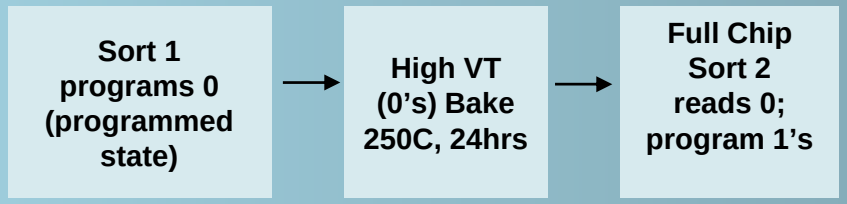
## Current Production Probe Flow




The current flow utilizes the Physical/Inverse CheckerBoard (PCB/iPCB) patterns in 2 inserts.

- Sort1 programs the device into the PCB state which is read at Sort2 after a 24hr bake.
- Sort2 verifies the PCB pattern and then programs the part into an iPCB pattern to be read at Sort3 after a 24hr bake.
- Both high and low read states are covered in this flow.

## Optimized New Probe Flow




The optimized flow utilizes solid all 0's patterns.

- The high Vt bake (all 0's) accelerates any charge loss failures after Sort1.
- Sort2 verifies all 0's pattern before programming all 1's.
- The all 1's pattern is verified at Burn-In to check for any charge gain.
- Burn-In and Final Test flows remain unchanged.



freescale semiconductor

# Freescale NVM Background & History

- The original double wafer bake Checkerboard/iCheckerboard probe flow was implemented on Hip7 as a safe launch procedure.

- To improve customer cycle time and to streamline the test flow for optimal manufacturability, Freescale has completed qualification of a single data retention wafer bake probe flow for Hip7 NVM products.

- Freescale is committed to delivering zero defects on its eNVM technologies and to preventing customer application failures due to data retention bit flip issues.

- 0.13um 1T flash is the 3rd of 4 generations of floating gate bitcell technology, and we are confident in our knowledge of 1T flash cell behavior.





freescale™ semiconductor

# 1T FG Bitflip History

- Risk assessment for this process change included review of historical CDR1 and CDR3 customer returns.
  - This process change deemed non-critical for these failure mechanisms

| 1T FG Bitflips | | | Customer Return? | | | ECC Correctable? |
|---|---|---|---|---|---|---|
| Fail Type | Description | Root Cause | CDR1 | CDR3 | HiP7 | |
| Charge Gain (Adjacent Bit) | Resistive short between floating gates. Vt shift observed only when adjacent bits on same row have opposite polarity. | Process Defectivity (Residual Poly) | Yes | Yes | No | Yes |
| Charge Loss (Single Bit) | E-Field enhanced thermal emission. Thermally accelerated and highly reproducable. | Process Defectivity (Typically NDF but likely caused by small physical anomaly) | Yes | Yes | No | Yes |
| Charge Gain (Single Bit) | E-Field enhanced thermal emission. Thermally accelerated and highly reproducable. | Process Defectivity (Typically NDF but likely caused by small physical anomaly) | Yes | No | No | Yes |
| Charge Loss (Intermittant Single Bit) | E-Field enhanced leakage. | Process Defectivity (Silicon Pit in Drain) | Yes | No | No | Yes |
| Charge Gain (Bit Cluster) | Multiple bits gaining charge | Process Defectivity (Poly Protrusion) | Yes | No | No | Yes |
| Charge Gain during Device Operation (Multiple Bits) | Unselected bitline incorrectly biased to Vdd | Process Defectivity (Dislocation) | No | Yes | No | Yes |

Note: ECC implemented on 0.13um and beyond.
NDF = no defect found





freescale™ semiconductor

# Hip7 NVM Probe Flow Optimization
# DOE Summary

An evaluation was carried out to validate the risk level of the flow change.

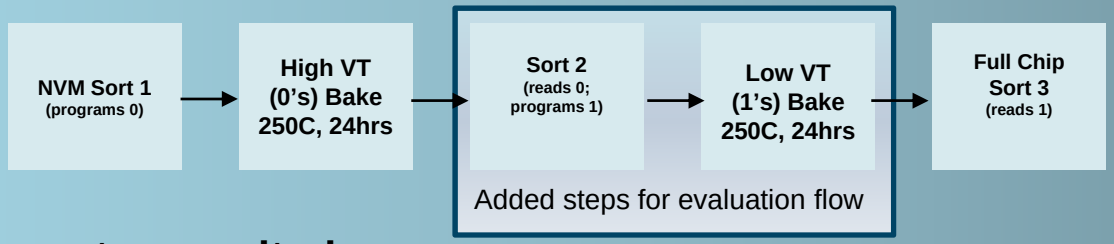
- 5 wafer lots were equally split with approximately 60 wafers in each split.
- Low Vt and High Vt Data Retention tests were performed after 24hrs bake.

Program and Erase Margin read values were performed to catch single bit failures.

The production flow was emulated with the following flash patterns:

**Evaluation:**

- Sort1 : All 0's (programmed state)
- Sort 2 : All 1's (erased state; added step for evaluation flow only)



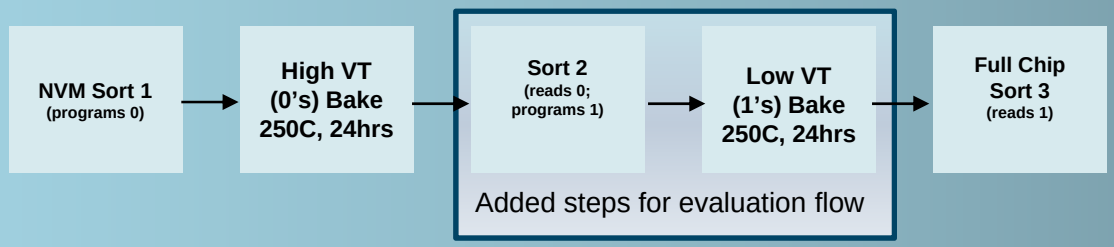

**Acceptance criteria**:

- 0 retention failures for 1's.



freescale semiconductor

# Hip7 NVM Probe Flow Optimization DOE Results




| | Control Flow | Evaluation Flow | Pass Acceptance? |
|---|---|---|---|
| Retention failures for 1's | 0 | 0 | Yes |

**Summary:**

- **The results meet acceptance criteria.**
- **The quality risk of implementing the change is negligible.**



freescale semiconductor ™

# Hip7 NVM Probe Flow Optimization
# Risk Assessment

- Hip7NVM data retention bake optimization is protected by advanced screening techniques.
  - Advanced Outlier Detection (AOL) methods and ECC further reduce the risk of latent data retention failures.
  - Burn-In and Final Test flows remain unchanged.
- C90NVM technology, utilizing the same bitcell technology with smaller geometry, has completed qualification with a similar wafer bake.
- 0.13um devices have had no latent CQI returns with 26M shipped due to single bit data retention failures.
- Freescale is confident that the single bake optimization from checkerboard/icheckerboard to single solid pattern wafer bake on 0.13um flash adds no additional latency failure rate risk.



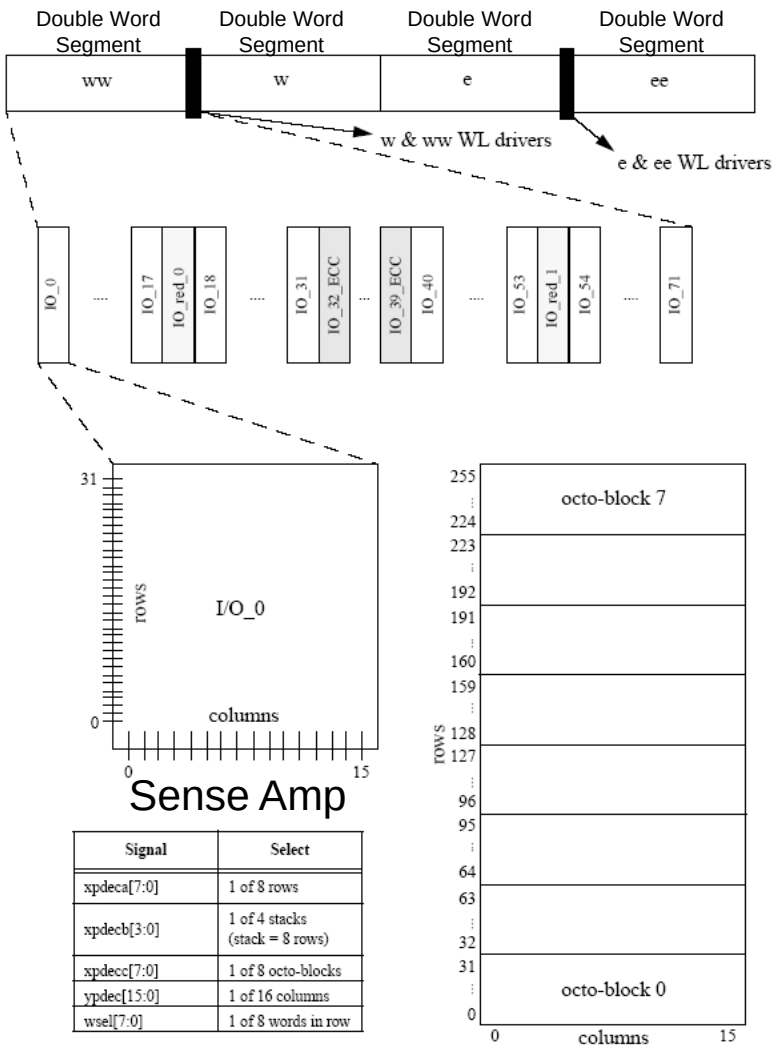
freescale™ semiconductor

# Back-up



freescale™
semiconductor

# ECC Insurance – HiP7 Design and Beyond




| Signal | Select |
|---|---|
| xpdeca[7:0] | 1 of 8 rows |
| xpdecb[3:0] | 1 of 4 stacks (stack = 8 rows) |
| xpdecc[7:0] | 1 of 8 octo-blocks |
| ypdec[15:0] | 1 of 16 columns |
| wsel[7:0] | 1 of 8 words in row |

- ECC can correct any single bit failure within a 64 bit word boundary.
- A 64 bit word is read by reading the same column from each sense amp in a double word segment. I.e. every 16$^{th}$ column.
- All adjacent bit customer return failures would be corrected.

**All bit flip customer return failures seen on parts without ECC would have be corrected.**

- NOTE: All die leaving Freescale are naturally good. ECC only used by customer for insurance for latent defect mechanisms.





freescale semiconductor






freescale™
semiconductor