Freescale Semiconductor
Reference Manual Addendum

MPC5645SRMAD
Rev. 1, 07/2013

MPC5645S Reference Manual Addendum

This addendum describes corrections or updates to the *MPC5645S Reference Manual*, file named as MPC5645S RM. Please check our website at http://www.freescale.com/PowerPC, for the latest updates.

Table of Contents

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1 Addendum for Rev 6.0 OF MPC5645S RM

1.1 Updated Figure 3-1 “176-pin LQFP pinout”

- Location: Page 92 of MPC5645S RM Rev. 6.
- Changes made: “DCU_LITE_TAG” added for PK10.

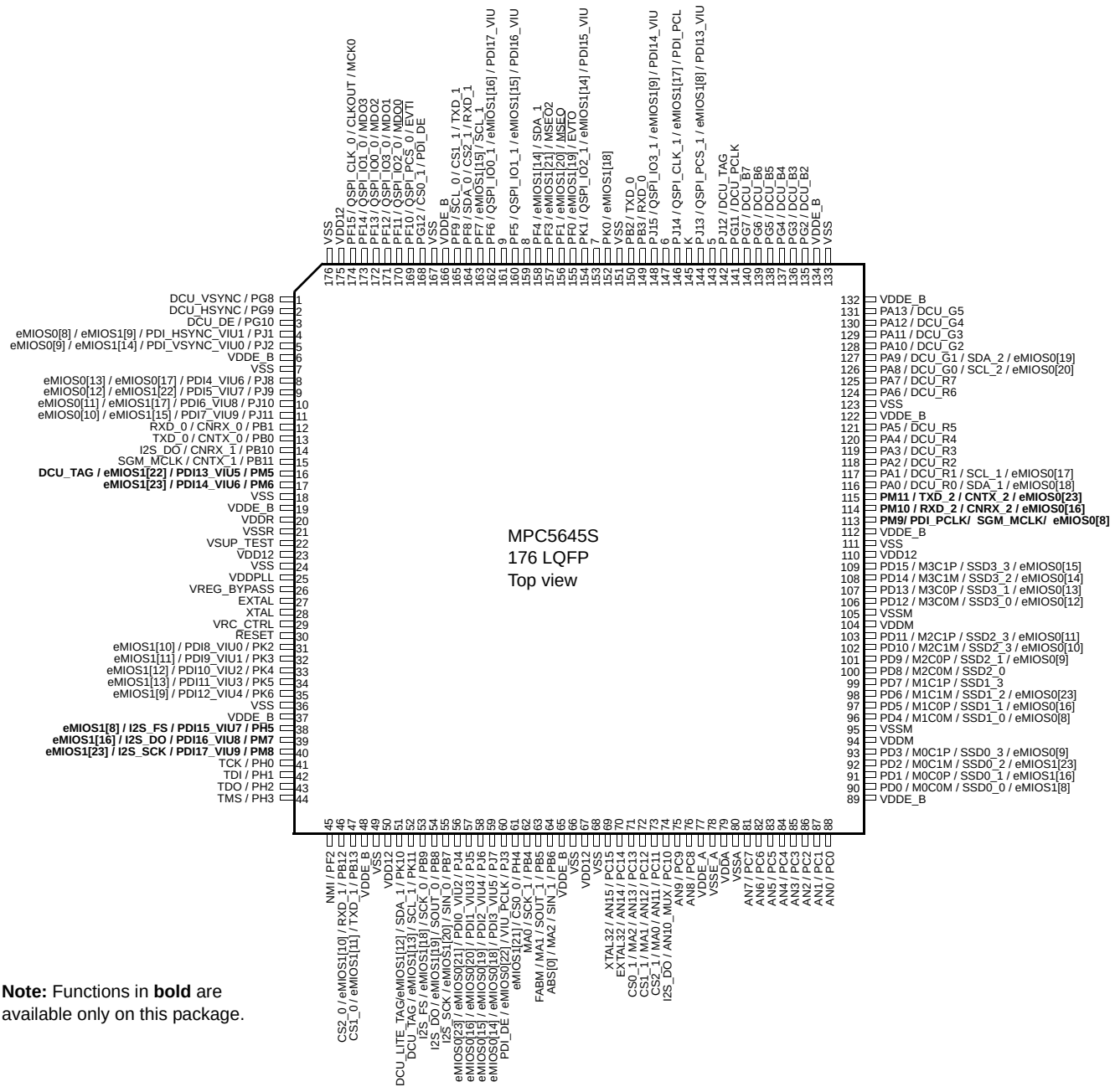

Figure: 176-pin LQFP pinout

1.2 Updated Figure 3-2 “208-pin LQFP pinout”

- Location: Page 93 of MPC5645S RM Rev. 6.
- Changes made:
  - “DCU_LITE_TAG” added and “DCU_TAG” removed for PK10.
  - “DCU_TAG” added and “DCULITE_TAG” removed for PK11.
  - “I2C1_SDA” added for PL0.
  - “I2C1_SCL” added for PL1.

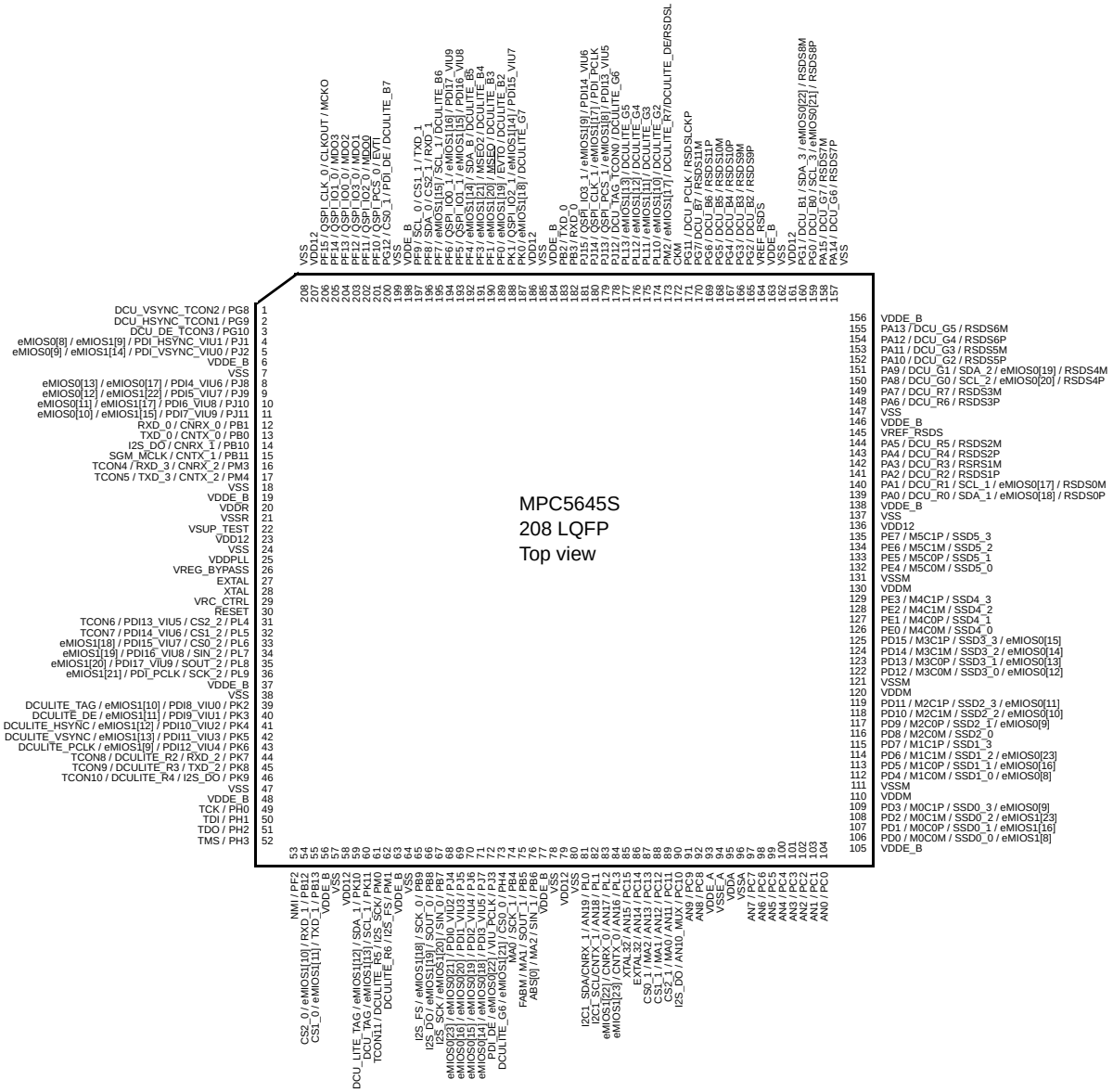

Figure: 208-pin LQFP pinout

1.3 Updated Table 5 “Port pin summary”

- Location: Page 105 of MPC5645S RM Rev. 6.
- Changes made: Updated “Function” entry for PB[10], PK[11], PL[0], and PL[1], updated “Peripheral” entry for PK[11], PL[0], and PL[1].

Port pin summary

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PORT B											
PB[10]	PCR[26]	Option 0 Option 1 Option 2 Option 3	GPIO[26] CANRX_1 I2S_DO/PWMO —	—	SIUL FlexCAN_1 SGM —	I/O	S	None, none	14	14	W2
PORT K											
PK[11]	PCR[132]	Option 0 Option 1 Option 2 Option 3	GPIO[132] SCL_1 eMIOS1[13] DCU_TAG	—	SIUL I^2C_1 PWM/Timer DCU	I/O	S	None, None	52	60	AC9
PORT L											
PL[0]	PCR[133]	Option 0 Option 1 Option 2 Option 3	GPIO[133] — CANRX_1 I2C1_SDA	ANS[19]	SIUL — FlexCAN_1 I2C1	I/O	M / ANALOG	None, None	—	81	AE22
PL[1]	PCR[134]	Option 0 Option 1 Option 2 Option 3	GPIO[134] — CANTX_1 I2C1_SCL	ANS[18]	SIUL — FlexCAN_1 I2C1	I/O	M / ANALOG	None, None	—	82	AE21

NOTES:

1 Alternate functions are chosen by setting the values of the PCR[PA] bitfields inside the SIUL module.
PCR[PA] = 00 selects Option 0
PCR[PA] = 01 selects Option 1
PCR[PA] = 10 selects Option 2
PCR[PA] = 11 selects Option 3
This is intended to select the output functions. To use one of the input functions, the PCR[IBE] bit must be written to ‘1’, regardless of the values selected in the PCR[PA] bitfields. For this reason, the value corresponding to an input only function is reported as “—”.

2 Special functions are enabled independently from the standard digital pin functions. Enabling standard I/O functions in the PCR registers may interfere with their functionality. ADC functions are enabled using the PCR[APC] bit; other functions are enabled by enabling the respective module.

[3] Using the PSMI registers in the System Integration Unit Lite (SIUL), different pads can be multiplexed to the same peripheral input. Please see the SIUL chapter of the *MPC5645S Microcontroller Reference Manual* for details.

[4] See the “Pad types” section for an explanation of the letters in this column.

[5] Reset configuration is given as I/O direction and pull, e.g., “Input, pullup”.

1.4 Updated Table 43-14 “Peripheral input pin selection”

- Location: Page 1489 of MPC5645S Rev. 6.
- Changes made: Updated entries for PSMI[48], PSMI[49], PSMI[50], PSMI[51], PSMI[52], PSMI[53], and PSMI[54].

Table: Peripheral input pin selection

PSMI register	SIUL address offset	Peripheral input	Mapping of input pin to peripheral input [1]
PSMI[48]	0x530	I2C_SCL_1	0:PCR[1] 1:PCR[77] 2:PCR[132] 3:PCR[134]
PSMI[49]	0x531	I2C_SDA_1	0:PCR[0] 1:PCR[74] 2:PCR[131] 3:PCR[133]
PSMI[50]	0x532	LIN0_RXD	0:PCR[19] 1:PCR[17]
PSMI[51]	0x533	LIN1_RXD	0:PCR[28] 1:PCR[78]
PSMI[52]	0x534	LIN2_RXD	0:PCR[128] 1:PCR[157] 2:PCR[163]
PSMI[53]	0x535	LIN3_RXD	0:PCR[150] 1:PCR[171]
PSMI[54]	0x536	EVTI	0:PCR[80] 1:EVTI

NOTES:
1 Connecting a peripheral input to a pad requires assigning both the PSMI value for the peripheral input and the pad assignment in the SIU_PCR register for that signal.

1.5 Updated Table 49-1 “Wakeup vector mapping”

- Location: Page 1591 of MPC5645S RM Rev. 6
- Changes made: Updated “Function” entries for PB10 and PL0.

Table: Wakeup vector mapping

Wakeup vector	Wakeup number	Function				Package		
		Port	#1	#2	#3	176	208	416
0	WKUP4	PB10	CANRX_1	I2S_DO	—	x	x	x
1	WKUP15	PL0	AN[19]	CANRX_1	I2C1_SDA	—	x	x

2 Revision History

Table 1 provides a revision history for this document.

Table 1. Addendum Revision History Table

Rev. Number	Substantive Changes	Date of Release
1.0	First release: • Updated “176-pin LQFP pinout” figure. • Updated “208-pin LQFP pinout” figure. • Updated “Port pin summary” table. • Updated “Peripheral input pin selection” table. • Updated “Wakeup vector mapping” table.	07/2013