0.25um ATMC and TSMCFAB3/11 KLM QFP Copper Wire Qualification (PCN 16253)

1. Objective

This report describes the Freescale Austin Technology Manufacturing Center (ATMC) fab site for 0.25um QFP devices electrical distribution data on 23um Cu wire versus baseline on 25um Au wire.

Current Wire:
25um Au wire

Proposed New Wire:
23um Cu wire

2. General Information

Product Family: S9S08DZ128/S12XD/S12D/S12C/S12B/S12XHZ/S12K/S12H/S12HZ
Fab site: ATMC
Mask set: M78G/M23S/M42E/M80F/M84E/L01Y/M34C/M66G/L59W/M65G/M89C
Package(s): 80QFP/100LQFP/112LQFP/144LQFP
Assembly Site: Freescale Kuala Lumpur, Kuala Lumpur, Malaysia

3. Method

Two data sets taken from selected key product, 30 units in each set at T0 analysis:

1. 30 units from 23um Cu wire diameter qual lot from ATMC fab site
2. 30 units from 25um Au wire diameter control lot from ATMC fab site

Both qualification and control lots are tested to standard production final test flow. Electrical distribution data generated from the selected key parametric tests with Freescale standard criteria CPK > 1.67 and shift ≤ 15%, justification will be provided if otherwise.

4. Data and Summary:

4.1. Electrical Distribution Table:

Selected Evaluation Vehicle: S912XD (144LQFP) M23S
The ED data from Selected Evaluation Vehicle will be representing the parts stated in section 2 General Information

				Au Wire			Cu Wire					
				Temp	-40	C	Temp	-40	C	Shift within +/- 1 sigma or less than 15% to spec	Shift within +/- 1 sigma or less than 15% to spec	Comment
Parameter Name, as in Datasheet	**Units**	**Lower Spec Limit** (NA if no spec)	**Upper Spec Limit** (NA if no spec)	**Avg**	**Std**	**Cpk**	**Avg**	**Std**	**Cpk**			
Input Leakage on I/O (V=0)	uA	-1	1	-0.0011	0.0008	394.01	-0.0016	0.0012	266.38	-0.06%	-0.06%	PASS
Input Leakage on I/O (V=5)	uA	-1	1	0.0055	0.0010	338.10	0.0061	0.0014	228.72	0.06%	0.06%	PASS
Internal pull up current test at VILmax (VDD=5)	uA	-130	NA	-91.3763	1.3829	9.31	-98.6536	2.0091	5.20	-18.84%	NA	Justify, difference insignigicant < 10uA
Internal pull up current test at VILmax (VDD=3v3)	uA	-60	NA	-39.4336	0.4805	14.27	-41.7899	0.9918	6.12	-11.46%	NA	PASS
Internal pull down current test at VIHmin (VDD=5)	uA	NA	130	84.4427	2.6240	5.79	82.3978	3.1132	5.10	NA	-4.49%	PASS
Internal pull down current test at VIHmin (VDD=3v3)	uA	NA	60	35.0580	1.2912	6.44	33.7198	2.1819	4.01	NA	-5.37%	PASS
Output full drive low test, 5V	mA	10	NA	30.5904	1.2633	5.43	33.7621	1.4990	5.28	15.40%	NA	Justify, Avg move away from LSL
Output full drive high test, 5V	mA	NA	-10	-21.3377	0.5514	6.85	-22.4549	0.6907	6.01	NA	-9.85%	PASS
Output full drive low test, 3V3	mA	4.75	NA	11.8808	0.4452	5.34	11.8686	0.5049	4.70	-0.17%	NA	PASS
Output full drive high test, 3V3	mA	NA	-4	-8.4875	0.1905	7.85	-8.9548	0.2448	6.75	NA	-10.41%	PASS
Stop IDD	uA	NA	100	13.7155	1.0022	28.70	13.8614	0.9154	31.37	NA	0.17%	PASS
Wait IDD	mA	NA	95	73.6712	0.8791	8.09	72.7806	1.4936	4.96	NA	-4.18%	PASS
Wait IDD RTI	mA	NA	10	5.1745	0.0768	20.93	5.3527	0.0834	18.58	NA	3.69%	PASS
Run IDD	mA	NA	110	91.0158	1.5414	4.11	91.3324	2.0959	2.97	NA	1.67%	PASS
CRG self clock mode frequency test at dc_max	MHz	1.0	5.5	1.9923	0.1240	2.67	2.5792	0.1526	3.45	59.14%	16.73%	Justify, Avg move towards center of limit
CRG self clock mode frequency test at dc_min	MHz	1.0	5.5	1.8687	0.1172	2.47	2.3784	0.1381	3.33	58.67%	14.04%	Justify, Avg move towards center of limit
ATD IREF_VRH, 2 ATD blocks on (5V)	mA	NA	750	0.1820	0.0024	106155.24	0.1876	0.0052	48048.73	NA	0.00%	PASS
ATD IREF_VRH, 2 ATD block on (3.3V)	mA	NA	500	0.1190	0.0029	56820.80	0.1236	0.0039	43196.99	NA	0.00%	PASS
ATD IREF_VRH, 1 ATD block on (5V)	mA	NA	375	0.1820	0.0034	36554.74	0.1878	0.0050	25096.25	NA	0.00%	PASS
ATD IREF_VRH, 1 ATD block on (3.3V)	mA	NA	250	0.1190	0.0031	27111.71	0.1227	0.0034	24402.53	NA	0.00%	PASS
Output voltage core (rpm)	V	1.40	2.75	2.2800	0.0478	3.27	2.3715	0.0449	2.81	10.40%	19.47%	Justify, Avg move towards center of limit
Output voltage PLL (rpm)	V	1.25	2.75	2.2800	0.0414	3.78	2.3651	0.0391	3.28	8.26%	18.10%	Justify, Avg move towards center of limit
Output voltage core (fpm)	V	2.35	2.75	2.5000	0.0115	4.33	2.5141	0.0118	4.64	9.37%	5.62%	PASS
Output voltage PLL (fpm)	V	2.35	2.75	2.5100	0.0138	3.87	2.5242	0.0082	7.09	8.85%	5.90%	PASS

				Au Wire			Cu Wire			Shift within +/- 1 sigma or less than 15% to spec	Shift within +/- 1 sigma or less than 15% to spec	Comment
				Temp	125	C	Temp	125	C			
Parameter Name, as in Datasheet	**Units**	**Lower Spec Limit** (NA if no spec)	**Upper Spec Limit** (NA if no spec)	**Avg**	**Std**	**Cpk**	**Avg**	**Std**	**Cpk**			
Input Leakage on I/O (V=0)	uA	-1	1	0.0016	0.0052	64.03	0.0036	0.0064	52.29	0.20%	0.20%	PASS
Input Leakage on I/O (V=5)	uA	-1	1	0.0664	0.0079	39.60	0.0607	0.0106	29.62	-0.53%	-0.61%	PASS
Internal pull up current test at VILmax (VDD=5)	uA	-130	NA	-56.7000	1.1822	20.67	-57.3656	1.1802	20.52	-0.91%	NA	PASS
Internal pull up current test at VILmax (VDD=3v3)	uA	-60	NA	-23.9000	0.5551	21.68	-24.0172	0.5600	21.42	-0.32%	NA	PASS
Internal pull down current test at VIHmin (VDD=5)	uA	NA	130	48.6000	1.4866	18.25	52.4822	1.1216	23.04	NA	4.77%	PASS
Internal pull down current test at VIHmin (VDD=3v3)	uA	NA	60	20.9314	0.6226	20.92	23.1988	0.5487	22.36	NA	5.80%	PASS
Output full drive low test, 5V	mA	10	NA	19.4763	0.4792	6.59	19.7012	0.3776	8.56	2.37%	NA	PASS
Output full drive high test, 5V	mA	NA	-10	-14.2369	0.2405	5.87	-14.3481	0.2191	6.61	NA	-2.62%	PASS
Output full drive low test, 3V3	mA	4.75	NA	7.4379	0.1727	5.19	7.6576	0.1463	6.62	8.17%	NA	PASS
Output full drive high test, 3V3	mA	NA	-4	-5.5009	0.0993	5.04	-5.5739	0.0923	5.68	NA	-4.86%	PASS
Stop IDD	uA	NA	7000	471.8501	72.4564	30.03	677.6832	28.8765	72.98	NA	3.15%	PASS
Wait IDD	mA	NA	95	77.3721	0.7230	8.13	78.9502	0.9787	5.47	NA	8.95%	PASS
Wait IDD RTI	mA	NA	10	5.4781	0.0914	16.50	5.7517	0.0795	17.82	NA	6.05%	PASS
Run IDD	mA	NA	110	97.2745	0.8999	4.71	95.3158	1.4772	3.31	NA	-15.39%	Justify, Avg move away from USL
CRG self clock mode frequency test at dc_max	MHz	1.0	5.5	3.2175	0.2071	3.57	3.5135	0.0679	9.75	13.35%	12.97%	PASS
CRG self clock mode frequency test at dc_min	MHz	1.0	5.5	3.0682	0.1891	3.65	3.3462	0.0739	9.71	13.44%	11.43%	PASS
ATD IREF_VRH, 2 ATD blocks on (5V)	mA	NA	750	0.2120	0.0027	92600.00	0.2217	0.0037	67339.57	NA	0.00%	PASS
ATD IREF_VRH, 2 ATD block on (3.3V)	mA	NA	500	0.1391	0.0030	56151.46	0.1451	0.0032	51819.64	NA	0.00%	PASS
ATD IREF_VRH, 1 ATD block on (5V)	mA	NA	375	0.2128	0.0030	41490.82	0.2220	0.0047	26852.29	NA	0.00%	PASS
ATD IREF_VRH, 1 ATD block on (3.3V)	mA	NA	250	0.1385	0.0032	25636.99	0.1452	0.0030	27412.32	NA	0.00%	PASS
Output voltage core (rpm)	V	1.40	2.75	1.8838	0.0390	4.14	1.9468	0.0361	5.05	13.02%	7.27%	PASS
Output voltage PLL (rpm)	V	1.25	2.75	2.0289	0.0366	6.57	2.0419	0.0326	7.25	1.67%	1.80%	PASS
Output voltage core (fpm)	V	2.35	2.75	2.5299	0.0104	5.79	2.5394	0.0120	5.27	5.29%	4.33%	PASS
Output voltage PLL (fpm)	V	2.35	2.75	2.5425	0.0095	6.75	2.5521	0.0098	6.75	5.03%	4.66%	PASS

"Shift analysis" refers to analysis of shift of the distribution mean towards the nearest specification limit:
"% Shift (USL) = {Mean(new)-Mean(old)} / {Upper Spec Limit-Mean(old)}
% Shift (LSL) = {Mean(new)-Mean(old)} / {Mean(old)-Lower Spec Limit}

4.2. Summary:

From the above data, it was verified that the requirements and acceptance criteria was achieved. Justifications were provided for shift of > 15%.

5. Document History:

Rev	Date	Originator
O	29th Apr 2014	Tan Wei Ming

Appendix A: Justifications for any Shifts > 15%

Justification as provided in the table.