
0.25um ATMC and TSMCFAB3/11 KLM QFP Copper Wire Qualification (PCN 16253)

1. Objective

This report describes the Taiwan Semiconductor Manufacturing Company Fab 3/11 (TSMCFAB3/11) fab site for 0.25um QFP devices electrical distribution data on 23um Cu wire versus baseline on 25um Au wire.

Current Wire:

25um Au wire

Proposed New Wire:

23um Cu wire

2. General Information

Product Family: S12XD/S12D/S12C/S12B/S12XHZ/S12K/S12H/S12HZ

Fab site: TSMCFAB3/11

Mask set: L15Y/L91N/L45J/L09S/L33V/L40K/L74N/L80R/L16Y/L86D/L94R/M48V/K78X

Package(s): 80QFP/80LQFP/112LQFP/144LQFP

Assembly Site: Freescale Kuala Lumpur, Kuala Lumpur, Malaysia

3. Method

Two data sets taken from selected key product, 30 units in each set at T0 analysis:

1. 30 units from 23um Cu wire diameter qual lot from TSMCFAB3 fab site
2. 30 units from 25um Au wire diameter control lot from TSMCFAB3 fab site

Both qualification and control lots are tested to standard production final test flow. Electrical distribution data generated from the selected key parametric tests with Freescale standard criteria $CPK > 1.67$ and $shift \leq 15\%$, justification will be provided if otherwise.

4. Data and Summary:

4.1. Electrical Distribution Table:

Selected Evaluation Vehicle: S912XD (144LQFP) L15Y

The ED data from Selected Evaluation Vehicle will be representing the parts stated in section 2 General Information

Parameter Name, as in Datasheet	Units	Lower Spec Limit (NA if no spec)	Upper Spec Limit (NA if no spec)	Au Wire			Cu Wire			Shift within +/- 1 sigma or less than 15% to spec	Shift within +/- 1 sigma or less than 15% to spec	Comment
				Temp	-40	C	Temp	-40	C			
				Avg	Std	Cpk	Avg	Std	Cpk			
Input Leakage on I/O (V=0)	uA	-1	1	-0.0011	0.0008	394.01	0.0003	0.0010	336.07	0.13%	0.13%	PASS
Input Leakage on I/O (V=5)	uA	-1	1	0.0055	0.0010	338.10	0.0060	0.0013	250.55	0.05%	0.06%	PASS
Internal pull up current test at VILmax (VDD=5)	uA	-130	NA	-91.3763	1.3829	9.31	-88.5125	2.3200	5.96	7.41%	NA	PASS
Internal pull up current test at VILmax (VDD=3v3)	uA	-60	NA	-39.4336	0.4805	14.27	-37.2614	1.0746	7.05	10.56%	NA	PASS
Internal pull down current test at VIHmin (VDD=5)	uA	NA	130	84.4427	2.6240	5.79	82.4468	3.0638	5.17	NA	-4.38%	PASS
Internal pull down current test at VIHmin (VDD=3v3)	uA	NA	60	35.0580	1.2912	6.44	33.6607	1.1869	7.40	NA	-5.60%	PASS
Output full drive low test, 5V	mA	10	NA	30.5904	1.2633	5.43	30.3583	1.2496	5.43	-1.13%	NA	PASS
Output full drive high test, 5V	mA	NA	-10	-21.3377	0.5514	6.85	-20.7938	0.6557	5.49	NA	4.80%	PASS
Output full drive low test, 3V3	mA	4.75	NA	11.8808	0.4452	5.34	11.7546	0.4268	5.47	-1.77%	NA	PASS
Output full drive high test, 3V3	mA	NA	-4	-8.4875	0.1905	7.85	-8.1781	0.2464	5.65	NA	6.89%	PASS
Stop IDD	uA	NA	100	13.7155	1.0022	28.70	15.3332	1.2267	23.01	NA	1.87%	PASS
Wait IDD	mA	NA	95	73.6712	0.8791	8.09	74.3075	1.2288	5.61	NA	2.98%	PASS
Wait IDD RTI	mA	NA	10	5.1745	0.0768	20.93	5.1260	0.0694	23.40	NA	-1.01%	PASS
Run IDD	mA	NA	110	91.0158	1.5414	4.11	90.5494	1.3480	4.81	NA	-2.46%	PASS
CRG self clock mode frequency test at dc_max	MHz	1.00	5.50	1.9923	0.1240	2.67	2.2239	0.1320	3.09	23.35%	6.60%	Justify, Avg move towards center of limit
CRG self clock mode frequency test at dc_min	MHz	1.00	5.50	1.8687	0.1172	2.47	2.1004	0.1257	2.92	26.67%	6.38%	Justify, Avg move towards center of limit
ATD IREF_VRH, 2 ATD blocks on (5V)	mA	NA	750	0.1820	0.0024	106155.24	0.1924	0.0029	85790.84	NA	0.00%	PASS
ATD IREF_VRH, 2 ATD block on (3.3V)	mA	NA	500	0.1190	0.0029	56820.80	0.1266	0.0027	62265.20	NA	0.00%	PASS
ATD IREF_VRH, 1 ATD block on (5V)	mA	NA	375	0.1820	0.0034	36554.74	0.1926	0.0025	49291.74	NA	0.00%	PASS
ATD IREF_VRH, 1 ATD block on (3.3V)	mA	NA	250	0.1190	0.0031	27111.71	0.1260	0.0022	37075.30	NA	0.00%	PASS
Output voltage core (rpm)	V	1.40	2.75	2.2800	0.0478	3.27	2.2910	0.0456	3.36	1.25%	2.33%	PASS
Output voltage PLL (rpm)	V	1.25	2.75	2.2800	0.0414	3.78	2.2943	0.0387	3.93	1.39%	3.05%	PASS
Output voltage core (fpm)	V	2.35	2.75	2.5000	0.0115	4.33	2.5070	0.0114	4.58	4.68%	2.81%	PASS
Output voltage PLL (fpm)	V	2.35	2.75	2.5100	0.0138	3.87	2.5151	0.0120	4.58	3.21%	2.14%	PASS

Parameter Name, as in Datasheet	Units	Lower Spec Limit (NA if no spec)	Upper Spec Limit (NA if no spec)	Au Wire			Cu Wire			Shift within +/- 1 sigma or less than 15% to spec	Shift within +/- 1 sigma or less than 15% to spec	Comment	
				Temp		125	Temp		125				C
				Avg	Std	Cpk	Avg	Std	Cpk				
Input Leakage on I/O (V=0)	uA	-1	1	0.0016	0.0052	64.03	0.0022	0.0069	48.54	0.06%	-0.17%	PASS	
Input Leakage on I/O (V=5)	uA	-1	1	0.0664	0.0079	39.60	0.0615	0.0105	29.66	-0.46%	-0.52%	PASS	
Internal pull up current test at VILmax (VDD=5)	uA	-130	NA	-56.7000	1.1822	20.67	-54.2976	1.7449	14.46	3.28%	NA	PASS	
Internal pull up current test at VILmax (VDD=3v3)	uA	-60	NA	-23.9000	0.5551	21.68	-22.8477	0.7506	16.50	2.92%	NA	PASS	
Internal pull down current test at VIHmin (VDD=5)	uA	NA	130	48.6000	1.4866	18.25	45.9985	2.3645	11.84	NA	-3.20%	PASS	
Internal pull down current test at VIHmin (VDD=3v3)	uA	NA	60	20.9314	0.6226	20.92	19.8288	0.9709	13.79	NA	-2.82%	PASS	
Output full drive low test, 5V	mA	10	NA	19.4763	0.4792	6.59	20.0485	0.5242	6.39	6.04%	NA	PASS	
Output full drive high test, 5V	mA	NA	-10	-14.2369	0.2405	5.87	-14.4320	0.2381	6.21	NA	-4.61%	PASS	
Output full drive low test, 3V3	mA	4.75	NA	7.4379	0.1727	5.19	7.6560	0.1868	5.18	8.11%	NA	PASS	
Output full drive high test, 3V3	mA	NA	-4	-5.5009	0.0993	5.04	-5.5866	0.0843	6.27	NA	-5.71%	PASS	
Stop IDD	uA	NA	7000	471.8501	72.4564	30.03	892.9852	95.8014	21.25	NA	6.45%	PASS	
Wait IDD	mA	NA	95	77.3721	0.7230	8.13	77.0648	1.0873	5.50	NA	-1.74%	PASS	
Wait IDD RTI	mA	NA	10	5.4781	0.0914	16.50	5.3321	0.0942	16.52	NA	-3.23%	PASS	
Run IDD	mA	NA	110	97.2745	0.8999	4.71	97.2169	1.1970	3.56	NA	-0.45%	PASS	
CRG self clock mode frequency test at dc_max	MHz	1.00	5.50	3.2175	0.2071	3.57	3.1609	0.1659	4.34	-2.55%	-2.48%	PASS	
CRG self clock mode frequency test at dc_min	MHz	1.00	5.50	3.0682	0.1891	3.65	3.0116	0.1610	4.17	-2.74%	-2.33%	PASS	
ATD IREF_VRH, 2 ATD blocks on (5V)	mA	NA	750	0.2120	0.0027	92600.00	0.2181	0.0028	89936.51	NA	0.00%	PASS	
ATD IREF_VRH, 2 ATD block on (3.3V)	mA	NA	500	0.1391	0.0030	56151.46	0.1422	0.0022	74669.29	NA	0.00%	PASS	
ATD IREF_VRH, 1 ATD block on (5V)	mA	NA	375	0.2128	0.0030	41490.82	0.2172	0.0031	39841.51	NA	0.00%	PASS	
ATD IREF_VRH, 1 ATD block on (3.3V)	mA	NA	250	0.1385	0.0032	25636.99	0.1428	0.0029	28764.37	NA	0.00%	PASS	
Output voltage core (rpm)	V	1.40	2.75	1.8838	0.0390	4.14	1.9243	0.0447	3.91	8.38%	4.68%	PASS	
Output voltage PLL (rpm)	V	1.25	2.75	2.0289	0.0366	6.57	2.0596	0.0407	5.66	3.94%	4.25%	PASS	
Output voltage core (fpm)	V	2.35	2.75	2.5299	0.0104	5.79	2.5269	0.0121	4.88	-1.68%	-1.37%	PASS	
Output voltage PLL (fpm)	V	2.35	2.75	2.5425	0.0095	6.75	2.5391	0.0132	4.79	-1.73%	-1.61%	PASS	

“Shift analysis” refers to analysis of shift of the distribution mean towards the nearest specification limit:

$$\% \text{ Shift (USL)} = \frac{\{\text{Mean}(\text{new}) - \text{Mean}(\text{old})\}}{\{\text{Upper Spec Limit} - \text{Mean}(\text{old})\}}$$

$$\% \text{ Shift (LSL)} = \frac{\{\text{Mean}(\text{new}) - \text{Mean}(\text{old})\}}{\{\text{Mean}(\text{old}) - \text{Lower Spec Limit}\}}$$

4.2. Summary:

From the above data, it was verified that the requirements and acceptance criteria was achieved. Justifications were provided for shift of > 15%.

5. Document History:

Rev	Date	Originator
0	29 th Apr 2014	Tan Wei Ming

Appendix A: Justifications for any Shifts > 15%

Justification as provided in the table.