Appendix A
Release Notes for Revision 3

A.1 Revision history

A.1.1 General changes throughout document

- In the Chip Configuration chapter:
  - Updated the table "Cache regions" in the section "Local memory controller region assignment"
  - Updated the tables "ADC0 channel assignment" and "ADC1 channel assignment"
- In the Clock Distribution chapter:
  - Updated the table "Clock definitions"
  - Updated the table "Clock summary"
  - Updated the figure "TSI low-power clock generation"

A.1.2 About This Document chapter changes

- No substantial content changes

A.1.3 Introduction chapter changes

- No substantial content changes

A.1.4 Chip Configuration chapter changes

- Clarified the "Wake-up Sources" section within the "Low-Leakage Wake-up Unit (LLWU) Configuration" section. Renamed the "LLWU inputs" table to "Wakeup sources for LLWU inputs", removed the multiplexed signals and provided the pin name only. Added a reference to the signal multiplexing table for the individual signal options.
- In ADCx Channel Assignment, updated AD27 and AD29 input signal description.
- Clarified ADC and PGA Reference Options section.
- In LPTMR pulse counter input options section, clarified LPTMR_CSR[TPS]=11 chip input.
- Added notes to VREF Overview and DAC External Trigger Input Connections sections.
A.1.5 Memory Map chapter changes

- Added the new section "Read-after-write sequence and required serialization of memory operations"
- For the table "System memory map", corrected the access and slave port information for the DRAM controller
- Added the area to which SDRAM and Flexbus is aliased to in System Memory map

A.1.6 Clock Distribution chapter changes

- Added note to Debug trace clock section.
- In Clock Summary table, added RTC_CLKOUT clock.
- Updated Debug trace clock diagram.
- Updated the "Internal clocking requirements" section.
- For the "USB FS OTG Controller clocking" section, added this note: "The MCGFLLCLK does not meet the USB jitter specifications for certification."
- Clarified OSC clock names in Clock definitions section.
- Updated USB HS controller clock generation section.

A.1.7 Reset and Boot chapter changes

- For the section "Reset pin filter", added more information about the separate LPO filter in the LLWU.
- For the section "Multipurpose clock generator loss-of-clock (LOC)"; updated note about unexpected loss of clock reset events.

A.1.8 Power Management chapter changes

- No substantial content changes
A.1.9 Security chapter changes
• No substantial content changes

A.1.10 Debug chapter changes
• For the "Debug Components Description" table in the "Introduction", replaced the "JTAG-AP" row with a row for "MDM-AP".

A.1.11 Signal Multiplexing and Signal Descriptions chapter changes
• No substantial content changes

A.1.12 PORT changes
• No substantial content changes

A.1.13 SIM changes
• In the SOPT2 register, updated the FBSL field description.
• In the SCGC5 register, updated the REGFILE field description to be reserved and always 1.
• In the MCR register, updated the ULPICLKOB field description to be reserved.

A.1.14 RCM changes
• Removed the reference SIM_COP register.

A.1.15 PMC changes
• No substantial content changes
A.1.16  LLWU changes

- No substantial content changes

A.1.17  MCM changes

- No substantial content changes

A.1.18  Crossbar switch module changes

- Unused PRS[Mn] fields now show as Reserved.
- PRS register reset value changed to ‘X’ with footnote.
- All AXBS_PRS Reserved field reset values changed to 0.
- Corrected AXBS_CRSn reset value.
- Unimplemented CRS[HPEn] bits show as Reserved and have reset value of 0.
- Changed reset values of PRS and CRS registers to 0. Added footnote to refer to chip-specific info.
- Added the note "See the chip-specific crossbar information for the reset value of this register." to the beginning of the Priority Registers Slave (AXBS_PRSn) and Control Register (AXBS_CRSn) sections.
- Changed occurrences of "AXBS" to "Crossbar Switch."

A.1.19  MPU module changes

Changed EAR and EDR reset values to 0000_0000
- Rearranged reset value and reset information in notes of RGDn_WORD2, RGDn_WORD3 and RGDAAC registers

A.1.20  AIPS module changes

- MPRn register(s): Now show correct access-privilege fields based on logical master ID. Added master ID to brief descriptions. Corrected statement re: master ID assignment.
- MPRn[MPROT] reset value is now 0b0000 when field is not present (Reserved).
- Changed AIPS_MPRA reset value to 0x7000_0000. Non-preset master fields changed to RW.
- Removed list item about dedicated clock enables in Features.
- Removed paragraph about AHB data-phase cycles in Functional description.
- Memory map/register definition: Incorporated minor editorial changes.
### A.1.21 DMAMUX module changes

<table>
<thead>
<tr>
<th>Change Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>In section Enabling and configuring sources, the DMA channel number used in the example from channel 2 to channel 1.</td>
</tr>
<tr>
<td>In DMA channels with periodic triggering capability section, modified Figure DMAMUX triggered channels.</td>
</tr>
<tr>
<td>Editorial (non-technical) fixes in some sections.</td>
</tr>
<tr>
<td>Added section Always-enabled DMA sources.</td>
</tr>
<tr>
<td>Changed the register name from CHCONFIG to CHCFG.</td>
</tr>
<tr>
<td>Updated note in the register description for Channel Configuration register (DMAMUX_CHCFGn) as follows: &quot;Setting multiple CHCFG registers with the same source value will result in unpredictable behavior. This is true, even if a channel is disabled (ENBL==0).&quot;</td>
</tr>
<tr>
<td>In the section &quot;Enabling and configuring sources,&quot; updated DMAMUX_BASE_ADDR in example code.</td>
</tr>
<tr>
<td>Changed code examples in &quot;Enabling and configuring sources&quot; section, from #define DMAMUX_BASE_ADDR 0xFC084000/* Example only ! <em>/ to #define DMAMUX_BASE_ADDR 0x40021000/</em> Example only ! */.</td>
</tr>
</tbody>
</table>

### A.1.22 eDMA module changes

<table>
<thead>
<tr>
<th>Change Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>In the DMAx_CR section, added &quot;from high to low&quot; in the sentences about round-robin arbitration. For example, &quot;For group round robin arbitration, the group priorities are ignored and the groups are cycled through (from high to low group number) without regard to priority.&quot;</td>
</tr>
<tr>
<td>Updated wording of first paragraph in Dynamic scatter/gather section.</td>
</tr>
<tr>
<td>Changed the following two sentences in the &quot;Error Reporting and handling&quot; section:</td>
</tr>
<tr>
<td>&quot;When a system-bus error occurs, the channel terminates after the read or write transaction, which is already pipelined after errant access, has completed.&quot; to &quot;When a system bus error occurs, the channel terminates after the next transfer. Due to pipeline effect, the next transfer is already in progress when the bus error is received by the eDMA.&quot;</td>
</tr>
<tr>
<td>&quot;The occurrence of any error causes the eDMA engine to stop the active channel immediately, and the appropriate channel bit in the eDMA error register is asserted.&quot; to &quot;The occurrence of any error causes the eDMA engine to stop normal processing of the active channel immediately (it goes to its error processing states and the transaction to the system bus still has peipeline effect), and the appropriate channel bit in the eDMA error register is asserted.&quot;</td>
</tr>
<tr>
<td>Added the following sentence to &quot;Dynamic Scatter/Gather&quot; section: It allows a DMA channel to use multiple TCDs; this enables a DMA channel to scatter the DMA data to multiple destinations or gather it from multiple sources.</td>
</tr>
<tr>
<td>Feature list, added 32-byte to this item (and removed &quot;burst&quot;): Internal data buffer, used as temporary storage to support 16- and 32-byte transfers</td>
</tr>
<tr>
<td>DMA_TCDn_ATTR[SSIze], added definition for 101b: 32-byte</td>
</tr>
<tr>
<td>Fixed big-endian ordering of DCHPRI and DCHMID registers. Also updated DCHMID to reflect the correct number of channels.</td>
</tr>
<tr>
<td>Changed TCDn_CSR[Reserved], TCDn_BITER_ELINKYES[Reserved], and TCD_CITER_ELINKYES[Reserved] to be WOZ instead of ROZ.</td>
</tr>
<tr>
<td>added image of TCD structure to the beginning of the Memory Map section.</td>
</tr>
<tr>
<td>Updated the CR description: changed text from &quot;where priority level 3 is the highest&quot; to be &quot;where priority level 1 is the highest&quot;, and changed GRPnPRI bit fields to be 1 bit instead of 2.</td>
</tr>
<tr>
<td>Changed reset value of DMA_CR from 0000_0000h to 0000_0400h.</td>
</tr>
<tr>
<td>Updated wording in the register description of DMA_TCD_NBYTES_MLNO, DMA_TCD_NBYTES_MLOFFNO, and DMA_TCD_NBYTES_MLOFFYES for better understanding.</td>
</tr>
<tr>
<td>DMA_TCD_SLAST register, added the following note to the bit field description: &quot;This register uses two's complement notation; the overflow bit is discarded.&quot;</td>
</tr>
<tr>
<td>DMA_TCDn_DLASTSGA[DLASTSGA]: added bullet about 2's complement.</td>
</tr>
<tr>
<td>Changed line above &quot;eDMA peak transfer rates&quot; table to be: &quot;This table compares peak transfer rates based n different possible system speeds. Specific chips/devices may not support all system speeds listed.&quot;</td>
</tr>
</tbody>
</table>
**Revision history**

- **HRS register:**
  - Changed access to Read-Only.

- **CR register:**
  - Reserved bit LSB: Changed access Read/Write Reserved.

- **HSR register:**
  - Bit MSB-4:
    - Changed access value from Read-Only One to Read-Only Zero.

- **Changed topic title from "Error reporting and handling" to "Fault reporting and handling".**

- **Editorial changes.**
  - Changed the chapter title to "Enhanced Direct Memory Access".
  - Changed the title of eDMA system block diagram (was "Block diagram") and revised its content to reflect the entire eDMA system.
  - In Features, changed "Support to cancel transfers via software" to "Support to cancel transfers via software error detection and error correction."

- **Changed description for value b101 of TCD_ATTR[SSIZE] to "32-byte burst (4 beats of 64 bits)".**

- **Made several editorial corrections and improvements.**

- **Removed "(4 beats of 64 bits)" from TCDn_ATTR[SSIZE] bit field description for b101 value.**

- **Fault reporting and handling:** Added note re. cancel transfer request. Added note re. channel priority errors.

- **Block parts:** Changed "16 bytes of register storage" to "a data buffer" in Data path description.

- **Added note to DMA_CR[CLM] description re. restriction on use of continuous link mode.**

- **In section "Peak transfer rates", added a note stating "All architectures will not meet the assumptions listed above. See the SRAM configuration section for more information."**

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**A.1.23  EWM changes**

- Added CTRL[INTEN] bit.
- Added 'EWM Interrupt' section.

**A.1.24  WDOG changes**

Updated the information about LLS for power down mode in Low Power Modes of operation section

**A.1.25  MCG changes**

- Updated MCG block diagrams for MCGFFCLK and MCGDDRCLK2X.
- Updated C1[CLKS] encoding and also updated C10 reset value.

- Updated C8[CME1] field description.
  - In section "External Reference Clock", added text "All clock monitors must be disabled before VLPR or VLPW power modes are entered."

- For the IRCST field in the MCG Status Register, changed references to the fast clock from "fast clock (2 MHz IRC)" to "fast clock (4 MHz IRC)".

- Updated the bitfield access of ATMF and LOCS0 in the MCG_SC register
### A.1.26 OSC changes
- No substantial content changes

### A.1.27 RTC Oscillator changes
- No substantial content changes

### A.1.28 LMEM changes
- Added "Special considerations when using the cache with low power modes" section.
- Deleted the section, "Special considerations when using the cache with low power modes."

### A.1.29 FMC changes
- No substantial content changes

### A.1.30 FTFE changes
- Correct Flash Configuration Field Offset Address for VFYKEY command input

### A.1.31 EzPort changes
In "Command descriptions" section, added timing diagrams for each command sequence.

### A.1.32 NFC changes
- Editorial changes.
- **Row address (NFC_RAR)**: Swapped the positions of the RBN and CSn fields.
- **NAND Flash Boot**: Deleted "See the Chip Configuration details for what the processor does after this" from step 4.
A.1.33 FlexBus changes

- Minor editorial changes and reorganization of sections:
  - Many sections were divided into multiple subsections.
  - Changed "Overview" section name to "Definition.”
  - Moved data from signal description subsections into the signal description table.
  - Removed "Chip Select Operation" section.
  - Moved "Modes of operation” section to “Functional description” section.
  - Combined “Bus Cycle execution” and data transfer cycle states sections into the “Data transfer states” section.

For little endian devices: Revised figure “Connections for External Memory Port Sizes (CSCRn[BLs] = 1)”: Added byte enable lines for each port size (included adding overbars to BE signals).

- Changed the Note in the CSMR[V] bitfield description to say: "At reset, FB_CS0 will fire for any access to the FlexBus memory region. CSMR0[V] must be set as part of the chip select initialization sequence to allow other chip selects to function as programmed.”

- Combined CSCR[PS] 10b and 11b options into 1X since they had the same bit field definition.

- Added FB_TBST trace to 6 burst timing diagrams
- Improved 2 diagrams ["Connections for external memory port sizes (CSCRn[BLs] = 0)", "Connections for external memory port sizes (CSCRn[BLs] = 1)"]

In all 12 Read timing diagrams, updated FB_BE/BWEn signal to show BEM=1 and BEM=0.

A.1.34 CRC changes

- Changed the name of the CRC_CRC register to the CRC_Data register

- Editorial change in the section "CRC initialization/reinitialization.”

A.1.35 MMCAU changes

- No substantial content changes

A.1.36 RNGA chapter changes

- Updated description of RNGA Control Register, RNG_CR[HA] field, RNG_SR[OREG_LVL] field, RNG_SR[ERRI] field, RNG Output Register, RNG_ER[EXT_ENT] field
- Updated RNGA block diagram
- Updated description of RNGA Control Block
- Updated description of Initialization/application information.

In "Overview," updated bulleted item from "Mouse and keyboard motions, or equivalent if being used on a cell phone or PDA" to "Real-time system inputs that can be characterized as 'random'."
A.1.37 DryIce changes

- No substantial content changes

A.1.38 ADC changes

- In ADC Signal Descriptions section: Added note to refer to chip configuration for inputs supported.
- Updated the bit field description of CFG1[ADICLK] to Bus Clock/2
- Editorial changes
  - Changed bitfield access of ADC_SC3[CALF] to w1c (write 1 to clear).

A.1.39 CMP changes

- Updated CMPx_CR1[PMODE] field description.
- Updated SE value in 'Sampled, Filtered (# 4B): Sampling point internally derived' diagram.
- Added Reserved field (was previously PSTM, Pass Through Mode Enable) in CMP_MUXCR register

A.1.40 DAC changes

- Replace introduction topic content.

A.1.41 VREF changes

- No substantial content changes

A.1.42 PDB changes

- In the memory map, changed Channel n Status Register access to R/W.
- Updated the DAC trigger module in PDB Block Diagram
- Added the following sentence to section "PDB pre-trigger and trigger outputs":
  "When the ADC receives the rising edge of the trigger, the ADC will start conversion as the precondition determined by pre-triggers."
### A.1.43 FTM changes

- Corrected the figure "Example of the Prescaler Counter".
- For section "Filter for Input Capture mode", removed the phrase "5-bit" in references to the counter and clarified when the input signal is validated.

### A.1.44 PIT module changes

- In MCR, standardized access type for Reserved fields to read-only.
- Added to registers header: "Timer Channel n" table and all content.
- Deleted "Timer Channel n / RTI Channel" table because the same information is in the more comprehensive "PIT memory map" table.
- RTI_TCRTL register:
  - Deleted CHN bit.
  - Changed description of the TIE bit to show RTI_TFLG[TIF].
  - Changed bit map of TEN bit to show "RTI Timer".
- Introduction section. For SOCs that use PIT pulses to trigger DMA, added DMA text to sentence "The PIT module is an array of timers that can be used to raise interrupts and trigger DMA channels."
- Features section. For SOCs that use PIT pulses to trigger DMA, added DMA text to bullet "Ability of timers to generate DMA trigger pulses".
- MCR[MDIS or Reserved] bit.
  - Changed Reserved access to R/W.
- TFLG, TCTRL, CVAL, and LDVAL registers:
  - For implementations that use 6 channels, 6 channels can now be shown.
  - Removed "-RTI" from chapter title
- PIT_TCTRLn[CHN] description
  - Changed sentence to read "Timer 0 cannot be chained."
- For the third bullet updated 1 hour to 1 minute in Example configuration for chained timers.
- Added information about register access level at the end of each register description

### A.1.45 LPTMR changes

Updated the following sentence: "If CSR[TFC] is cleared, then the CNR is also reset whenever CSR[TCF] is set."

### A.1.46 CMT changes

- No substantial content changes
A.1.47  RTC changes

- Swapped the TDTL and TDTH fields in the RTC_TTR register.

A.1.48  ENET module changes

- Added Reference clock subsection in Functional description section.
- Added STAT_SECTION_EMPTY field to RSEM register in Memory Map section.
- Added AVB features included new regs RDAR1/2, TDAR1/2, RCMR1, Rate limiting traffic shaping support topic.
- Added DMAnCFG regs
- Removed ‘u’ reset values from register section.
- Clarified descriptions for TTL and header checksum in ipv4 checksum datagram format topic
- Registers topic: Replaced ETHER_EN with ETHEREN for consistency. Added bit values and note to TFRW register.
- Added RGMII_REF_CLK to external signals topic.
- Added 1G bandwidth limitation to features topic.
- Added QOS_SCHEME register topic. Corrected value in example 2 in DMACFG[IDLE_SLOPE] register description. Added RX_FLUSHn fields to EIR reg. Added missing fields to EIMR to match EIR. Added bitfieldaccess element to eim[rxfush_0]. Changed EIMR[8:13] to RW with note added to description. Changed EIMR[24:31] from W1C to RW. Added better descriptions to RXFLUSH fields in EIR.
- Added round-robin mux and QoS select mux to Transmit arbitration scheme figure.
- Added note to clarify restriction on legacy description use.
- Removed EIR[RXFLUSH_0] and EIRM[RXFLUSH_0] fields and QOS_SCHEME register.
- Added note to ENET_EIR register description about use in enhanced mode.
- In Enhanced transmit buffer descriptor (TxBD) table, for offset + 8 entry in , changed "Generate interrupt" to "Generate interrupt flags".
- In External signal description, replaced ‘—’ with "1588_TMRn" in 1588_TMRn row and RGMII column.
- Tables for enhanced and legacy buffer descriptors have been modified to show correct byte order for little endian devices.
- Improved register descriptions in Receive FIFO and Transmit FIFO sections.
- Added Statistic Event Counter registers, 0X0200-0x02E0, to Memory map/register definition section and removed Statistic event counters section.
- Corrected 1588EN to EN1588 in IEEE 1588 functions.
- Updated descriptions for RSEM, RSFL, RSEM, RAEM, TSEM, TAEM, and TAFL registers.
- Corrected first note in Legacy buffer descriptors.
- Removed redundant content from RSFL[RX_SECTION_FULL] description.
- Corrected widths of Reserved and Flags fields in TCP header fields table.
- Added note to ECR[ETHEREN] description.
- In Ethernet MAC features, changed operating speeds from 25 MHz to 2.5/25 MHz and spelled out AVB.
- In figure "MAC frame format overview" and "VLAN-tagged MAC frame format overview," corrected position of Frame Length brace.
- Changed R/W access of some of the reserved fields in: TDAR, ATCR, .
- Removed note from ENET_ATCR register description. Added note and "This field automatically clears to 0 after the command completes." to ATCR[CAPTURE] and ATCR[RESTART] descriptions.
- Changed "this register to 0x0000_0004" to "MII_SPEED to 0x4" in MSCR register description.
- Added Warning to Adjustable Timer Control Register (ENET_ATCR) register CAPTURE and RESTART field descriptions.
**Revision history**

- In TFWR: Bit field values now show only valid values. Removed note that referred reader to chip-specific information.
- In Sleep mode: Replaced ambiguous use of "core" with "MAC".
- In Adjustable timer module: Removed sentence referring to time-stamp clock source.
- Removed Receive Flushing topic; does not apply to single-queue ENET.
- Removed reference to DMAnCFG register in Legacy buffer descriptors.
- Added value descriptions to ENET_MIBC register fields.
- Added Input Capture and Output Compare.
- Corrected field width of ENET_MRBn[R_BUF_SIZE].
- Corrected access type of ENET_ATCR[Reserved] to WOO and added note to its description that it must be written with one.
- In MDIO clause 22 frame format changed "IEEE803.2" to "IEEE 802.3".
- Made improvements to Block diagram figure.
- Memory map/register definition: Added statement regarding allowed accesses width to registers and made editorial changes.
- Transmit Inter-Packet Gap (ENET_TIPG): Corrected description of IPG field.
- Inter-packet gap (IPG): Corrected text regarding IPG values.
- Removed sentences regarding register reset/initilization in Physical Address Lower Register (ENET_PALR) and Physical Address Upper Register (ENET_PAUR).
- Improved descriptions of statistics register fields.
- Removed Receive Parser block from Figure 47-109.
- Updated descriptions for Frames Received OK Statistic Register (ENET_IEEE_R_FRAME_OK) and Octet Count for Frames Received without Error Statistic Register (ENET_IEEE_R_OCTETS_OK).
- Changed occurrences of DMA to uDMA, where appropriate, for clarity.
- Added note to ENET_IEEE_T_FRAME_OK[COUNT] description.
- Added note to ENET_IEEE_R_OCTETS_OK[COUNT] description.
- Added receive and transmit FIFO depths to FIFO thresholds.
- Added description of uDMA to Overview. Replaced "DMA" with "uDMA" in Transmit FIFO Watermark Register (ENET_TFWR) and Soft reset.
- Added descriptions for RMON_T_DROP, IEEE_T_DROP, IEEE_T_SQE, and RMON_R_RESVD_0 registers.
- Added new IEEE 802.3 Clause 45 content:
  - Added this feature to Ethernet MAC features.
  - Modified ENET_MMFR field descriptions.
  - Changed content and title of MDIO clause 22 frame format.
  - Added MDIO clause 45 frame format.
- Changed full register names of RMON_T_DROP, IEEE_T_DROP, and RMON_R_RESVD_0 to "Reserved Statistic Register".
- In ENET_TCSRn[TMODE] description changed "1100 Reserved" to "110X Reserved".
- Changed Reserved Statistic Register (ENET_RMON_T_DROP) and IEEE_T_DROP Reserved Statistic Register (ENET_IEEE_T_DROP) to have single, 32-bit, Reserved fields.

### A.1.49 USB full speed OTG controller changes

- In "Host mode operation examples", corrected the "Data toggle" in the first bullet of Step 11 for the "To complete a control transaction to a connected device" procedure.
- In the "Buffer descriptor fields" table within the "Buffer Descriptors (BDs)" section, added information to the description of the BDT_STALL bit.
- In "OTG and Host mode operation" section, changed the following sentence, "Support is provided for ISO transfers, but the number of ISO streams that can be practically supported is affected by the interrupt latency of the processor servicing the token during interrupts from the SIE," to "Support is provided for ISO transfers, but the number of ISO streams that can be practically supported is affected by the interrupt latency of the processor servicing the Token Done interrupts from the SIE."
• Under USB_ENDPT register description, added table, "Endpoint enable and direction control," to clarify functioning of EPCTLDIS, EPRXEN, and EPTXEN bits.
• Changed ADDINFO[IRQNUM] description to "Reserved; should always have the value zero."
• Added new topic under "Functional description": "On-chip transceiver required external components."
• Corrected range of USB SRAM for use in Keep Alive mode from 256 bytes to 512 bytes.

A.1.50 USBDCD changes

• No substantial content changes

A.1.51 USB VREG changes

• No substantial content changes
• Removed the number specified for the STANDBY regulator output load current.
• Corrected the figure "Ideal Relation Between the Regulator Output and Input Power Supply".

A.1.52 USB high speed OTG controller changes

• No substantial content changes

A.1.53 FlexCAN module changes

• Added a new section, "Clock domain relations"
• In table in description of CTRL2[RFFN] field: Added footnote to heading of second-to-last column
• In FlexCAN module features section, added bullet "Compliant with the ISO 11898-1 standard".
• Updated CAN engine clocking scheme figure of Protocol timing section.
• Updated table title from "CAN standard compliant bit time segment settings" to "Bosch CAN 2.0B standard compliant bit time segment settings".
• In Module Configuration Register (CAN_MCR)
  • Changed reserved field access from read/write to read-only and always read as 0:
    • Reserved
    • Reserved
• In description of in added "error" to first sentence: "Disables completely the memory error detection and correction mechanism."
• In description of in added: "The two least significant bits of this field always read as 0."
• Previous errata e7724 integrated into the RM: Changed access for and from read/write to read-only
• Interrupts
  • Edited text and standardized format of references to registers
A.1.54 SPI module changes

- In 'Transmit FIFO Fill Interrupt or DMA Request' section, added note on using TFFF flag.
- Added links to corresponding functional description in the Delay fields in CTAR register.
- Renamed DSICR to DSICR0.
- Updated EOQ interrupt request description.
- Added SPITCF and DSITCF interrupt request descriptions and updated corresponding bit fields in SR register.
- Updated DIS_TXF and DIS_RXF bit field descriptions in MCR register.
- Updated 'Sample MSC downstream transmission using ITSB mode' diagram.
- Updated Features section about 8 extended CTAR registers; programmable serial frame size up to 64 bits; DMA Support for CMDFFF and DDIF; Interrupt Support for CMDFFF, CMDTCF, TFIWF.
- Added XSPI field to MCR register.
- Updated CTAR[FMSZ] field description. Added FMSZ6 field to CTAR_Slave.
- DSPI_SR Register: Updated TFFF description. Added BSYF, CMDFFF, CMDTCF and TFIWF fields.
- DSPI_RSER register: Updated fields CMDFFF_RE, CMDTCF_RE, TFIWF_RE, CMDFFF_DIRS and DDIF_DIRS.
- Updated PUSHR_Master, PUSHR_Slave and TXFRn Register Descriptions.
- Added SDR1, ASDR1, COMPR1, DDR1, SSR1, PISR4-7, DIMR1, DPRIR1, CTARE, SREX Registers.
- Updated DSPI Memory Map.
- Updated PUSHR[CONT] bit description.
- Updated Stop Mode, Module Disable Mode descriptions under Power Saving Features.
- Updated Following figures : Block Diagram, DSI Serialization, DSI Deserialization, TSB Downstream Frames, TSB Data Frame Format for MSC Dual Receiver Operation, TSB Data Frame Format for MSC Dual Receiver Operation.
- Updated "Deserial Serial Interface (DSI) configuration" functional description to mention about the new DSIS64 Mode and its usage.
- Added a Note to "Multiple Transfer Operation (MTO)".
- Updated "Combined Serial Interface (CSI) configuration" to include effects of the new XSPI and DSIS64 modes.
- Added "Command FIFO Fill Interrupt or DMA Request", "Transmit FIFO Invalid Write Interrupt Request", Command Transfer Complete Interrupt Request", "Deserialized Data Match DMA Request" to "Interrupts/DMA Requests".
- Added "Address Calculation for first-in-entry and last-in-entry in the CMD FIFO.
- Modified Async Clocking Scheme and CMDTCF Feature Descriptions
- Updated descriptions of the following bitfields: MCR[MDIS], CTAR[FMSZ], SR[CMDTCF], SR[TFFF], PUSHR[PE_MASC], PUSHR[PP_MCSC]
- Updated register description for PUSHR_Slave and RXFRx
- Changed CTAR_SLAVE[FMSZ6] to CTAR_SLAVE[FMSZ5]
- Updated mention of system clock to protocol clock at all places appropriate
- Revised the field description of DSPI_CTAxn_SLAVE[FMSZ]
- In the Combined Serial Interface (CSI) Configuration, revised the note
- In the Timed Serial Bus (TSB) section, revised the figure
- Editorial updates
- Notes added in DSPI_CTAxn_SLAVE[CPOL] bit description
- Notes added in DSPI_CTAxn[CPOL] bit description
- In DSPI_MCR changed Reserved bit from read-only to read/write
- Included two topics Modified SPI Transfer Format (MTFE = 1, CPHA = 0) and Modified SPI Transfer Format (MTFE = 1, CPHA = 1).
- Reduced bit width of SPI_CTAxn_SLAVE [FMSZ] from 5 to 4.
- In RSER register, added note "Always write the reset value to this field." to Reserved bits.
- In PUSHR register, added note "Always write the reset value to this field." to Reserved bits.
- In Memory Map/Register Definition section, added "RXFRn' word.
- In Module Configuration Register (SPI_MCR) register, added "Refer to the chip-specific..." sentence in PCSIS bit.
- In PUSH TX FIFO Register In Master Mode (SPI_PUSHR) register, added "Refer to the chip-specific..." sentence in PCS bit.
A.1.55  I2C changes

- In description of F[ICR], added new final sentence and table containing examples of MULT and ICR field settings.
- In description of C2[SBRC], added sentence describing an example of a "very fast" I2C mode.
- In "Clock stretching" section, added new final sentence to clarify the effect of clock stretching.
- Clarified that the reserved bit 7 of the Programmable Input Glitch Filter register can be written but that writing it has no effect.
- In the "SCL high timeout" section, removed references to detection of a HIGH timeout after a STOP condition appears on the bus.
- Reorganized the "Address matching wakeup" section, and added in the final note the sentence "The main purpose is not communication."
- Reorganized the "Address matching" section, and clarified the sources of a 7-bit and 10-bit address, including the involvement of ADEXT and AD[10:8] in Control Register 2.
- In "I2C divider and hold values" section: Added note preceding the table, and shaded table cells containing ICR values of 00h to 0Fh
- In Inter-Integrated Circuit (I2C) chapter, added new section "I2C module address matching to wake the device from stop mode"
- Updated and clarified the flowchart figure "Typical I2C SMBus interrupt routine".
- Used the wording "I2C module clock" instead of "bus clock" in the register definitions and the "Programmable input glitch filter" section.
- Updated in the statements of register fields S[IAAS], S[RAM], C2[RMEN], RA[RAD] and the section "Address matching", to clarify that the Range Address register is only meaningful when the C2[RMEN] bit is set.
- Added notes in the sections "Address matching wake-up".
- No substantial content changes.
- Added the handling of START/STOP interrupt in the ISR flowchart Typical I2C interrupt routine.

A.1.56  UART changes

- Updated S2[MSBF], S2[RXINV], C3[TXINV] and C7816[INIT] register bit field descriptions to mention that Initial Character Detect feature can only be used in TTYPE = 0 mode.
- Updated Initial Characters Section in 7816 Functional Description.
- Updated Protocol T=0 Section in 7816 Functional Description.
- Updated IE[ISDIE] register bit field description.
- Added bits CFIFO[RXOFE] and SFIFO[RXOF] which were missing. These are legacy register bits.
- Updated the section "RXEDGIF description"
- Added reference to the "Hardware Flow Control" section, in the field description for UART_MODEM[RXRTSE]
## A.1.57 SDHC changes

- No substantial content changes

## A.1.58 I2S/SAI changes

- For both TCSR[TE] and RCSR[RE] fields, clarified the description for field value of 1.
- In "Introduction" section: Clarified support for TDM mode.
- Revised descriptions of BCS and BCI fields in TCR2.
- Clarified descriptions of TCE field in TCR3 and RCE field in RCR3.
- In "FIFO pointers" section: Clarified 8-bit and 16-bit accesses to the FIFOs.
- In "Frame sync configuration" section: Clarified various configuration options.
- Added "Integrated Interchip Sound (I2S)" to the main title to clarify the module's support for this standard.
- Removed references to "received" from description of TCR4[MF]
- Removed references to "transmitted" from description of RCR4[MF]
- In the descriptions of TCR2[MSEL] and RCR2[MSEL], added this Note: "Depending on the device, some Master Clock options might not be available. See the chip configuration details for the availability and chip-specific meaning of each option."
- In the "Bit clock" section of the "Clocking" section, added a new final paragraph: "If the SAI transmitter or receiver is using an externally generated bit clock in asynchronous mode and that bit clock is generated by an SAI that is disabled in stop mode, then the transmitter or receiver should be disabled by software before entering stop mode. This issue does not apply when the transmitter or receiver is in a synchronous mode because all synchronous SAIs are enabled and disabled simultaneously."

## A.1.59 GPIO changes

- No substantial content changes

## A.1.60 TSI changes

- No substantial content changes

## A.1.61 JTAGC module changes

- Removed arrow from TDI to TAP instruction register in block diagram figure
- Added EZPORT row to 4-bit JTAG instructions table with Code 1101
- In the General JTAG instructions table, updated the Instruction summary cells to emphasize which instructions assert functional reset.