

## 1 背景

扩频是一种将传输信号的频谱转换为比其原始带宽更宽的通信技术，并广泛应用于无线通信领域。

本文旨在介绍有关扩频的基本理论，以及如何为 RT 功能启用此功能以增强 EMI 性能。

## 2 扩频介绍

### • 窄带信号

窄带信号的信号强度集中在 [图 1](#) 中。

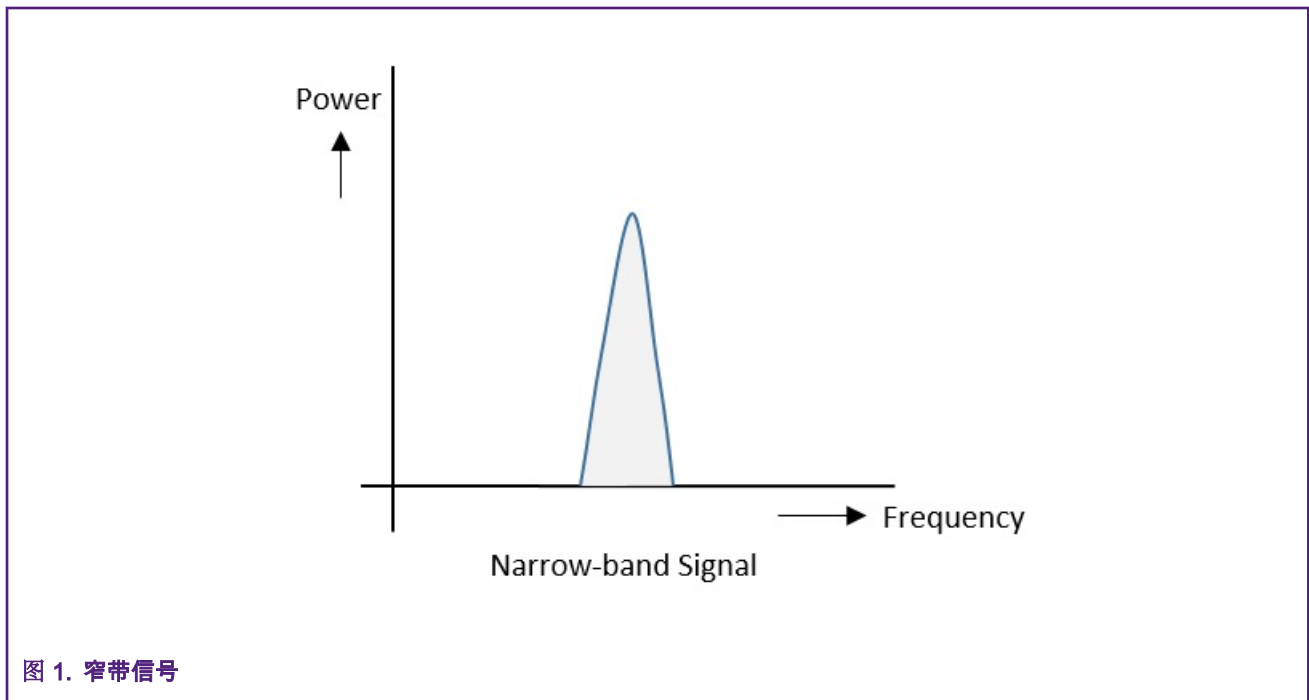


图 1. 窄带信号

它有如下一些特性：

- 信号频带占用的频率范围很窄。
- 功率密度高。
- 能量扩散低且集中。

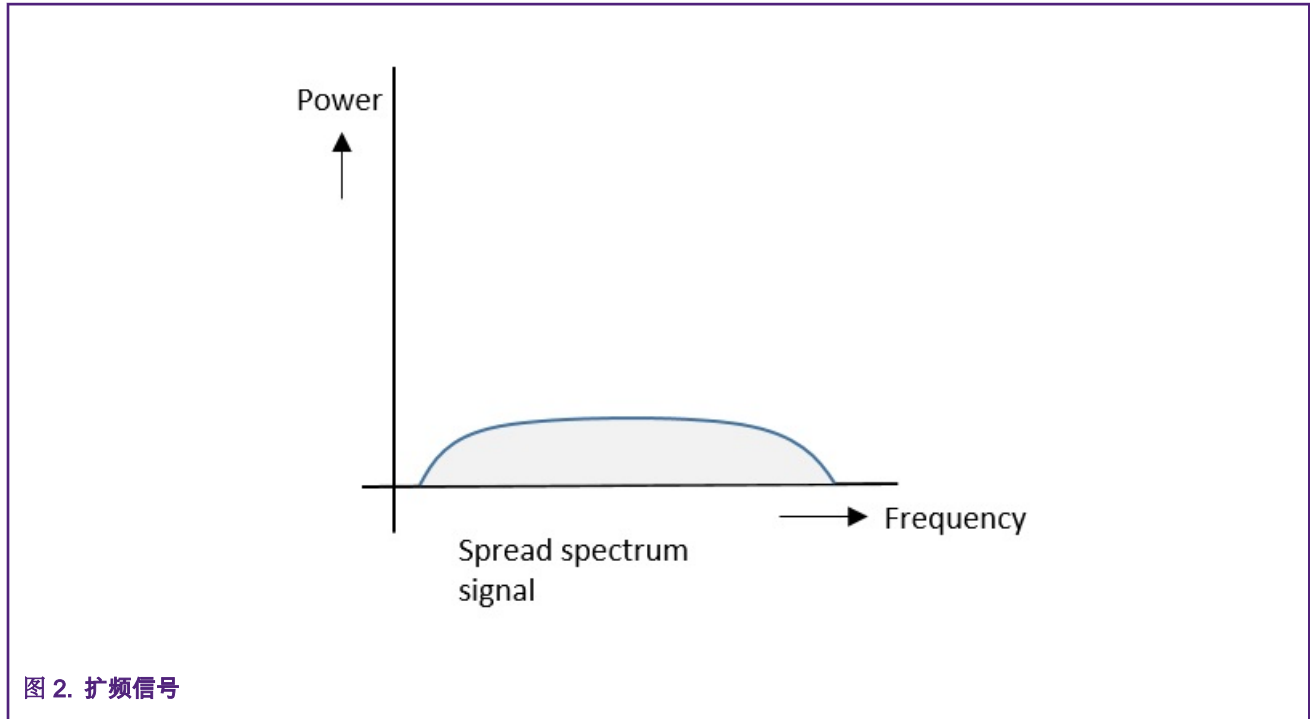
这种信号很容易产生干扰。

### • 扩频信号

扩频信号具有 [图 2](#) 所示的信号强度分布。

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它有如下一些特性：

- 信号频带占据很宽的频率范围。
- 功率密度很低。
- 能量分布很广。

从上面的描述中可以看到扩频信号具有很高的抗干扰能力。

### 3 扩频配置

对于 RT 系列，SYS\_PLL2，AUDIO\_PLL 和 VIDEO\_PLL 支持扩频（向下扩频）。要启用扩频功能，请使用图 3 扩频软件配置来配置 SDK 中的寄存器。

```

/*
0x40c84260 is used to configure the value of
STOP(bit[31:16]), and STEP(bit[14:0]). Bit 8
is the enable bit.
The Frequency change is:
    Frequency change = STOP/B *24MHz

The Step value is :
    The max frequency change for each time = STEP/B * 24MHz

0x40c842a0 is used to configure the value of B.

So that, the following configure is :
STOP = 0x480;
B = 0x960;
STEP = 0x6;
Frequency change = 12MHz
The max frequency change for each time = 60KHz

STOP = 0x240;
B = 0x960;
STEP = 0x6;
Frequency change = 6MHz

The max frequency change for each time = 60KHz
*/
*(uint32_t *) (0x40c84260) = 0x04808006; //12MHz
/*(uint32_t *) (0x40c84260) = 0x02408006; //6MHz
*(uint32_t *) (0x40c842a0) = 0x00000960;

typedef struct _clock_sys_pll_config
{
    uint8_t loopDivider; /*< PLL loop divider. Intended to be 1 (528M).
        0 - Fout=Freq*20;
        1 - Fout=Freq*22 */
    uint32_t mfn; /*< 30 bit mfn of fractional loop divider.*/
    uint32_t mfi; /*< 30 bit of fractional loop divider */
    uint16_t ss_stop; /*< Stop value to get frequency change. */
    uint8_t ss_enable; /*< Enable spread spectrum modulation */
    uint16_t ss_step; /*< Step value to get frequency change step. */
} clock_sys_pll_config_t;

```

图 3. 扩频软件配置

### 4 扩频辐射比较

使用 EVK-MIMRT1170 平台进行此测试。使用非接触式探头和频谱分析仪，在不同配置下对扩频测试辐射值。根据测试结果，在这种情况下建议使用 6 MHz 和 12 MHz 的停止值，以提高 EMI 性能。

Spread Spectrum(HZ)	0.75M	1.5M	3M	6M	12M	24M
Test Result(dBm)	-46.2	-46.56	-49.85	-52.31	-53.35	-54.3



**6M&12MHZ configure is recommended**

图 4. 不同扩频配置下的测试结果



图 5. 3 MHz 配置下的频谱

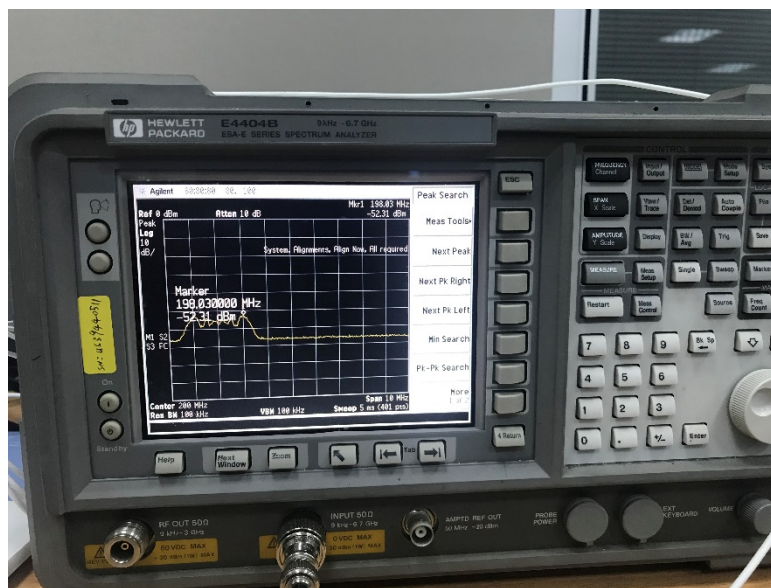


图 6. 6 MHz 配置下的频谱

## 5 频谱扩展下的可靠性测试

SDRAM 可靠性在 RT1170EVK 平台上启用的频谱扩展下进行了测试。有关测试模式，请参见 [表 1](#) 可靠性测试的基本配置。

表 1. 测试的基本配置

	Module	Freq
Core	Cortex-M7	996 MHz
AXI to SEMC	32 bit	240 MHz
SEMC	32 bit	198 MHz
SDRAM chip	w9825g6kh	256 Mb/up to 200 MHz
L1 Dcache	Total 32 KB/One-line 32 B	—
Code	Text region in ITCM Data region in DTCM CStack region in DTCM	—

从测试结果来看，6 M 和 12 M 都可以通过全温度测试下的压力测试，这意味着为 SDRAM 时钟启用频谱扩展功能非常可靠。

```
DRAM test setting:
    Base Address: 0x80000000;
    Test Size: 67108864 Bytes;
    Test Loop: 1;
    DRAM Freq: 198010624;
    Fail Stop: 0;
    Enable Cache: 0;
    Core clock: 996056064;
    AHB clock: 120006784;
    SEMC clock: 198010624;

memtester version 4.3.0 (32-bit)
Copyright (C) 2001-2012 Charles Cazabon.
Licensed under the GNU General Public License version 2 (only).

want 64MB (67108864 bytes)
Loop 1/1:
    Stuck Address: ok
    Random Value: ok
    Compare XOR: ok
    Compare SUB: ok
    Compare MUL: ok
    Compare DIV: ok
    Compare OR: ok
    Compare AND: ok
    Sequential Increment: ok
    Solid Bits: ok
    Block Sequential: ok
    Checkerboard: ok
    Bit Spread: ok
    Bit Flip: ok
    Walking Ones: ok
    Walking Zeroes: ok
    8-bit Writes: ok
    16-bit Writes: ok

Done and Passed!
exit_code 0x0
```

图 7. 可靠性测试结果

## 6 频谱扩展下的 SEMC 时序配置

还请注意频谱扩展下的 SEMC 时序配置，请检查以下几点。

- 为了提高 SDRAM 的稳定性，可以基于工作时钟速度以更大的余量设置 SEMC 时序配置。
- 参考图 8 所示的 SDRAM 芯片时序要求，可以在 SEMC 寄存器 SDRAMCR1 和 SDRAMCR2 中将 tRC，tRAS，tRP，tRCD，tRW，tRRD 的最小值设置一个或两个以上的周期。例如，标准的 tRC 是 6 个周期（在 166 MHz 时至少为 60 ns），我们可以在频谱扩展模式下将其设置为 7（或 8）个周期。
- 对于 tREF（刷新周期时间），应将其设置为小于最大刷新周期（64 ms）。这可以在 SEMC 寄存器 SDRAMCR3 中实现。在 NXP SDK 中，tREF 设置为小于最大刷新周期的一半。
- 有关 SEMC 时序的详细配置，请参考 NXP SDK。

tRC	Command Period (REF to REF / ACT to ACT)	60	—	60	—	ns
tRAS	Command Period (ACT to PRE)	42	100K	37	100K	ns
tRP	Command Period (PRE to ACT)	18	—	15	—	ns
tRCD	Active Command To Read / Write Command Delay Time	18	—	15	—	ns
tRRD	Command Period (ACT [0] to ACT[1])	12	—	14	—	ns
tDPL	Input Data To Precharge Command Delay time	12	—	14	—	ns
tDAL	Input Data To Active / Refresh Command Delay time (During Auto-Precharge)	30	—	30	—	ns
tMRD	Mode Register Program Time	12	—	14	—	ns
tDDE	Power Down Exit Setup Time	6	—	7	—	ns
tXSR	Exit Self-Refresh to Active Time <sup>(4)</sup>	66	—	70	—	ns
t <sub>t</sub>	Transition Time	0.3	1.2	0.3	1.2	ns
tREF	Refresh Cycle Time (8192)					
	T <sub>A</sub> ≤ 70°C Com., Ind., A1, A2	—	64	—	64	ms
	T <sub>A</sub> ≤ 85° C Ind., A1, A2	—	64	—	64	ms
	T <sub>A</sub> > 85°C A2	—	32	—	32	ms

图 8. SDRAM 设备时序

## 7 扩频下的性能测试

性能测试是在频谱扩展下进行的，请检查以下测试环境和测试结果。可以得出结论，频谱扩展对 SDRAM 读 / 写性能影响很小，对应用程序没有影响。

- 项目配置：s dram\_debug。
- SDRAM MPU 配置: non-shareable/cacheable/wb/disable Dcache。
- 测试环境: Initial, 6 MHz, 12 MHz, 24 MHz。
- 测试结果: 测试几秒钟的 16 KB 和 32 KB 数据写入/读取性能，结果显示读取性能均为 22 MB / s，写入性能如 图 9 所示。

表 2. SDRAM Performance test under spread spectrum

		Initial	6 M	12 M	24 M
Average write	Perf (MB/S)	693	689	685	677
	Reduction percentage	—	-0.6%	-1.2%	-2.3%

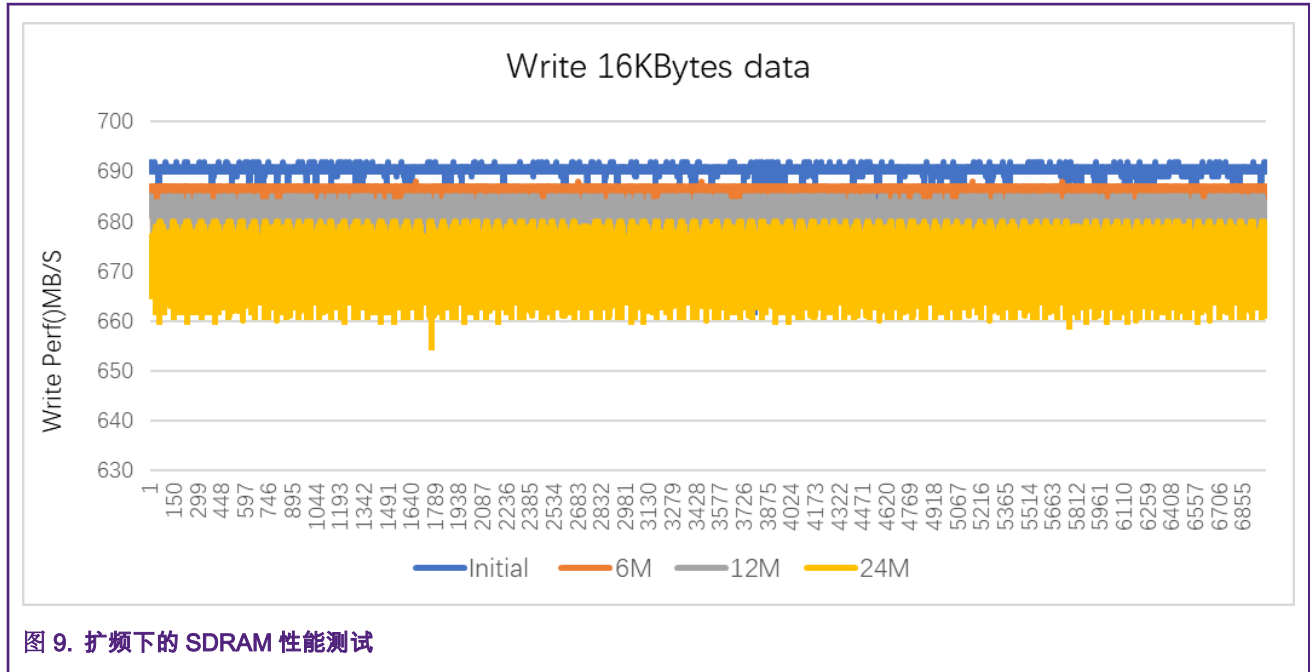


图 9. 扩频下的 SDRAM 性能测试

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