NXP EV-INVERTER

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March 2020

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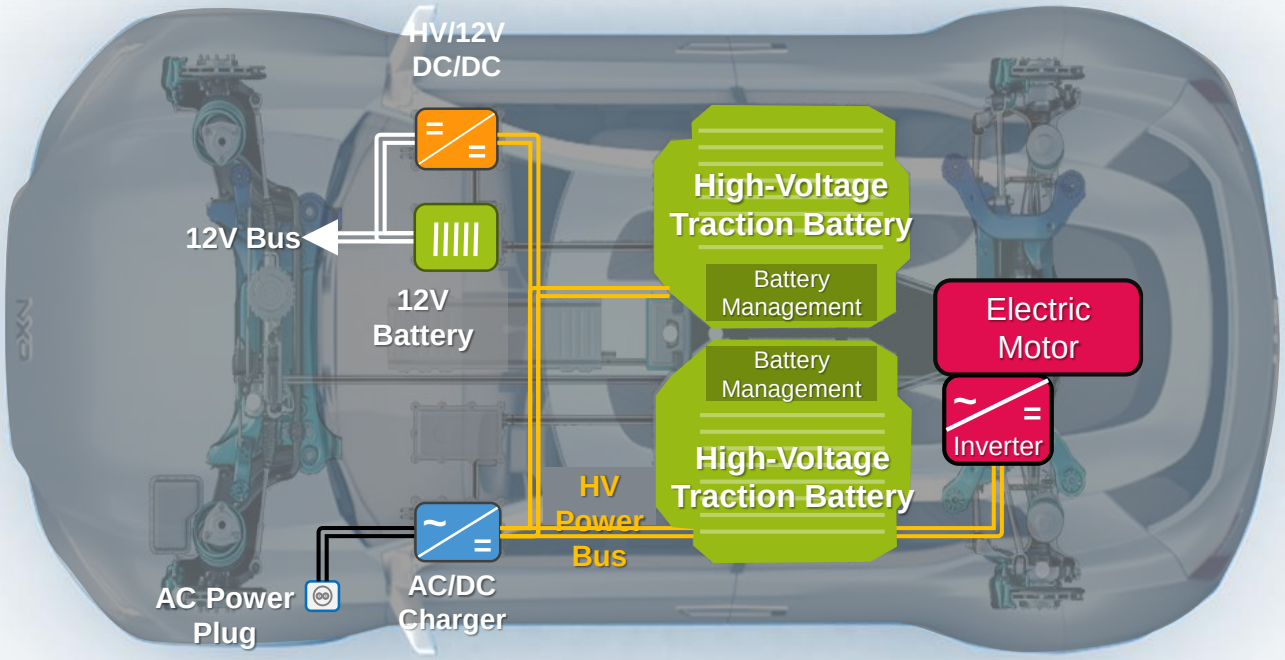
Agenda

- EV-INVERTER Description
- Key Parts Introduction
- IDH Engineering Service
- SW Enablement
- Safety Enablement

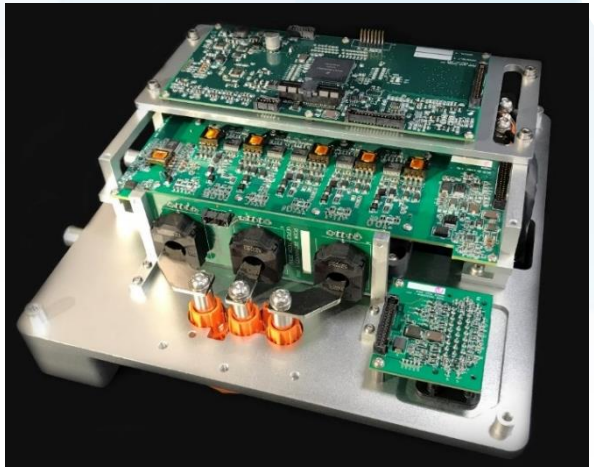
New Applications Driving Electrification Market Growth

NXP Major Components	MCU	SBC	COMM	Driver	AFE
Motor control, inverter, HCU	●	●	●	●	
DC/DC voltage domain converter	●	●	●		
On-board charger AC/DC converter	●	●	●		
Battery management system	●	●	●	●	●
48V eMachine (BSG, ISG, HVAC)	●	●	●		



What is a HV Power Inverter for EV Traction Motor?

Parameter	Value	Units
Operating input voltage Range	250- 420	VDC
Continuous output power	65	kW
Peak output power	110	kW
Nominal Voltage	330	VDC
Nominal Current	200	A, rms
Peak Current	420	A, rms
Control input supply voltage range	8 - 18	VDC
Motor Operating speed	0 - 10,000	RPM
PWM Switching Frequency	3-12	kHz
Control type	Current /Speed/Torque	
Maximum electrical Efficiency	> 97	%
Communication interface	CAN Bus	
Liquid Cooling		liters/min
Inverter mechanical envelope	28 x 28 x 14	cm x cm x cm
Inverter mass	< 10	Kg
Power Devices	Silicon IGBT (800A, 750 V)	1 module



NXP EV-INVERTER Overview

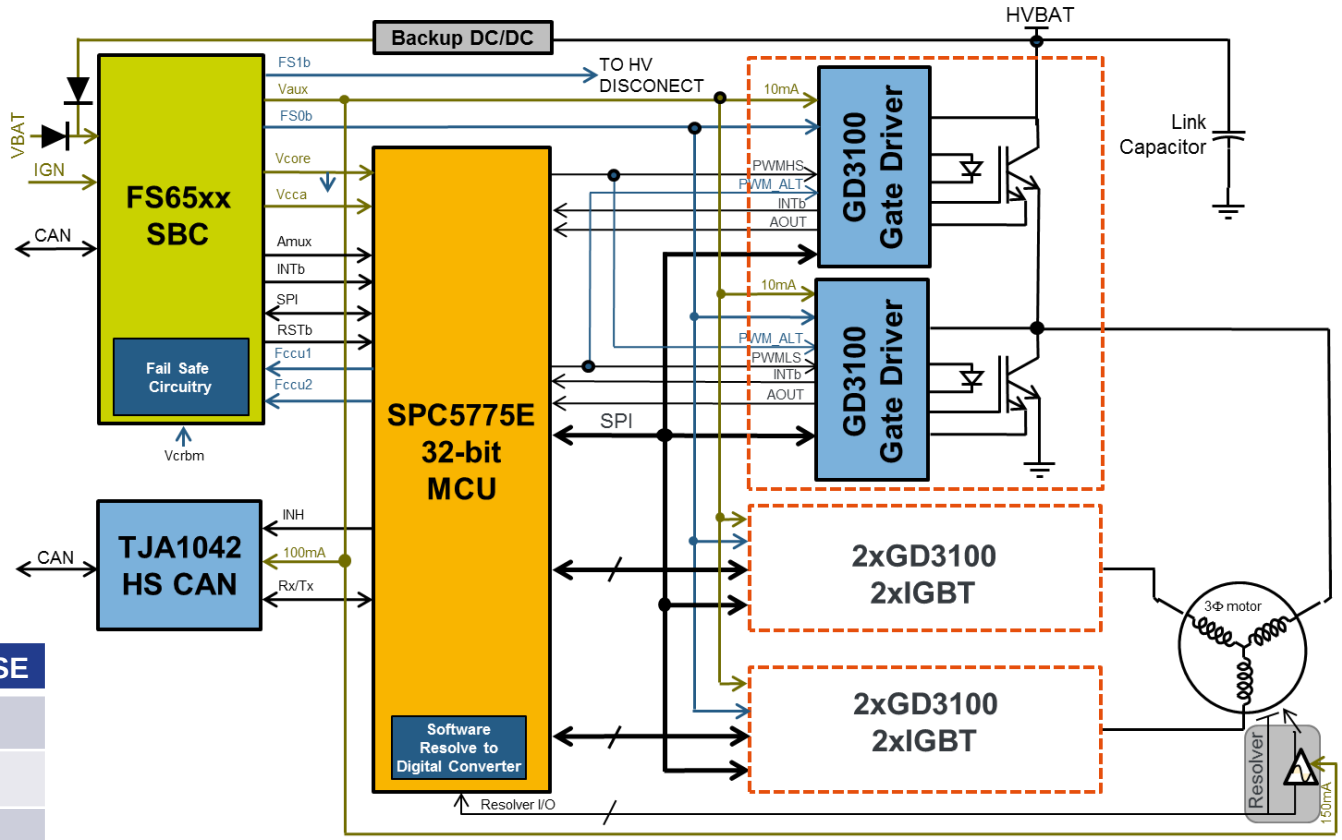
Features

- Efficiently drives 100kW 3 phase motor from 400V
- NXP system solution + Fuji IGBTs
- Functional safety case and enablement SW
- Production-quality platform enables confident, fast customer design

Applications

- EV motor power Inverters
- HV UPS power inverters
- Alternate energy power inverters

PART #	PKG	Footprint	RELEASE
FS65 Safety SBC w/ fail silent	48p LQFP	9 x 9 mm	Yes
MPC5775E 32-bit MCU w/ eTPU	416 MAPBGA	27 x 27 mm	Yes
TJA1042 CAN FD w/ Standby	SO8	4.9 x 6 mm	Yes
GD3100EK Gate Driver (x6)	SOICWB32	10 x 18 mm	Yes
Fuji M653 IGBT 6 in 1 Module	Liquid Cooled	117 x 162 mm	Now



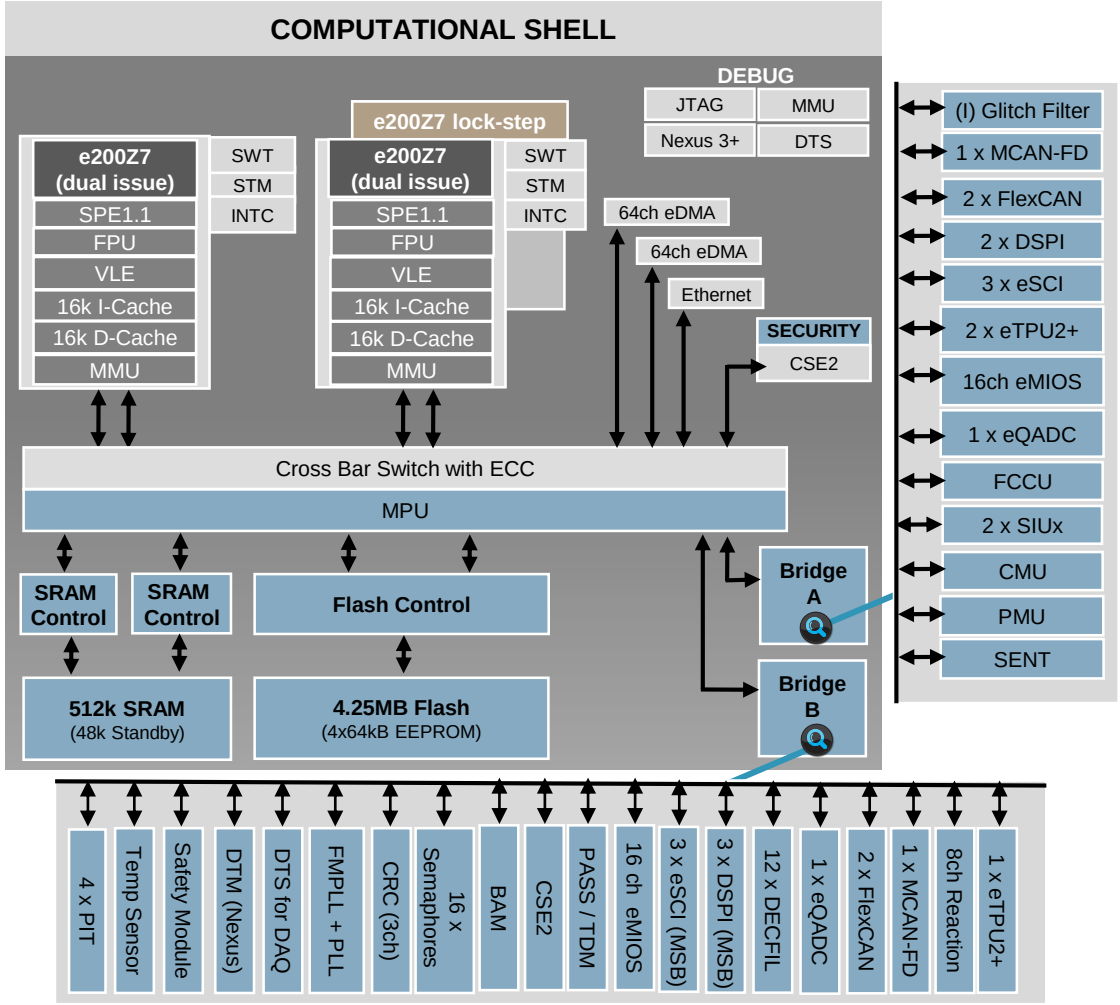
SPC5775E ASIL D MCU

Cores & Memory

- Two independent z7 dual issue computational cores @ 264MHz
  - Cores include VLE, SPE1.1, FPU , MMU
  - 16kB i-cache & 16kB data-cache w/ coherency
- Single z7 lockstep core @ 264MHz (for ISO26262 and ASIL-D)
- 4.25MB Flash RWW w/ ECC including 4 x 64kB EEPROM
- 512kB SRAM w/ ECC (up to 48KB standby)
- 45kB eTPU RAM , 32kB data cache (w/ line locking)
- Integrated ecurity w/ PASS, TDM (Tamper Detection), & CSE2 (Crypto Services Engine for Encryption & Secure Boot)

I/O & System

- Up to 70ch eQADC from 4 converters w/12bit resolution
  - On-chip temperature sensor and VGA (x1,x2,x4)
  - 12 x Decimation Filters w/ hardware knock integrators
- Timers – up to 128 channels (96ch eTPU2+ and 32ch eMIOS)
- 2 x 64ch eDMA support (128ch total)
- 6 x CAN ports (4 x CAN + 2 x CANFD) and Ehernet
- DSPI – 5 *channels (2 supporting µSec ch.)*
- eSCI – *6 channels (2 supporting uSec ch.)*
- Reaction module w/ 8 channels for current control
- Up to 12ch SENT
- 1 x CRC unit – w/ 3 independent channels,
- 4 x protected port outputs, MPU and MMU
- FMPLL + PLL
- Safety Monitors – e2eECC, CLK, Voltage, Fault Collection



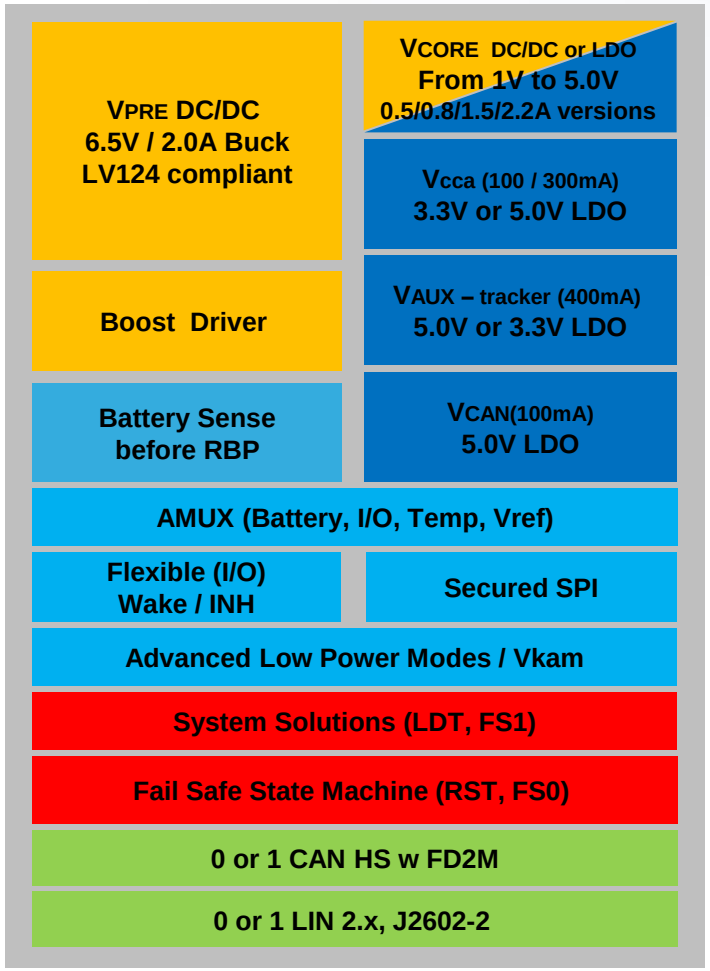
FS65XX Functional Safety SBC - ASILD

Advanced Power Management

- Buck/Boost Vpre from 2.7 to 36V
- 2.0A / 6.5V Vpre capable
- FS65xx with Vcore 2.4MHz SMPS 0.8/1.5/2.2A
- FS450x with Vcore LDO 0.5A
- Configurable Vcore (external resistor bridge)
- Multiple LDO and Tracker
- Ultra Low Standby Current 30µA

System Solution

- Analog Multiplexer to sense multiple critical signal
- Small package size :49 mm²
- Robust CAN PHY FD 2M
- Configurable I/Os
- Long Duration Timer, Keep Alive memory supply



Independent Safety Monitoring

- **Single Point Failure :** UV/OV Monitoring Unit
- **Latent Failure :** ABIST & LBIST
- **Common Cause Failure :** Independent electrical and physical fail safe circuitry and state machine
- **Reset, Fail Safe** pin to set system in predictive state when system is failing.
- **Configurable Fail Safe State**, while allowing system availibility, diagnostic and possible recovery.
- Optional **Fail Silent** operation
- **Second Fail Safe** pin to manage safe delay after failure event
- **Advanced SafeAsssure documentation** to fit for safety assessment
- **BOM cost savings :** No need for external MCU challenger
- MCU & external IC **Safety Monitoring**

SCALABLE
Family concept

PROVEN
Designed at OEMs

SAFE
Flexible Fail Silent

ROBUST
PASS 4200h HTOL

SIMPLIFIED
Tools & Documents

GD3100 IGBT Gate Driver with High Voltage Isolation

ASIL C/D ISO26262 compliant advanced gate driver for high voltage power IGBTs with integrated high voltage isolator, high speed current sense interface and robust functional safety mechanisms

Differentiation:

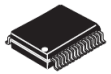
- **Fast short circuit** protection via direct feedback through i-sense IGBTs
- **High speed over current** protection with **soft shutdown**
- SPI interface for **ASIL C/D** monitoring/reporting and programmability
- Integrated **temperature sense** soft shutdown for **system protection**
- **Integrated galvanic signal** isolation
- Compact 10 x 18 mm SOIC package for reduced PCB area

Features:

- **Integrated gate drive** power stage capable of **10A** source and sink
- Compatible with 200V to 1700V IGBTs with power range >125kW
- Isolated **AMUX** for monitoring key circuit voltages and currents
- Gate-emitter **clamp eliminating** need for **negative gate** supply voltage

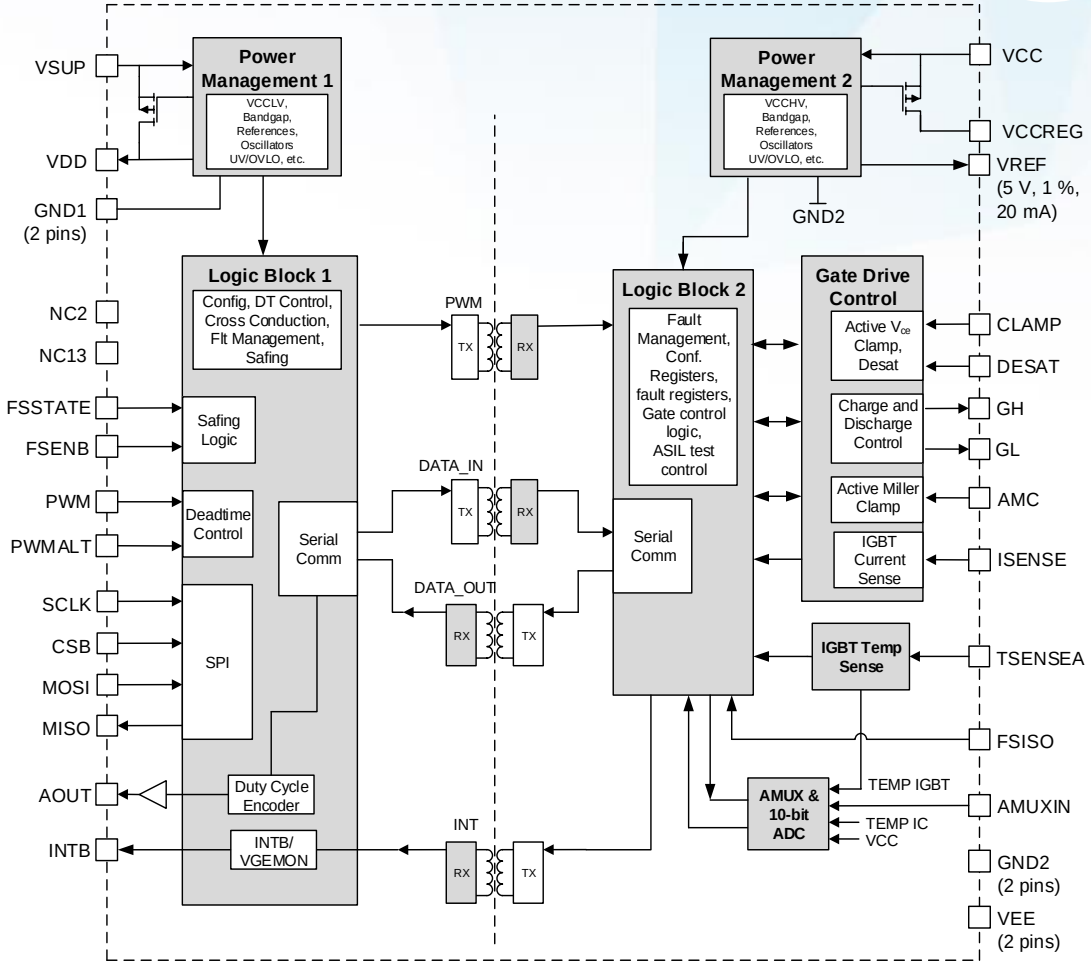
Applications:

- HEV Motor Inverters
- HV UPS Inverters
- Alternate Energy Inverters



32-Pin
SOIC-WB

PART #	PKG	SAMPLES	RELEASE
MC33HB3100EK	SOICWB32	NOW (P2.1	Q1'18



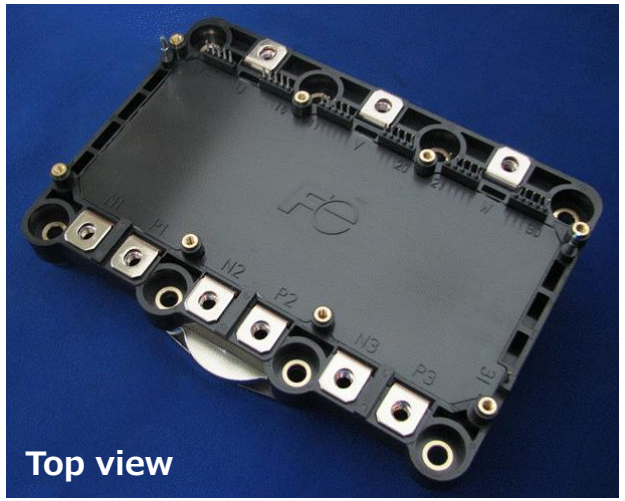
Fuji 750V/800A 6-in-1 Power Inverter Module

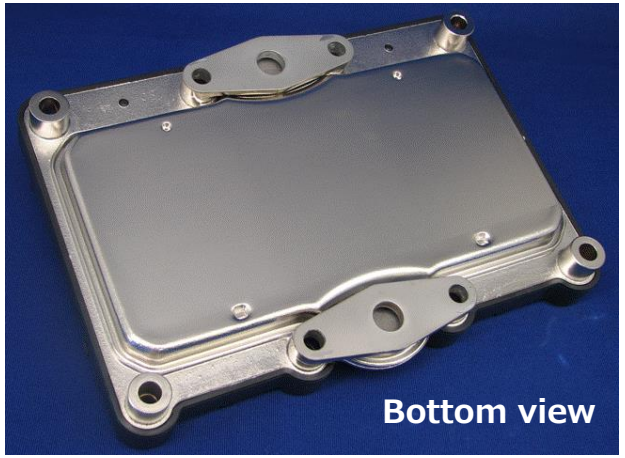
Features:

- 750V/800A 6-in-1 3-phase power inverter module
- Reverse-conducting IGBT with integrated temperature sensor
- Integrated ‘i-Sense’ current sensor for fast over-current detection
- 162mm × 117mm × 24mm compact direct-cooling water-jacket aluminum housing with new thin fin structure
- Flange structure at cooling water IN/OUT for 30% lower thermal resistance vs conventional fin type heat sink.
- 175℃ guaranteed operating temperature range

Application Example:

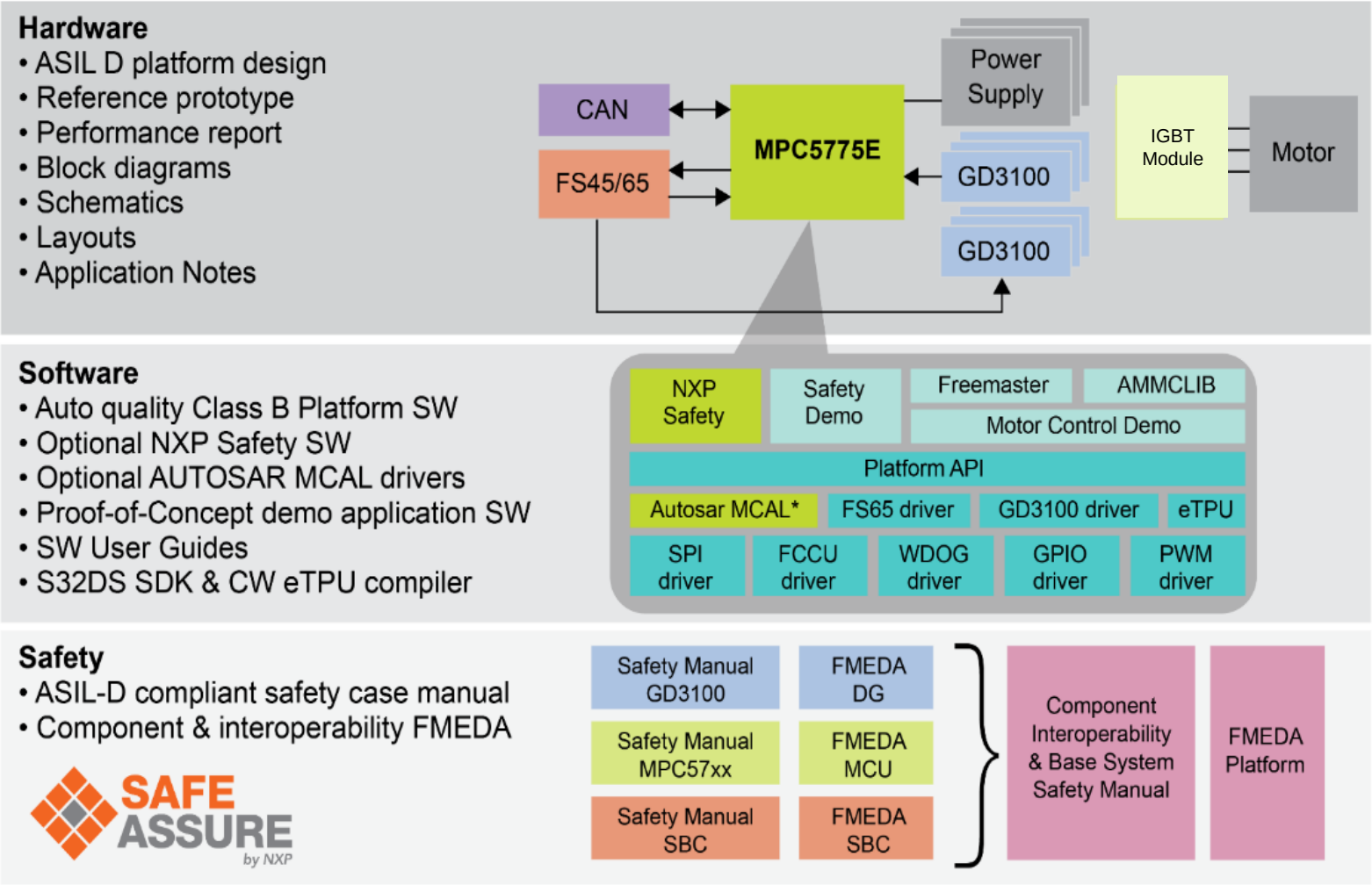
- 70～120kW motor output power
  - fsw=6kHz
  - Coolant temp.=65℃
  - Coolant flow rate=10L/min
  - Vdc=450V
  - Ipeak=460Arms @ 1s
  - Icont.=430Arms





VEPCO Engineering Services - Advanced development assistance

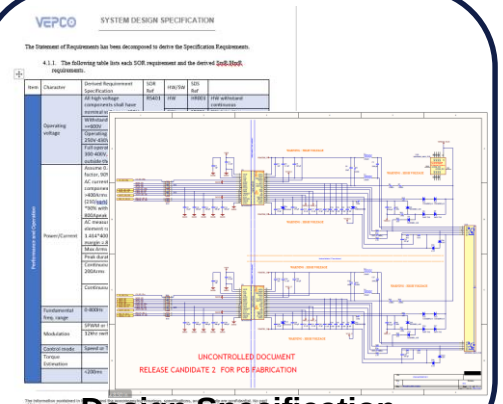
- **FS65xx** robust fail-silent SBC with operation from 36V down to 2.7 V
- **MPC5775E** secure multi-core 32-bit lockstep MCU with SW resolver
- **GD3100** isolated IGBT gate driver with <2us over-current protection
- **TJA1042** redundant CAN bus interface with low power standby
- **Enablement software** with API and functional safety case



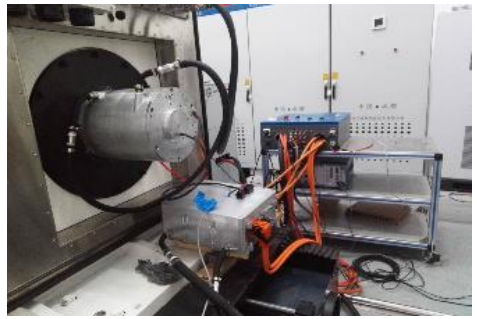
VEPCO
www.vepcotech.com

VEPCO Engineering Services - Advanced development assistance

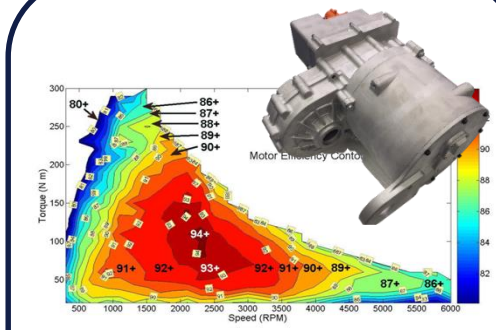
HW proof of concept



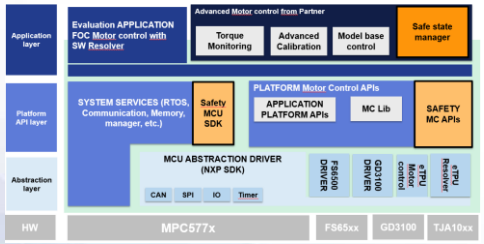
Design Specification



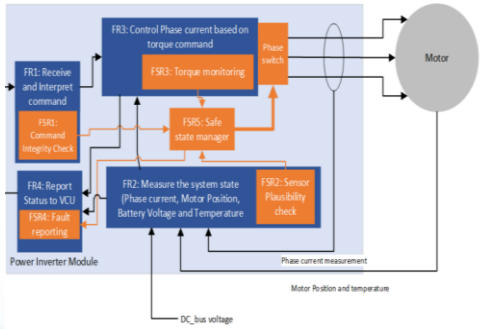
On-site dyno testing



Inverter Design and Motor design customization



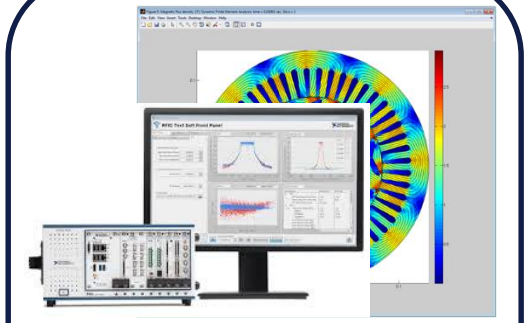
Software enablement



Functional safety concept

SAFE ASSURE™ by NXP

Functional safety library



Custom motor calibration

Package Offering and Ordering

Inverter Platform Enablement Kit: $5000

KIT INCLUDES

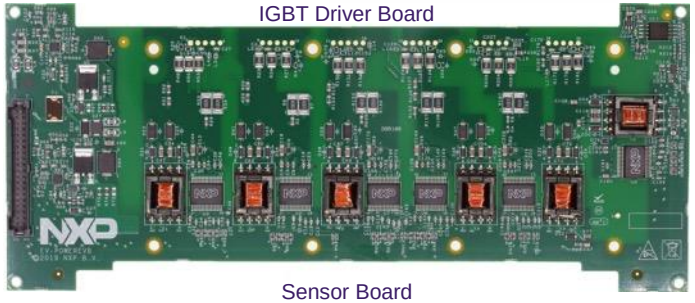
Offerings	Type	Offering Packages	
		Inverter Platform Enablement Kit	Inverter Platform Safety Kit *
Hardware design package (schematics & layout)	DOC	DL	
NXP device datasheets	DOC	DL	
NXP device functional safety documents	DOC	DL	
NXP device software drivers (GD3100 & FS65)	SW	DL	
Reference design enablement kit including control, driver, RDC interface, & sensor boards	HW	X	
BSW with service level, SDK, driver & GUI software	SW	DL	
Reference design enablement kit user manual	DOC	DL	
Design guide application note	DOC	DL	
BSW user manual	DOC	DL	
System proof-of-concept prototype test results	DOC	DL	
Safety basic software & safe-state library	SW		DL
Basic safety software user manual	DOC		DL
Inverter safety concept manual			
Analysis & fault reaction matrix	DOC		DL

DL = downloadable from NXP

* Available by end of 2019

Microcontroller Control Board

IGBT Driver Board



Sensor Board

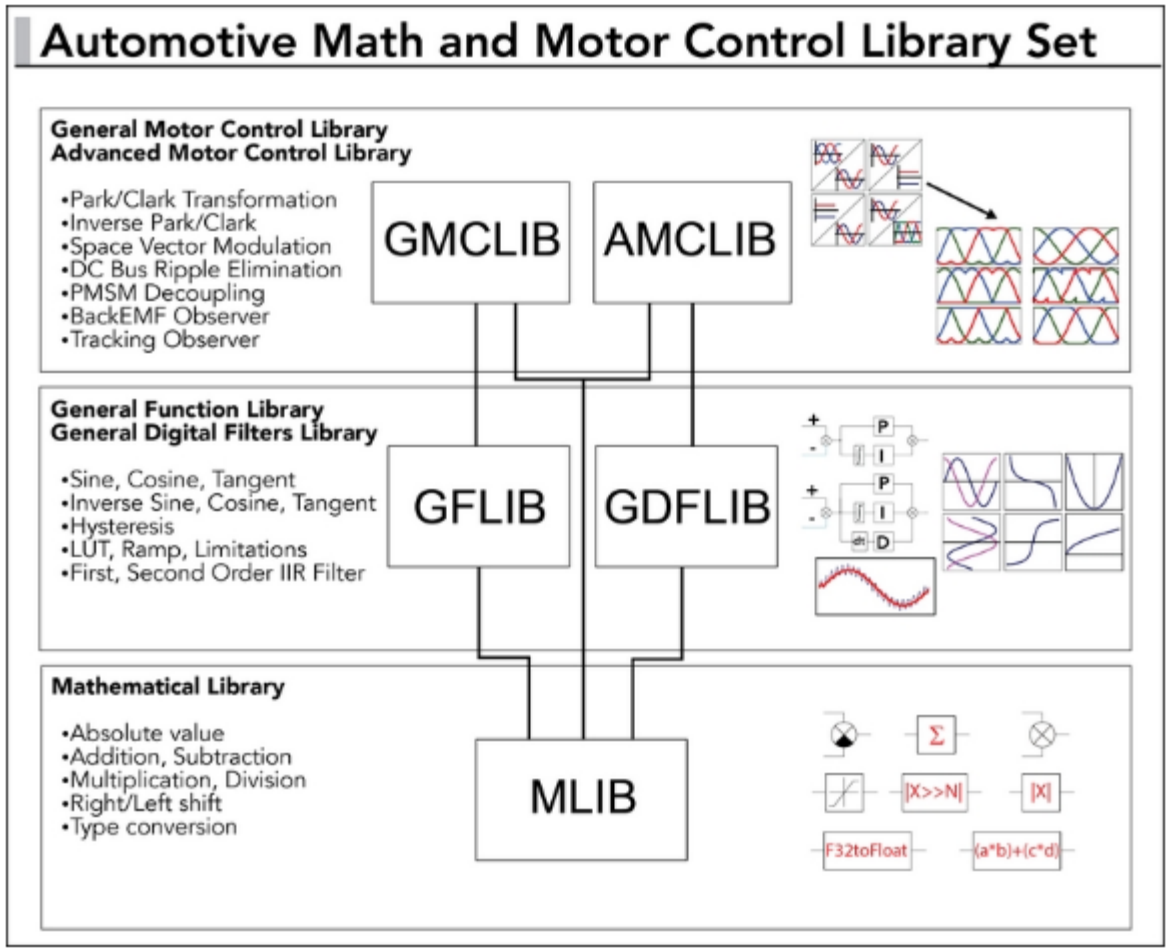
Interface Board

AMMCLS – FOC Algorithm

Automotive Math and Motor Control Library Set

Basic mathematical functions (MLIB) with elementary math functions
General motor control functions (GMCLIB) with space vector modulation, transformation and motor control specific functions
General digital filters functions (GDFLIB) with digital filter functions for signal control
Advanced motor control functions (AMCLIB) with BEMF observers for sensor-less applications and PMSM field weakening controller

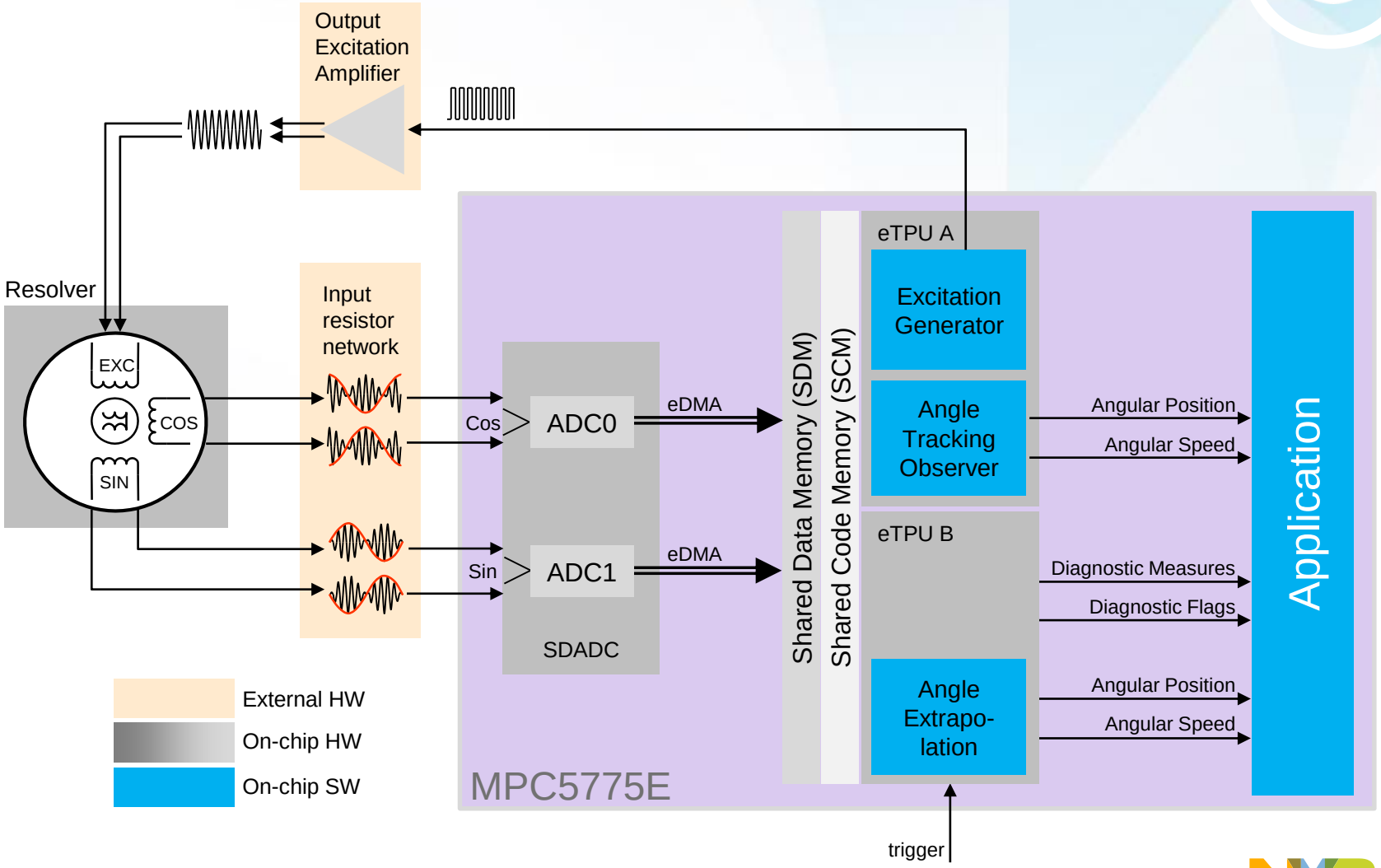
Developed according to SPICE Level 3 and ISO9001/TS16949 processes
Highly speed-optimized, including the SPE/SPE2/LSP optimization
Supplied as a binary file, source code available in the licensed version
MATLAB/Simulink® models for user application modeling



eTPU-Based SW Resolver to Digital Converter

Block diagram and performance specifications

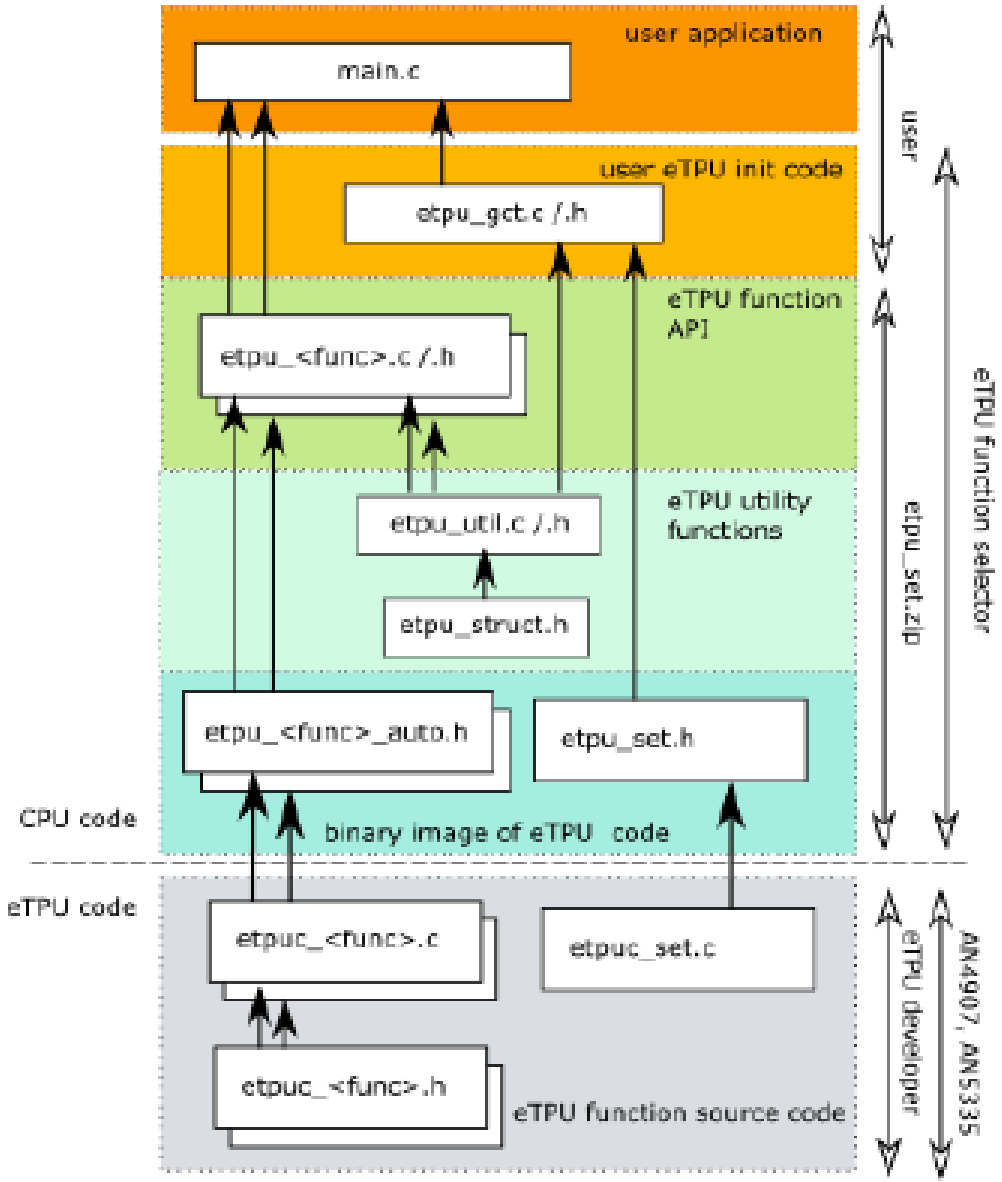
Parameter	Value
Output Resolution	2^{24}
Accuracy	±0.1º
Max angular acceleration (bandwidth dependent)	
Phase delay Output response time	±0.12º / 10k min^{-1} 2 µs
Tracking rate	300,000 min^{-1}
Settling time w/ 180º step input (bandwidth dependent)	4.8 ms @ 0.2 kHz BW 0.38 ms @ 2.5 kHz BW
Start-up time	25 ms
Algorithm Type	Angle tracking observer w/ error calc after demod
Output form	24-bit fractional
Diagnostics	Signal Loss (LOS) Signal Degradation (DOS) Tracking Loss (LOT) Signal Disconnects Signal Shortcuts



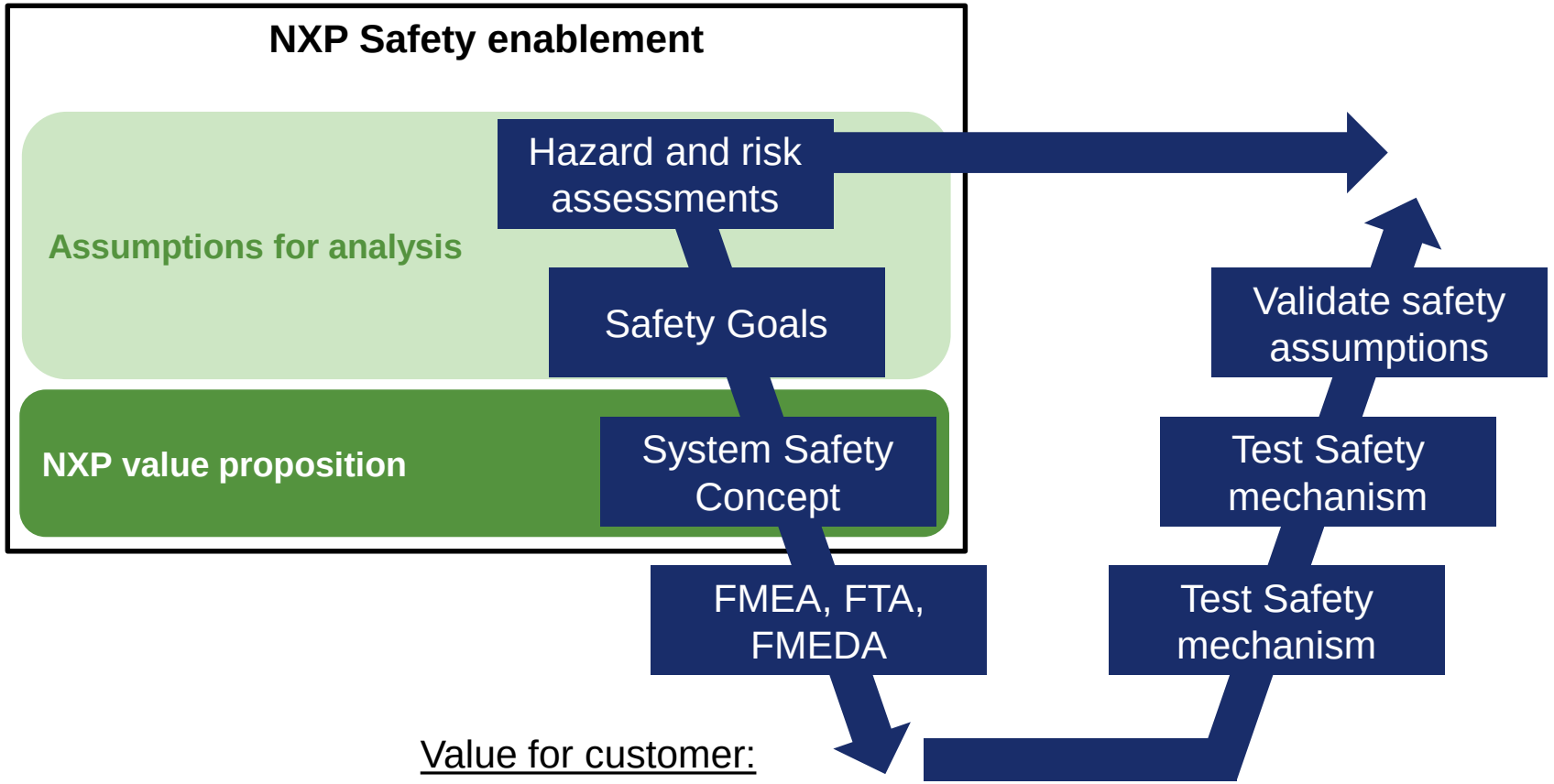
eTPU Motor Control Software

- CPU independent motor drive
- SDADC periodically sensing resolver Sin and Cos
- eQADC sensing phase currents (I_a,I_b,I_c) and DC bus voltage
- dDMA transfers date between ADCs and eTPU

eTPU handles:
- Resolver ATO
- PMSM FOC
- PWM Generation
- ADC synchronization



NXP - Vepco reference design – Safety enablement



NXP Safety support
Professional services

Access to Safety expert:
- System design
- IC design

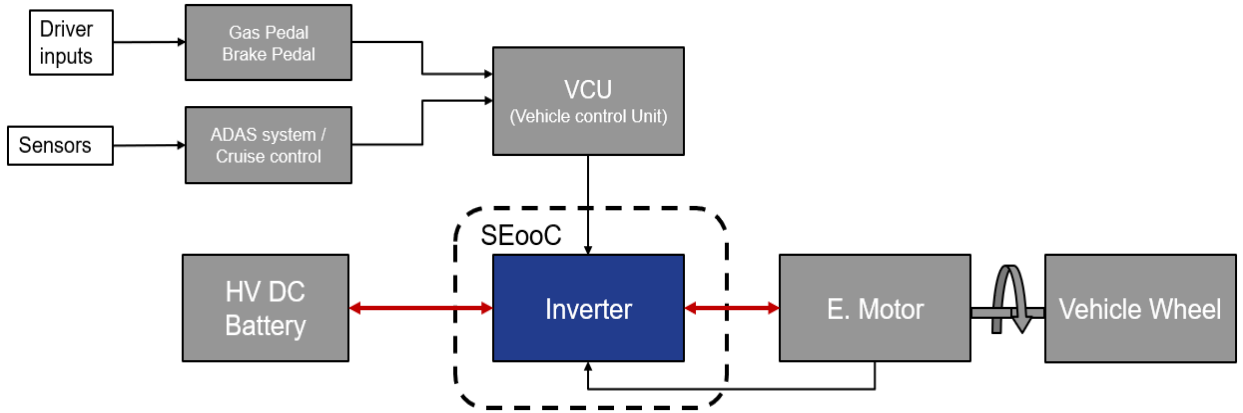
Support for:
- Customization
- Safety Metrics
- Safety Process
- Interaction with certification agencies

<u>Value for customer:</u>

- Help customer on their safety architecture
- Reduce engineering time (~6 months - 1year)
- Methodology for start-ups and new OEM

- **Not a “T1 certified” platform**
- **But more than a standard demo (~ A or B samples)**

Example of Assumptions and Safety goals

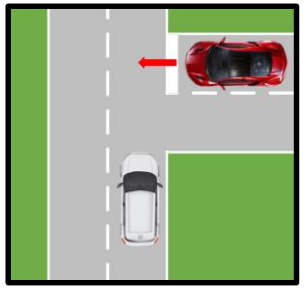


Assumption:

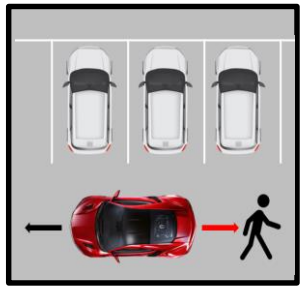
- Single permanent magnet motor PMSM
- No clutch

-> Cannot open motor phases at high speed !
(Back EMF, High braking power, SG5 violation)

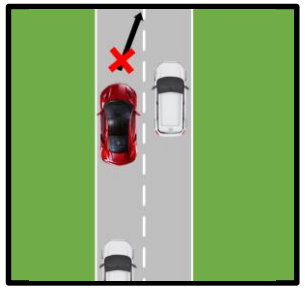
Traction hazards



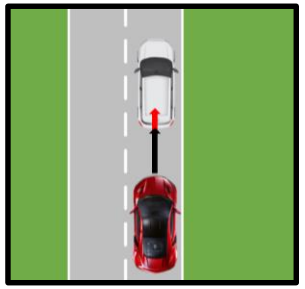
Unintended self acceleration while in stop



Unintended reverse speed wheel while in stop or parking

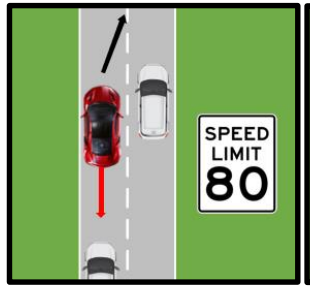


Unintended loss of torque while driving (overtaking)

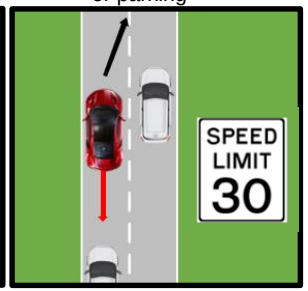


Unintended over torque while driving

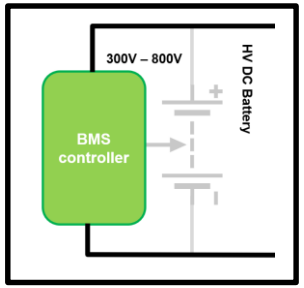
Braking hazards



Unintended self braking while driving at high speed



Unintended self braking while driving at low speed

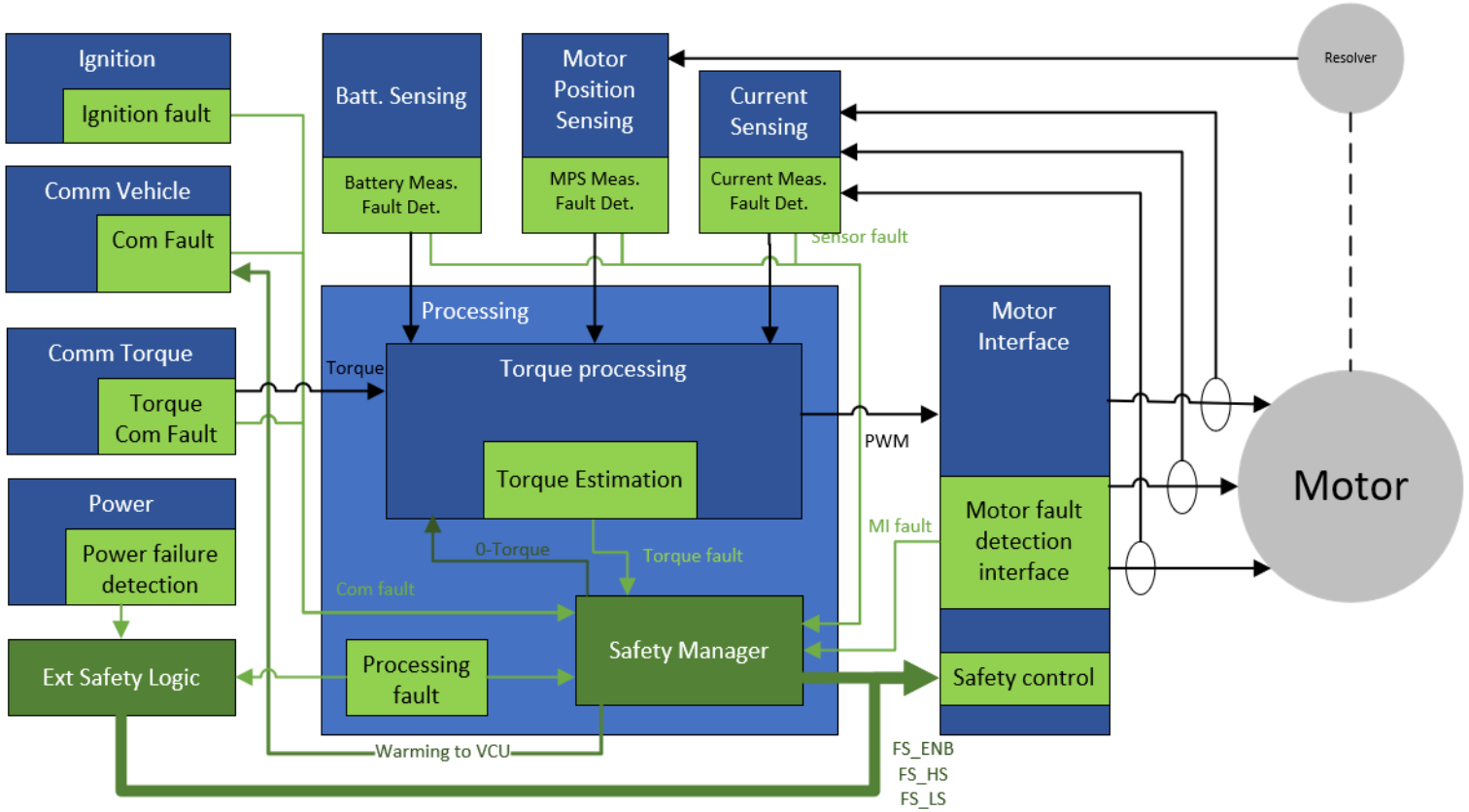


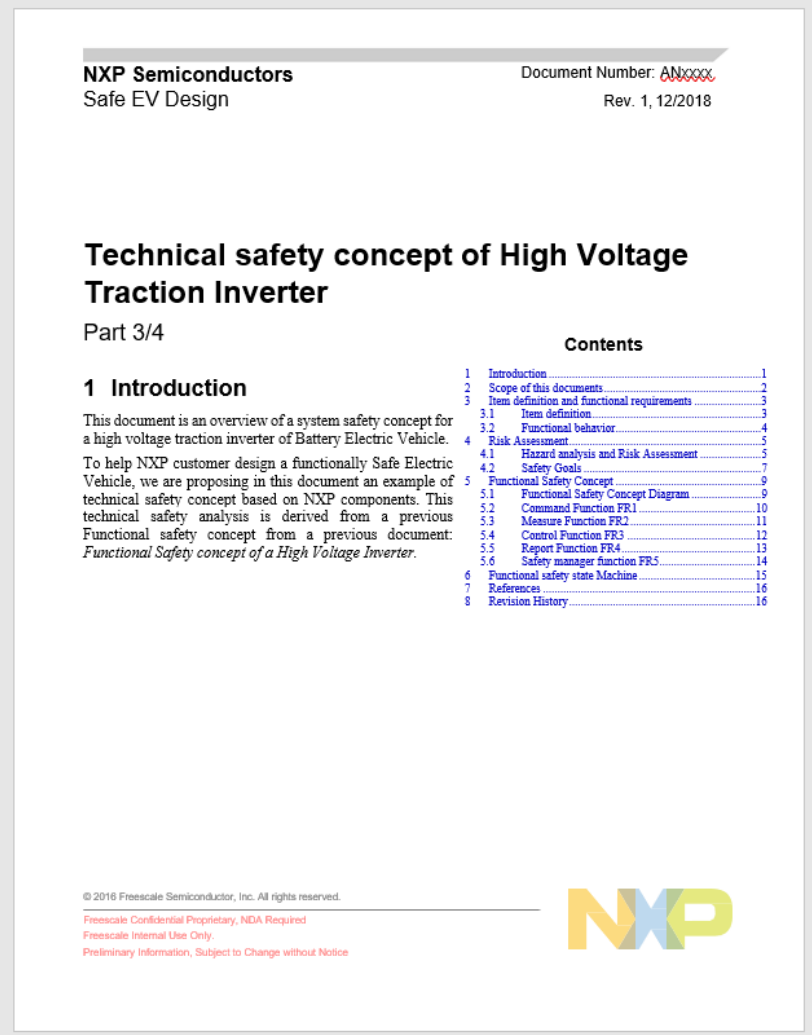
Unintended regeneration inside the HV Battery that could result in fire hazard

Safety goal	ASIL
SG1: Avoid unintended acceleration while in stop	D
SG2: Avoid unintended acceleration , torque lock or over acceleration torque while driving	B
SG3: Avoid reverse torque	D
SG4: Avoid sudden loss of acceleration torque	B
SG5: Avoid self-braking torque while driving at high speed	D
SG6: Avoid self-braking torque while driving at low speed	B

* One possible example, customer can have different safety goals

Technical Safety Requirements





NXP Semiconductors
Safe EV Design

Document Number: ANxxxx
Rev. 1, 12/2018

Technical safety concept of High Voltage Traction Inverter

Part 3/4

1 Introduction

This document is an overview of a system safety concept for a high voltage traction inverter of Battery Electric Vehicle.

To help NXP customer design a functionally Safe Electric Vehicle, we are proposing in this document an example of technical safety concept based on NXP components. This technical safety analysis is derived from a previous Functional safety concept from a previous document: *Functional Safety concept of a High Voltage Inverter*.

Contents

1 Introduction 1
2 Scope of this documents 2
3 Item definition and functional requirements 3
3.1 Item definition 3
3.2 Functional behavior 4
4 Risk Assessment 5
4.1 Hazard analysis and Risk Assessment 5
4.2 Safety Goals 7
5 Functional Safety Concept 9
5.1 Functional Safety Concept Diagram 9
5.2 Command Function FR1 10
5.3 Measure Function FR2 11
5.4 Control Function FR3 12
5.5 Report Function FR4 13
5.6 Safety manager function FR5 14
6 Functional safety state Machine 15
7 References 16
8 Revision History 16

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NXP EV-INVERTER Reference Platform Summary

Reference Platform

- Open system IP with hardware, Basic SW enablement and Safety concept
- Optimized BOM solution targeting ASIL-D
- System safety concept based on NXP’s Safety IC and ISO26262 methodology
- Automotive Quality proof-of-concept prototype available for Dyno Testing
- System design partners (e.g. Vepco) to reduce customer engineering efforts

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