DSC Architecture & Applications

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SECURE CONNECTIONS FOR A SMARTER WORLD

OVERVIEW

- The 56800EX core for Digital Signal Processing
- SoC Building Blocks
- Unique Features
- AC/DC Applications
- DC/DC Applications
- Q & A

DSC, a specialized MCU for

- Energy Conversion
  - Solar Power Inverter
  - Switched Mode Power Supply
  - Medical Power
- Motor control
  - 3 Phase AC Induction Motor
  - Brushless DC Motor
  - Permanent Magnet Synchronous Motor
- 100Mhz 32-bit 56800EX CORE Unifies DSP instructions into MCU core
- Specialized Analog, PWM IPs

MC56F83XXX BLOCK DIAGRAM

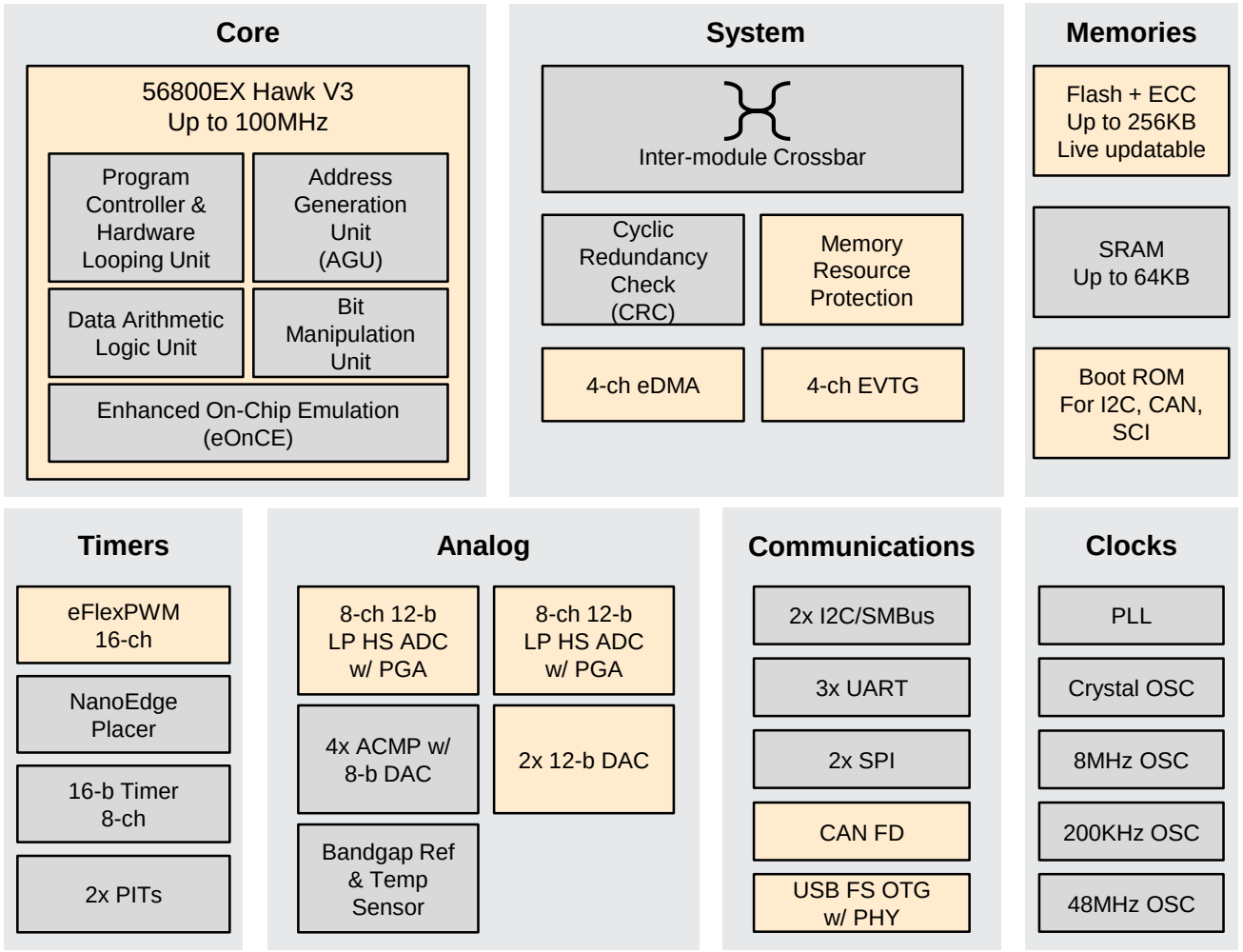
Key Features:

Core & System
- **56800EX Hawk V3** supporting fractional arithmetic with 4 ACC, separate program and data memory maps, nested looping, and a superfast interrupt
- Inter-module crossbar directly connecting any input and/or output with flexibility for additional logic functions (AND/OR/XOR/NOR) and EVTG
- eDMA controller for reduced core intervention when shifting data from peripherals
- Memory protection unit to ease safety certification

Timers
- eFlexPWM – Most advanced timer for Digital Power Conversion with up to 16ch 312pico-sec resolution, supported by 8 independent time bases, with half cycle reloads for increased flexibility and best in class performance
- QTimer – Up to 12 functions integration to reduce the function peripherals number

Analog
- 2x 12-bit high-speed Cyclic ADCs each with 300ns conversion rates and low power consumption
- Integrated PGAs to increase the accuracy of ADC conversions on small voltages and currents
- 2x 12-bit DACs with hardware sync updating
- 4 analog comparators with integrated 8-bit DAC that can enable emergency shutdown of the PWMs

Others:
- CAN FD – Supporting higher data rates to address the ever-evolving requirements of industrial and automotive markets
- USB OTG-capable (On-The-Go) controller complies with the USB 2.0 spec (only for 100LQFP)
- 5-volt tolerant I/O for cost-effective board design
- Supply voltage from 2.7V to 3.6V (analog performance degrading below 2.95V)
- Both -40~105C and -40~125C grades, ASILB qualification (ongoing)



Packages:
100LQFP, 80LQFP, 64LQFP, 48LQFP

Instruction Fetch:

PAB - 21 bits
PDB - 16 bits

1st Data Access:

XAB1 - 24 bits
CDBR - 32 bit
CDBW - 32 bit

2nd Data Access:

XAB2 - 24 bits
XDB2 - 16 bits

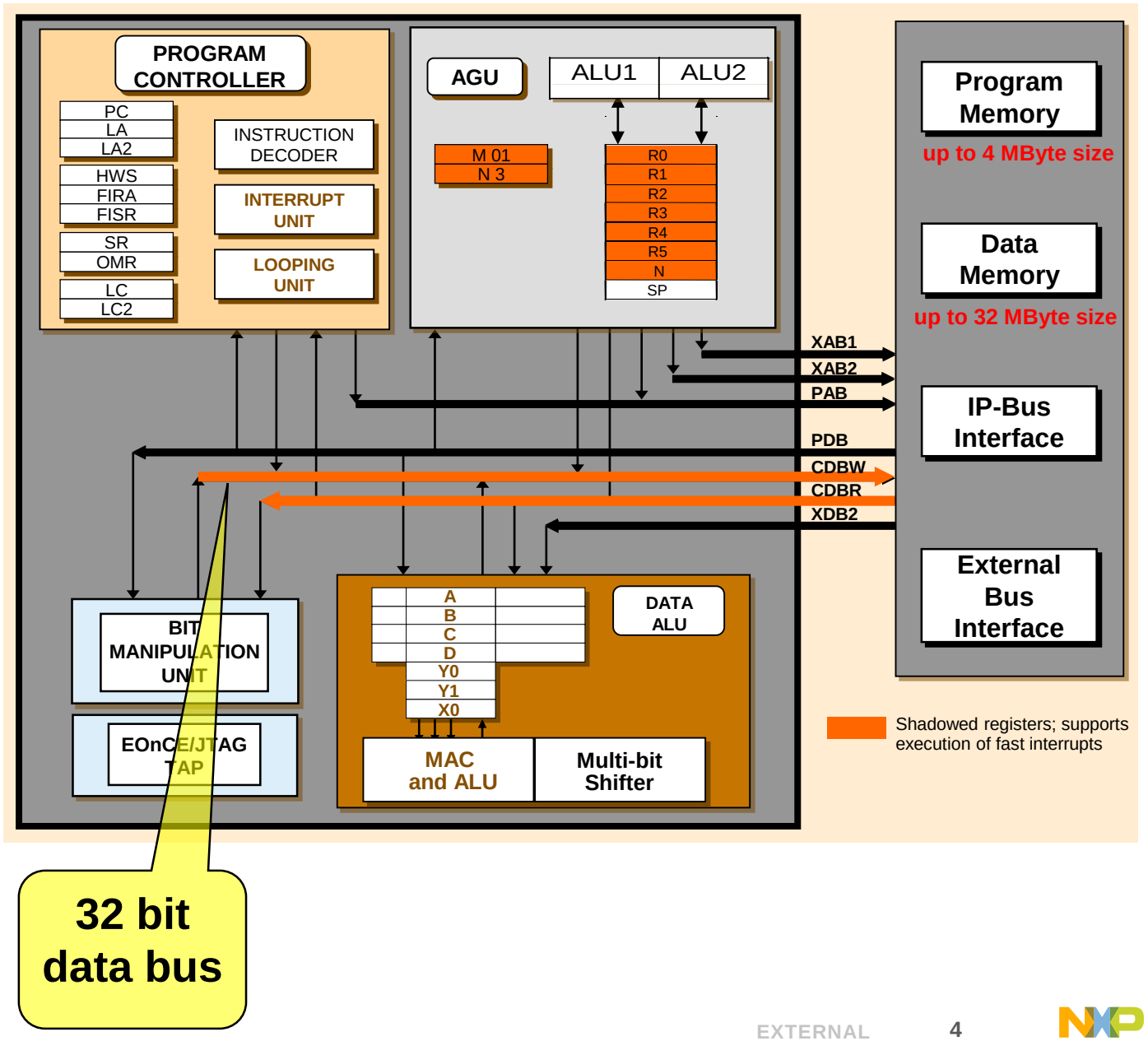
Operations Performed:

1st - PAB / PDB
2nd - XAB1 / CDBR- CDBW
3rd - XAB2 / XDB2

Fast Interrup

Harware do loop

The 56800EX CORE



MAC INSTRUCTION, NORMAL INTERRUPT

$$y(n) = \sum_{i=0}^{N-1} c(i)x(n-i)$$; Typical Digital Filter Formula

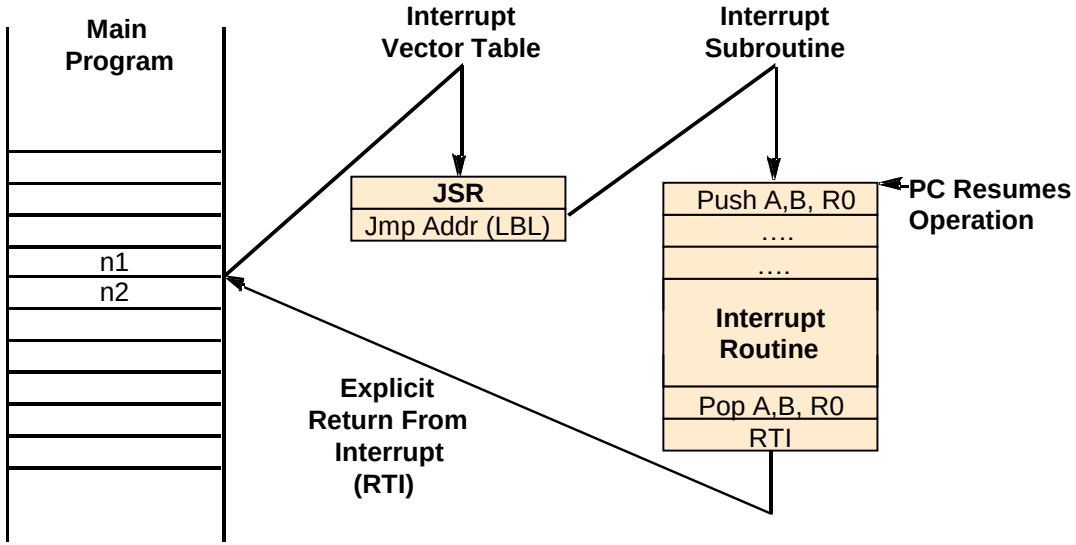
Parallel Move

```
MACR X0,Y0,A     X:(R0)+N,Y0     X:(R3)-,X0
```

OPCODE AND OPERANDS

PRIMARY READ (Uses XAB1 and CDBR)

SECONDARY READ (Uses XAB2 and XDB2)



General Case:

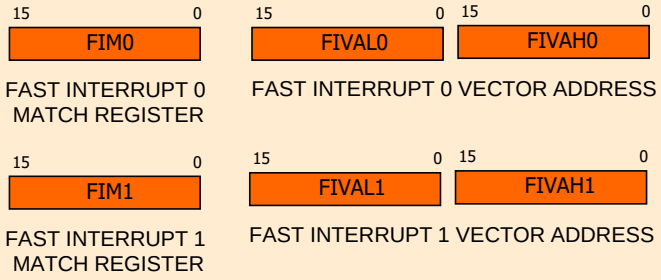
- Vectored Interrupts - Vectors may be located anywhere in Program Memory (controlled by VBA)
- Priority Levels 0,1,2,3 - Highest is non-maskable
- Software Traps at each priority level
- One additional software trap (5th level) at lowest priority for O/S support

FAST INTERRUPT PROCESSING

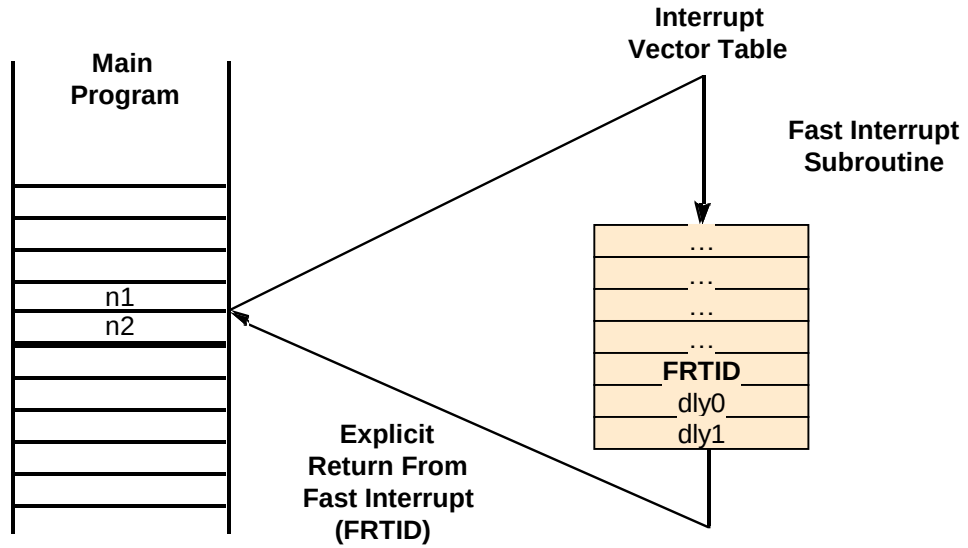
• Establishing of Fast Interrupts

- ✓ Setting the priority of the interrupt as level2, with the appropriate field in the IPR registers.
- ✓ Setting the FIM0 and FIM1 registers to the appropriate vector numbers.
- ✓ Setting the FIVAL0 and FIVAH0 registers with the address of the service code for the fast interrupt.
- ✓ The core then fetches the instruction from the indicated vector address and if it is not a JSR, the fast interrupt starts

ITCN FAST INTERRUPT REGISTERS



• Implemented Techniques

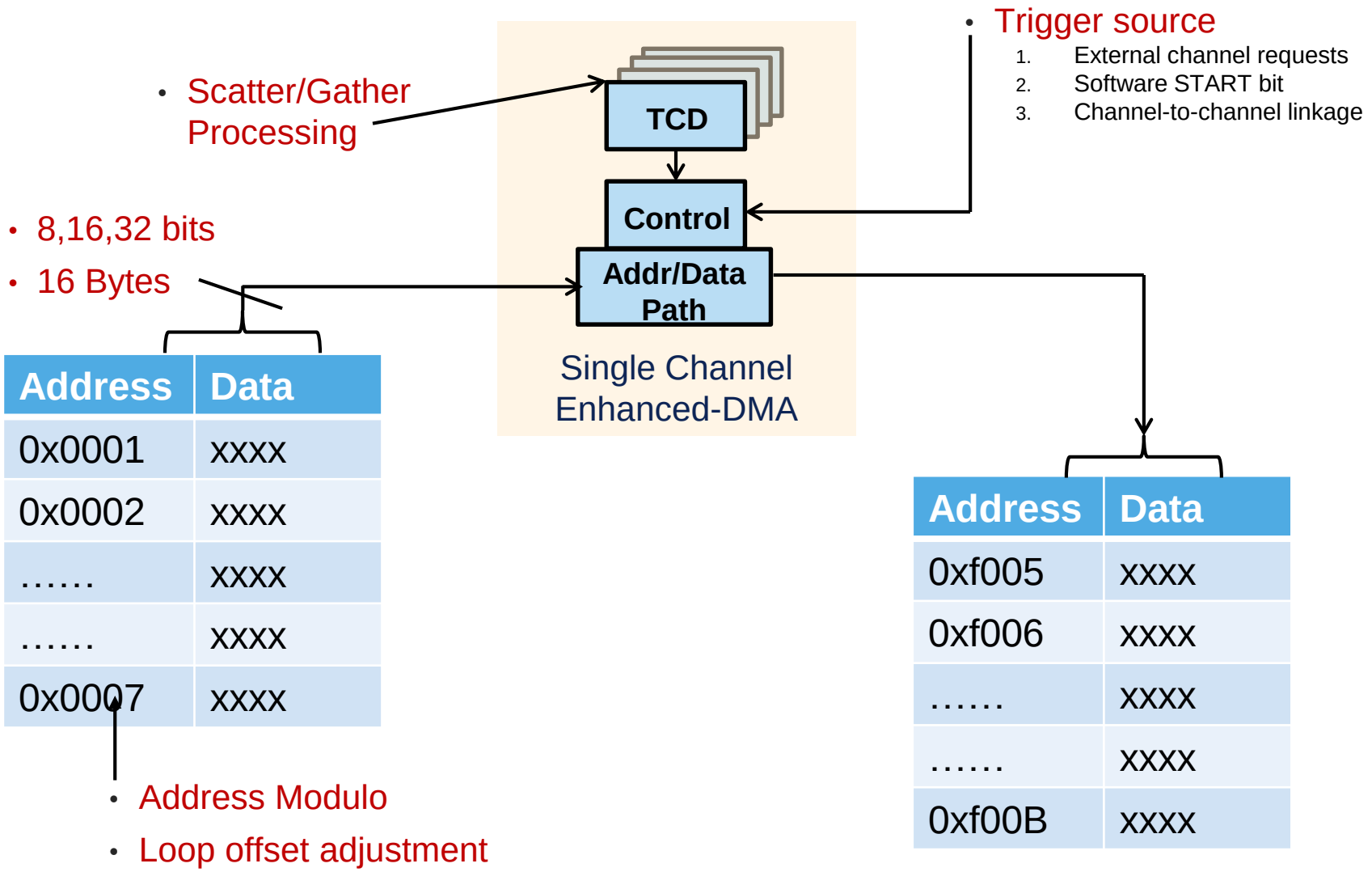


• Improved Latency and Throughput

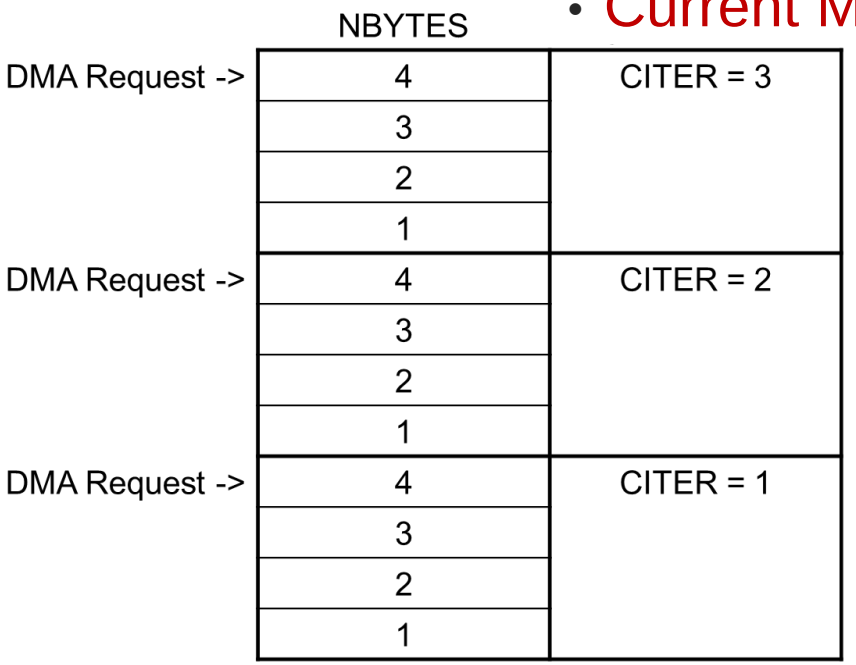
- ✓ Overcome vectors and jumps directly to service routine
- ✓ Automatically swaps registers with shadows: R0~5, N, and M01
- ✓ Automatically aligns SP and pushes the Y0 and Y1 registers onto the stack
- ✓ Automatically advances the SP to an empty 32-bit location and automatically restores above registers on exit

The enhanced DMA

- The enhanced direct memory access (eDMA) controller is a module capable of performing complex data transfers with minimal intervention from a host processor.
- The eDMA module works in conjunction with the direct memory access multiplexer (DMAMUX), which routes DMA sources, called slots , to any of the DMA channels.
- The eDMA module in 56F83xxx has 4 channels, supporting fixed-priority and round-robin channel arbitration.
- Each channel supports two-deep nested transfers called minor and major loops.


Scatter/Gather Processing
Trigger source
1. External channel requests
2. Software START bit
3. Channel-to-channel linkage
TCD
Control
Addr/Data Path
Single Channel Enhanced-DMA
8,16,32 bits
16 Bytes
Address
Data
0x0001
xxxx
0x0002
xxxx
……
xxxx
……
xxxx
0x0007
xxxx
Address Modulo
Loop offset adjustment
Address
Data
0xf005
xxxx
0xf006
xxxx
……
xxxx
……
xxxx
0xf00B
xxxx

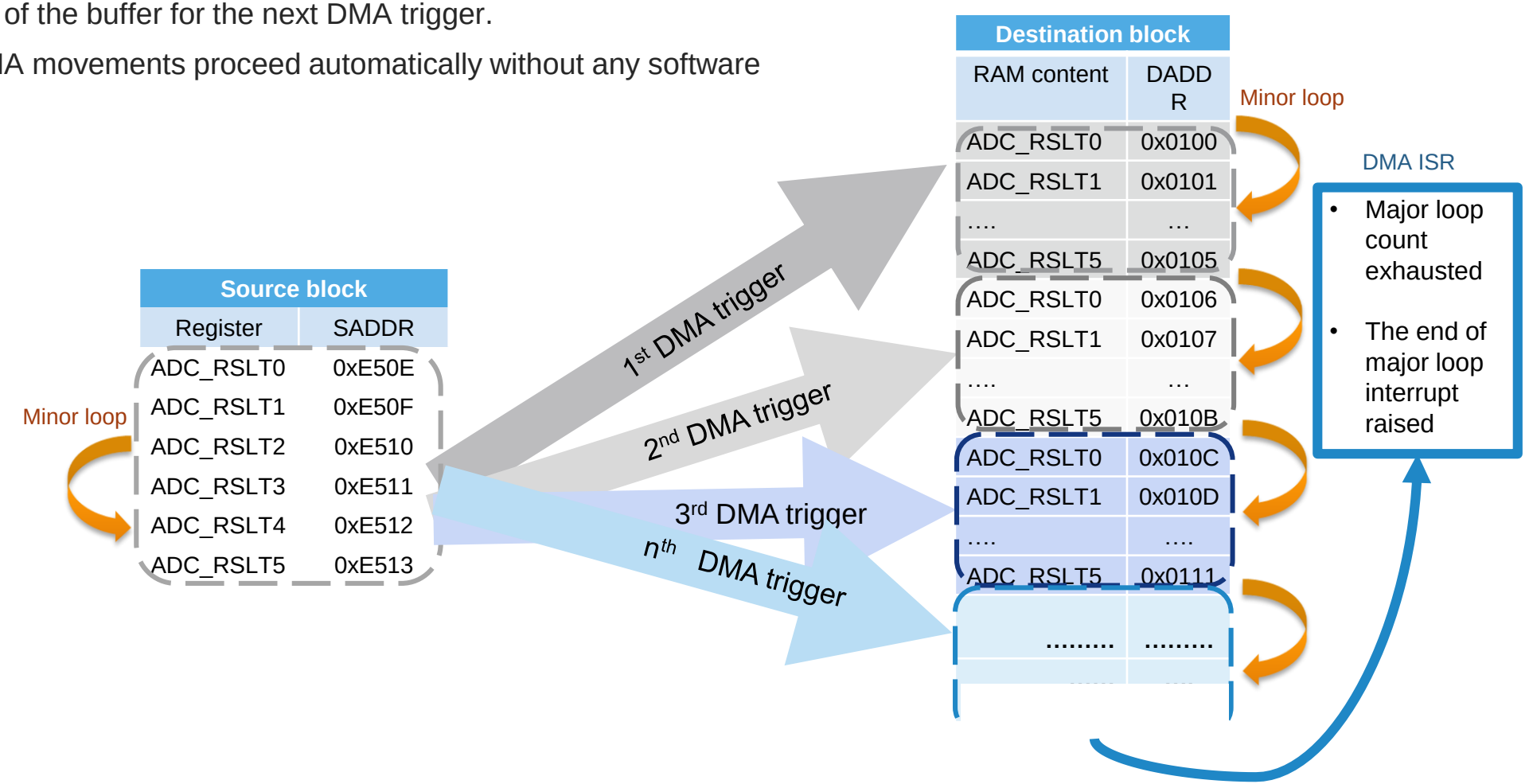
- Current Major Iteration count



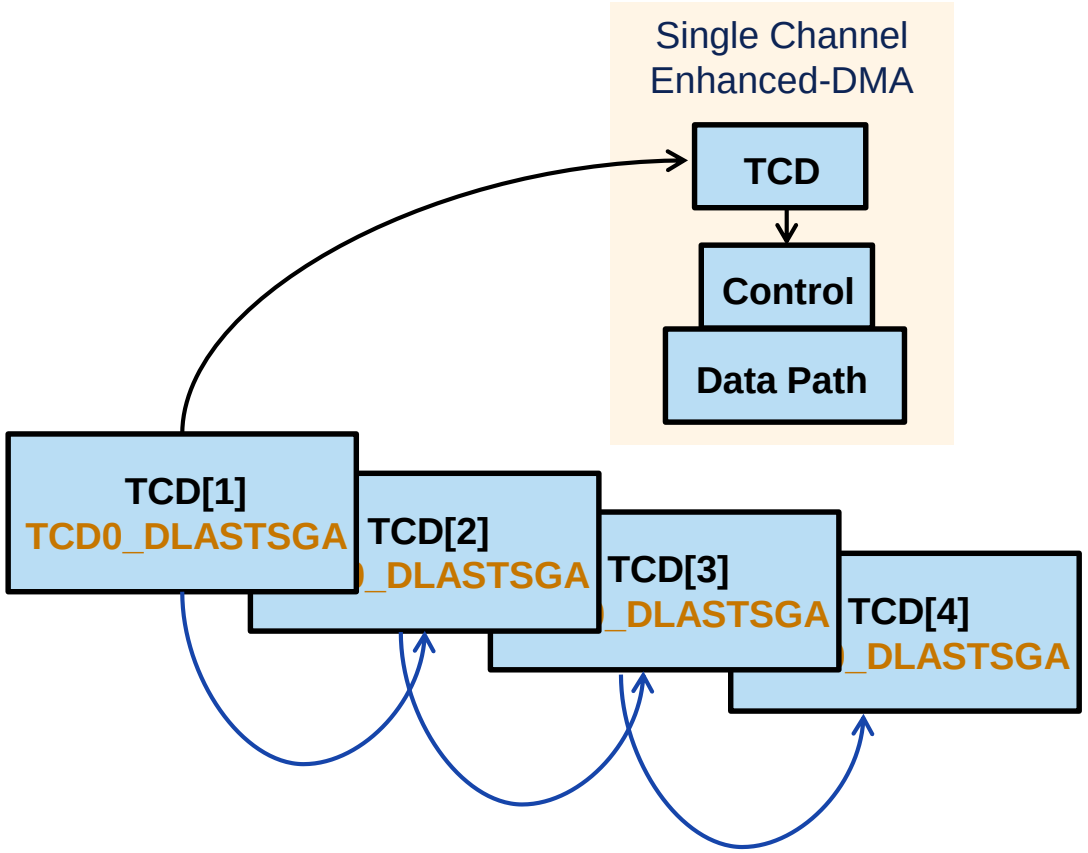
- At the end of Major loop
  1. SADDR += SLAST (Source address Last adjustment)
  2. DADDR += DLASTSGA (Destination address Last adjustment)
  3. CITER = BITER (Starting value for CITER)
  4. Assert the start bit for linked eDMA channel
  5. Requests interrupt, if TCD[x].CSR[INTMAJOR] enabled
  6. Assert the start bit for linked eDMA channel

APPLICATION INSTANCE 1: MULTIPLE ADC CHANNELS OVERSAMPLING

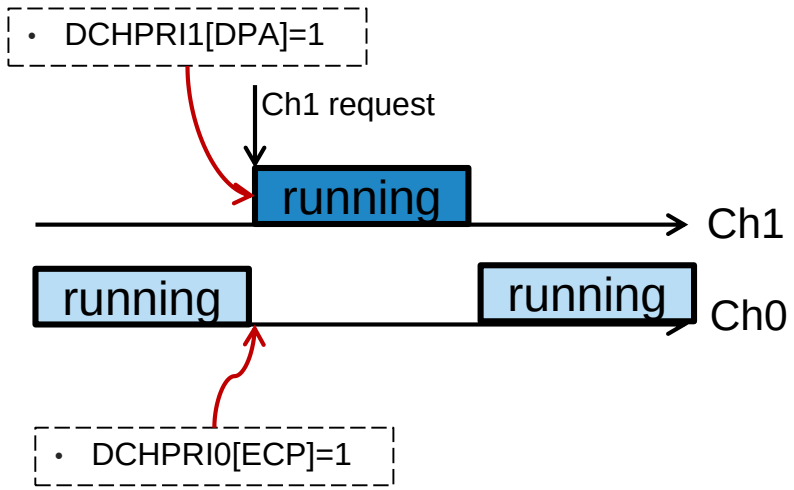
- In this example, we transfer the contents of ADC_RSLT0~ADC_RSLT5 to a circular buffer on every DMA trigger signal (this signal is ADC EOS in this case). Once the destination buffer is full, the major loop interrupt generated for users to process the data in the buffer, and DADDR will roll back to the beginning of the buffer for the next DMA trigger.
- These DMA movements proceed automatically without any software overhead.



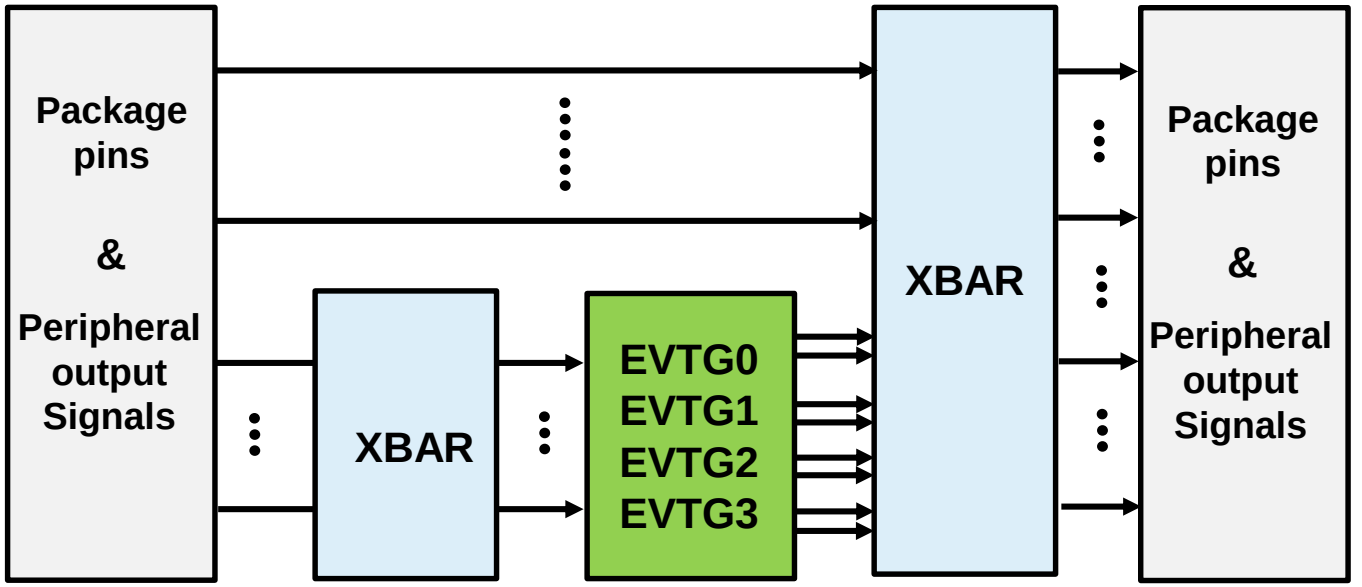
- TCDn_CSR[ESG] = 1
- At the end of major loop, load DLASTSGA pointed TCD settings
- Infinity data movement profiles



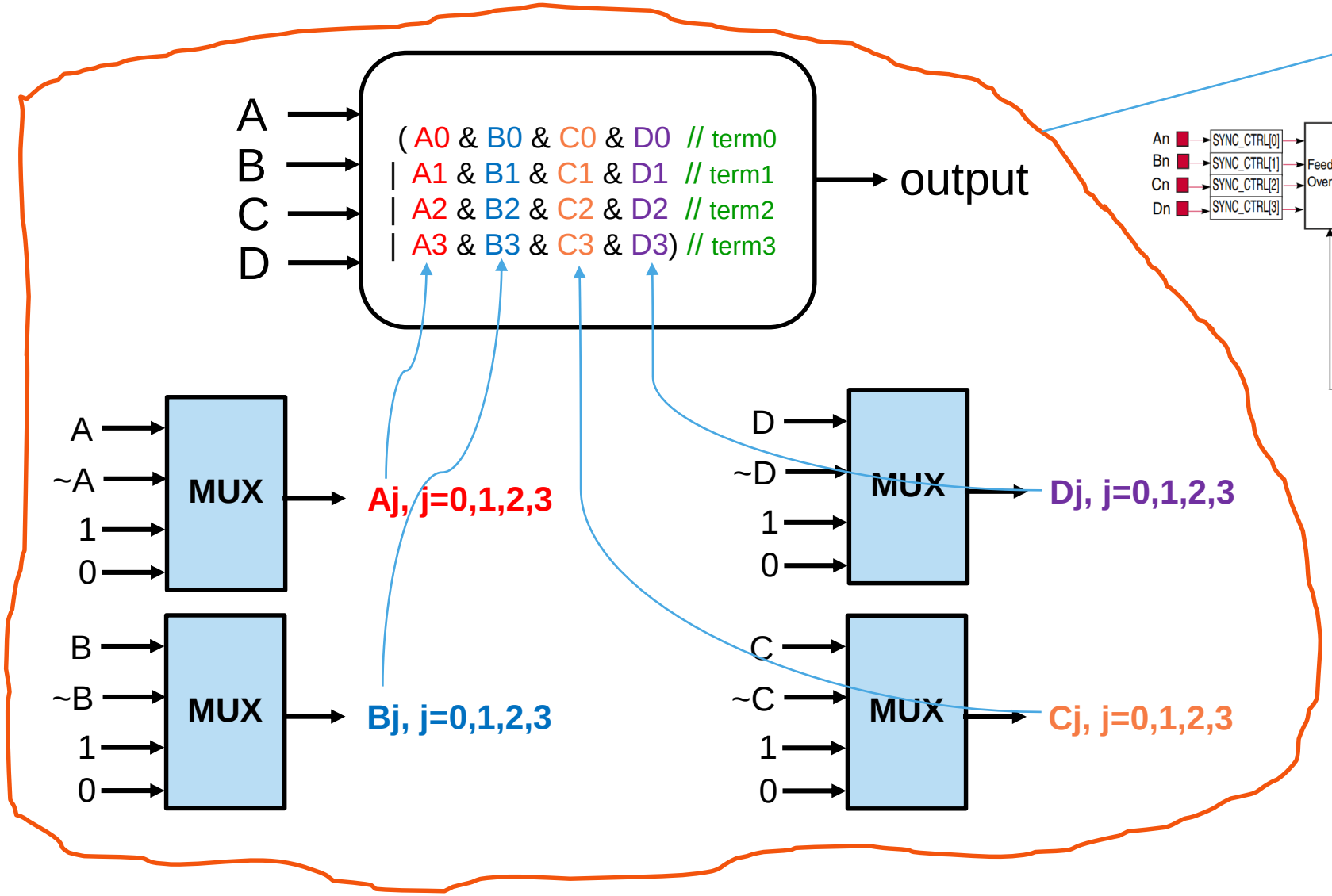
- Handling multiple transfer requests
  - Fixed-priority：
    - ERCA=0, CHPRI=0,1,2,3
    - Unique priority values for each channels is required
    - Preemption, occurs when a channel is performing a transfer while a transfer request is asserted to a channel of a higher priority. One level of preemption is supported
  - Round-robin：
    - ERCA=1
    - channels are cycled through (from high to low channel number) without regard to priority

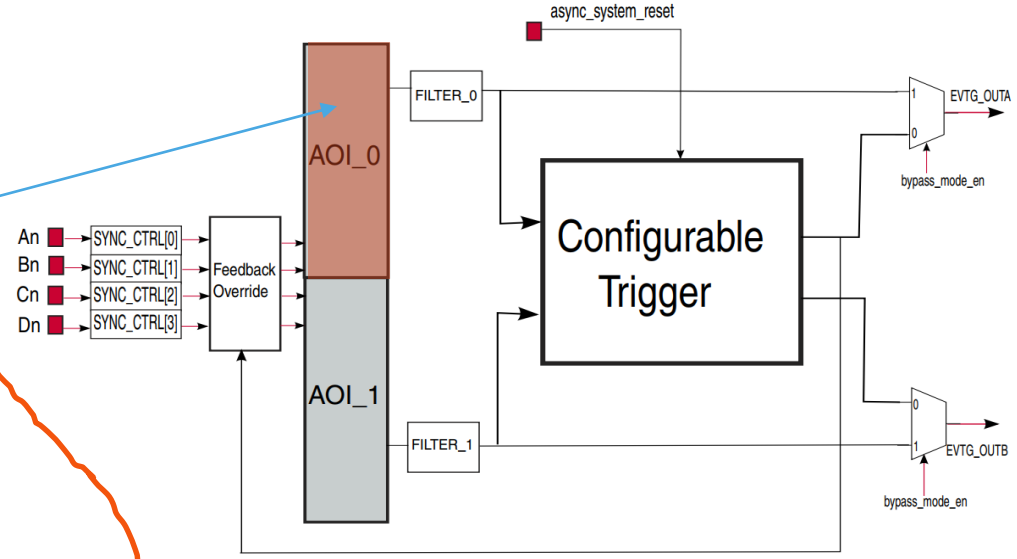


The Event Generator



AND-OR-INVERT (AOI) UNIT



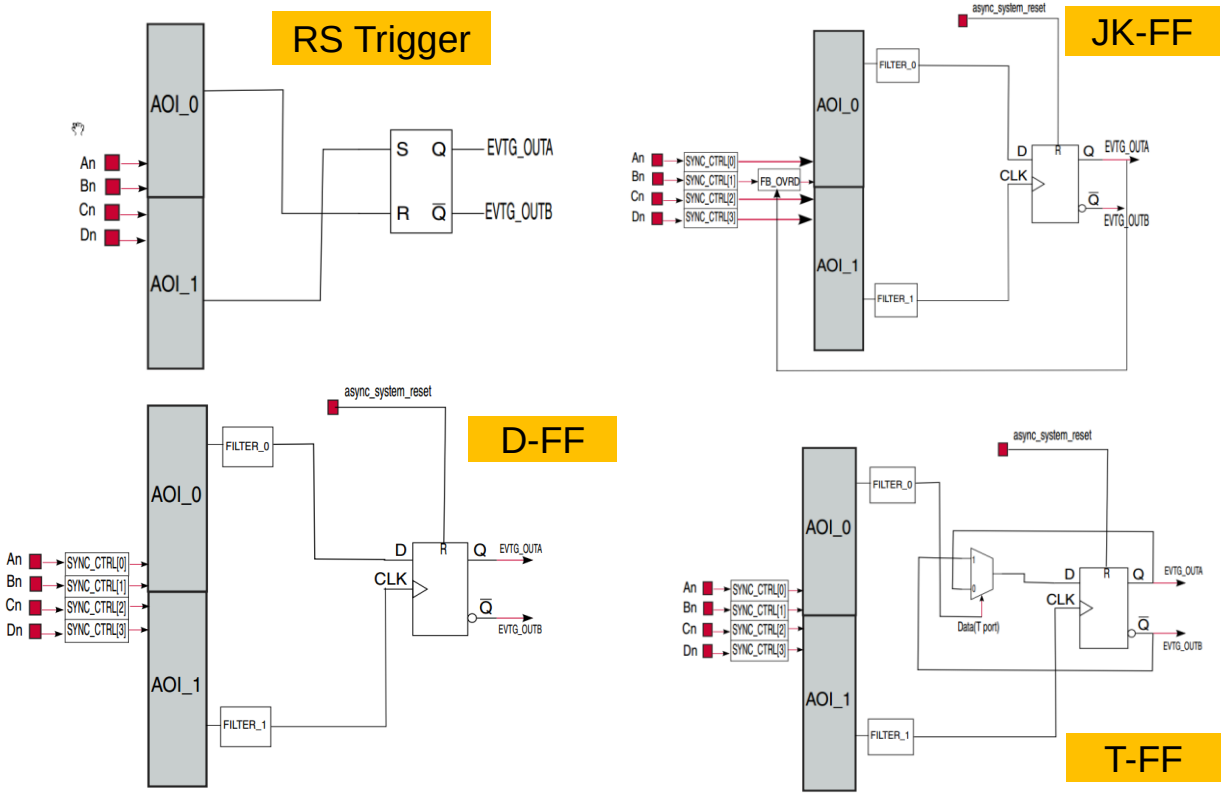


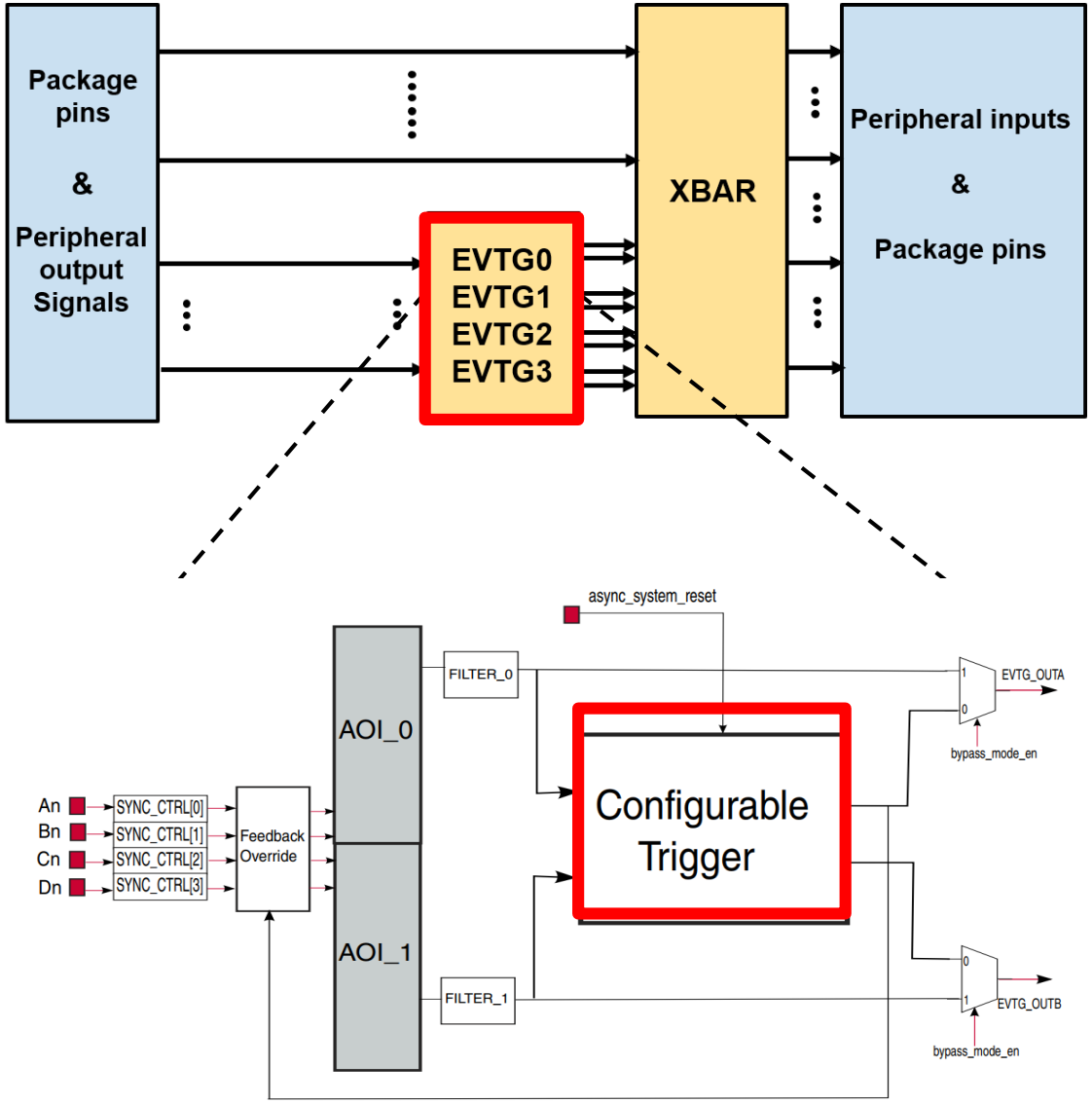
- AOI_1 and AOI_0 share the same four inputs.

EVENT GENERATOR (EVTG) MODULE

Four EVTG modules on MC56F83xxx:

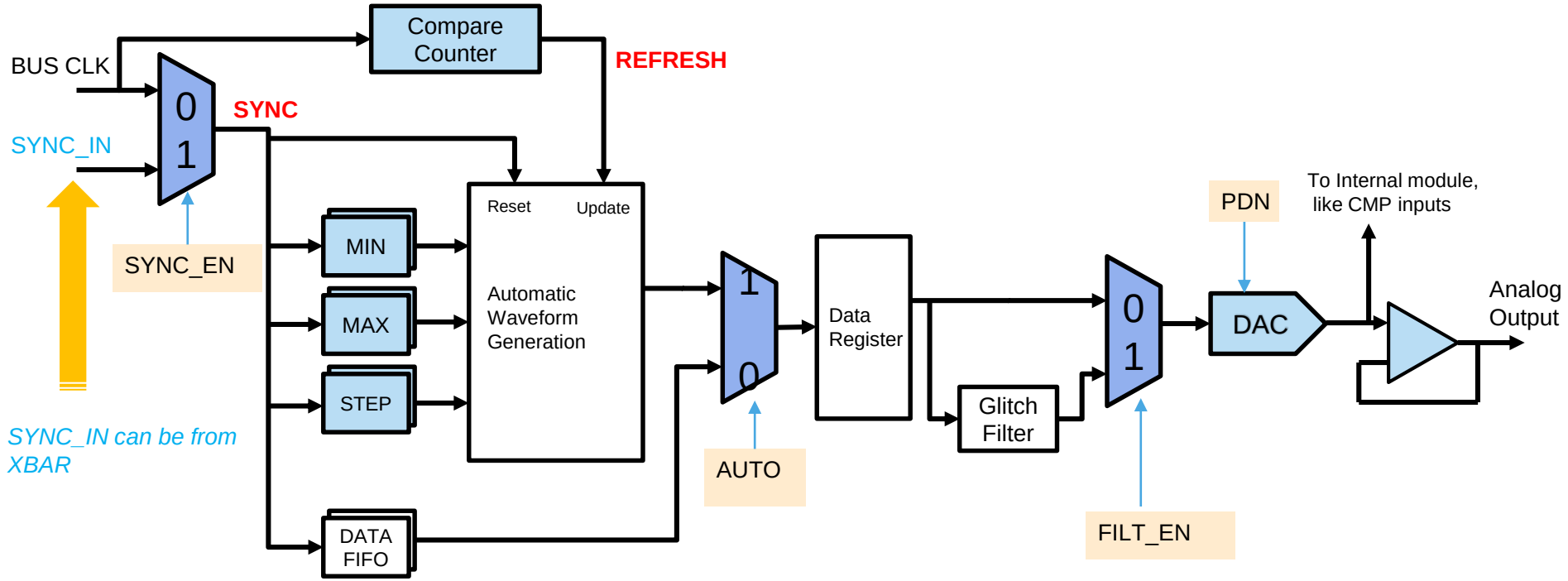
- Each has four input A,B,C and D and two outputs
- Each has two groups of AOI to generate two combinational expressions.
- Each has one flexible flipflop that can be configured as RS, D-FF,T-FF, JK-FF and Latch, etc.





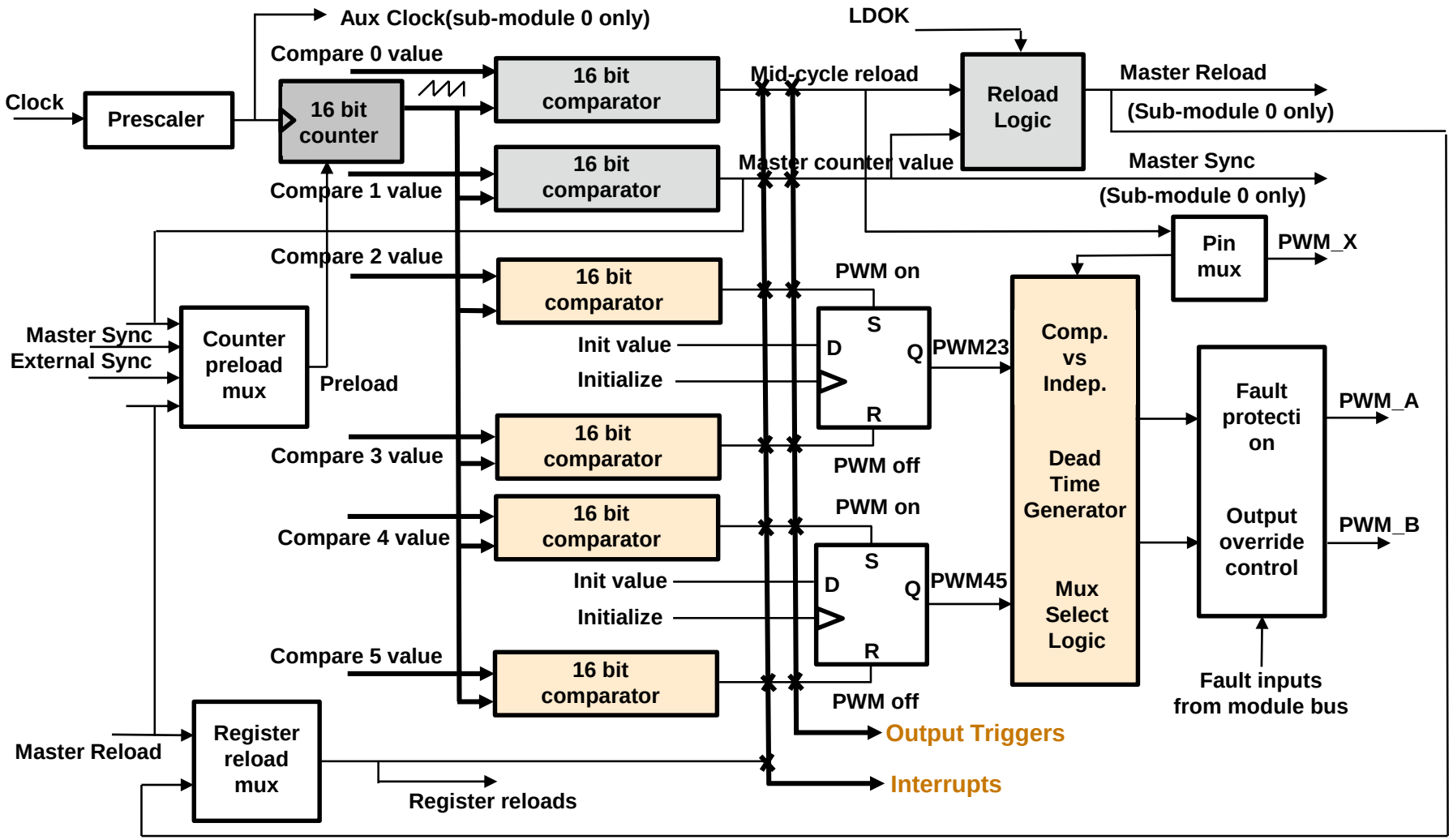
BLOCK DIAGRAM OF 12-BIT DAC

- Automatically square, triangle and sawtooth waveform generation
- Programmable period, update rate and range
- Right justified and left justified format support
- eDMA support with configurable watermark level

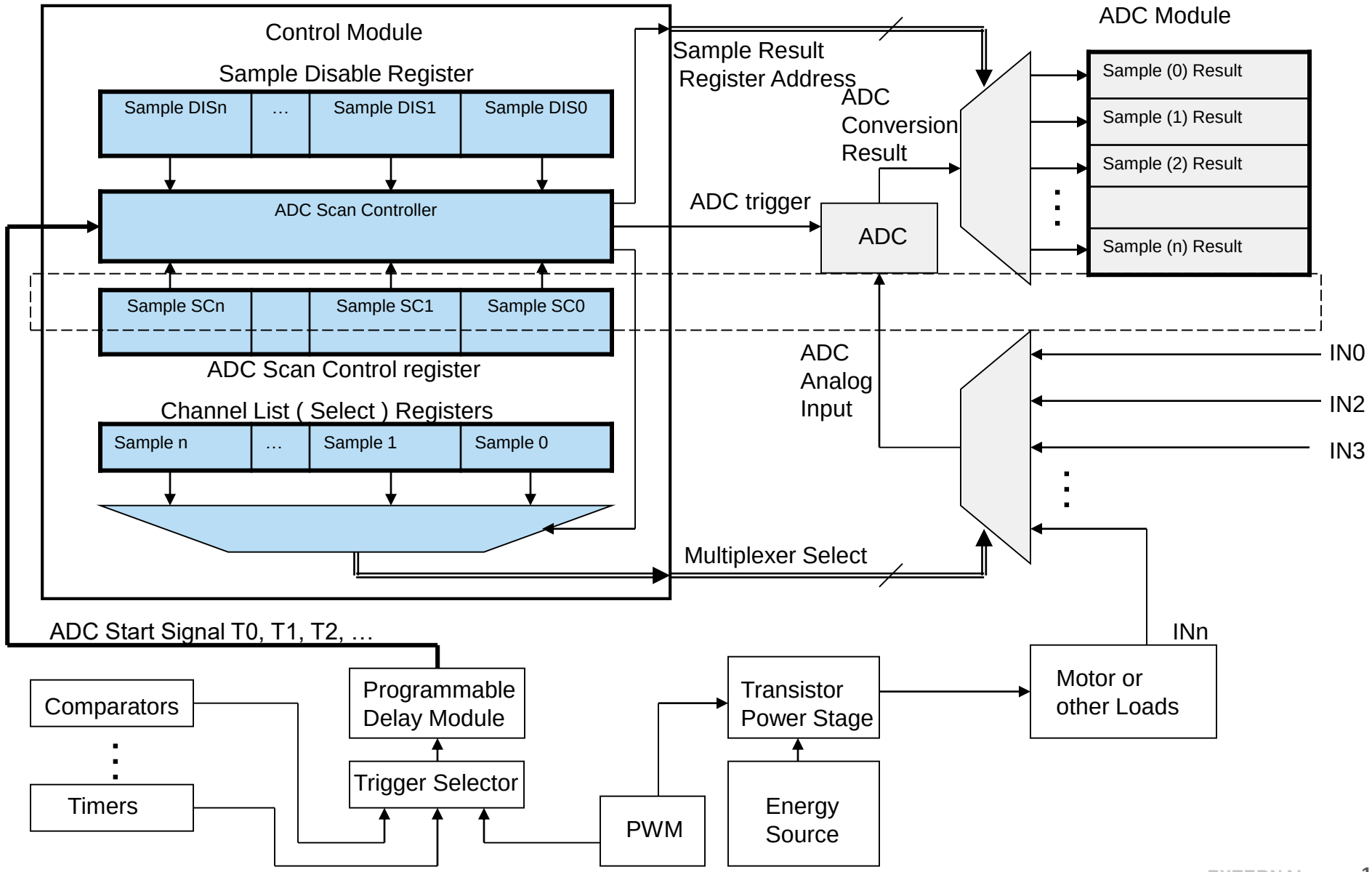


IP Flexibility

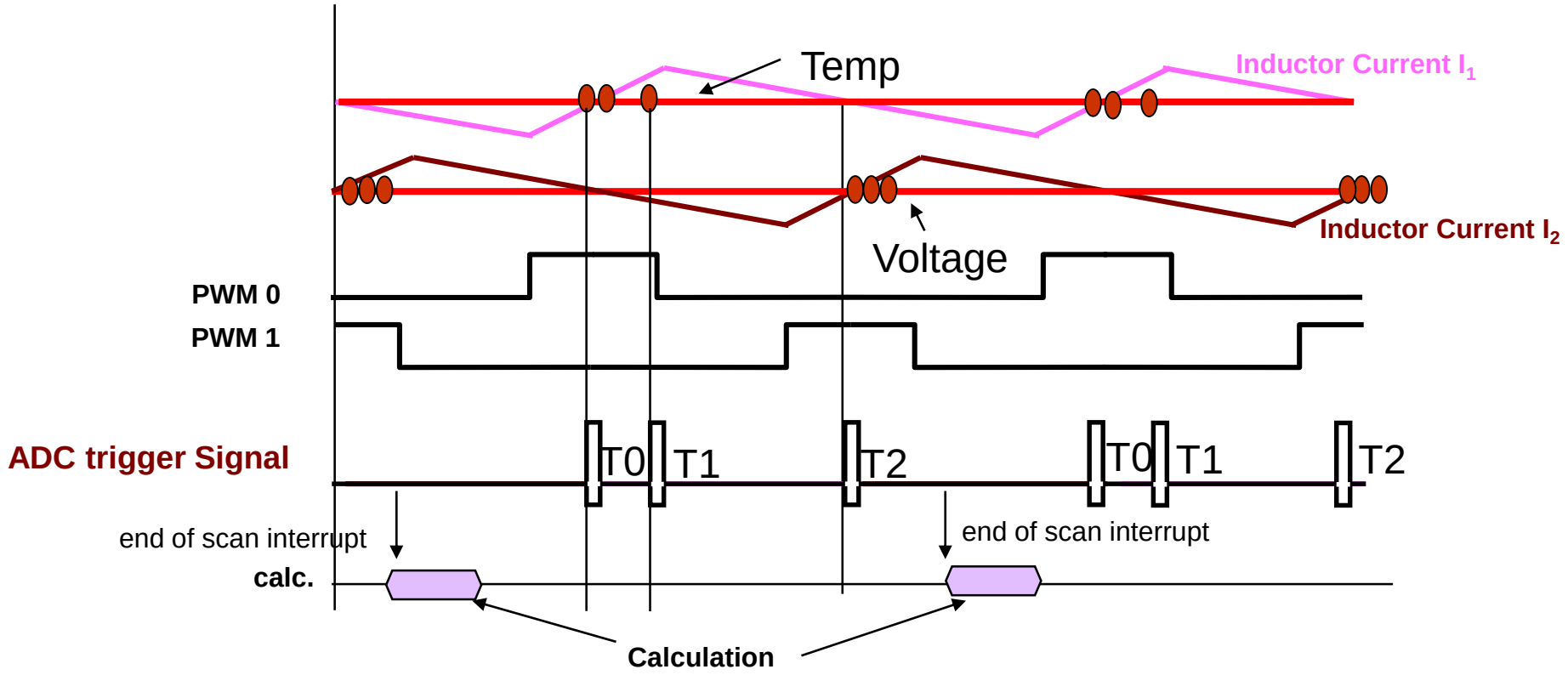
SECURE CONNECTIONS
FOR A SMARTER WORLD


Aux Clock(sub-module 0 only)
LDOK
Compare 0 value
Clock
Prescaler
16 bit counter
16 bit comparator
Mid-cycle reload
Reload Logic
Master Reload
(Sub-module 0 only)
Compare 1 value
16 bit comparator
Master counter value
Master Sync
(Sub-module 0 only)
Pin mux
PWM_X
Compare 2 value
16 bit comparator
PWM on
Master Sync
External Sync
Counter preload mux
Preload
Init value
Initialize
S
D
Q
R
PWM23
Comp. vs Indep.
Dead Time Generator
Mux Select Logic
Fault protecti on
Output override control
PWM_A
PWM_B
Compare 3 value
16 bit comparator
PWM off
Compare 4 value
16 bit comparator
PWM on
Init value
Initialize
PWM45
Compare 5 value
16 bit comparator
PWM off
Fault inputs from module bus
Output Triggers
Interrupts
Master Reload
Register reload mux
Register reloads

ADC IRREGULAR TRIGGERS



Application Example of Irregular Triggers

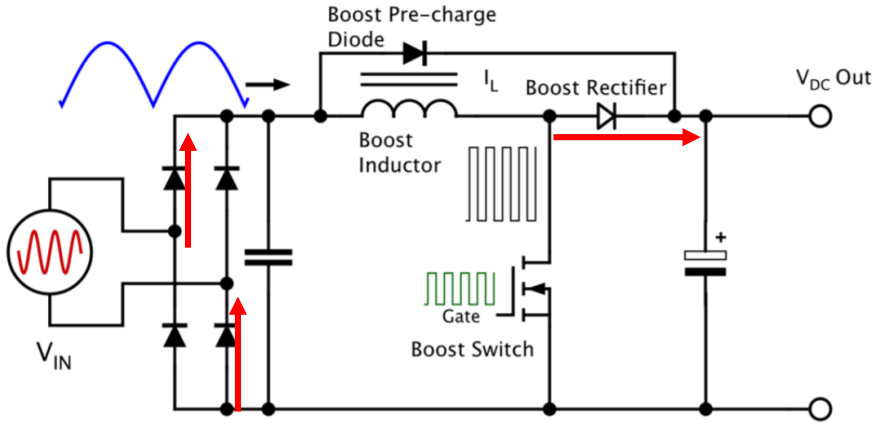


- ✓ Trigger 0 (T0) starts 1st conversion which ADC takes two conversions then wait next trigger
- ✓ Trigger 1 (T1) starts 2nd conversion which ADC takes one conversion then wait next trigger
- ✓ Trigger 2 (T2) starts 3rd conversion which ADC takes three conversions then generates INT

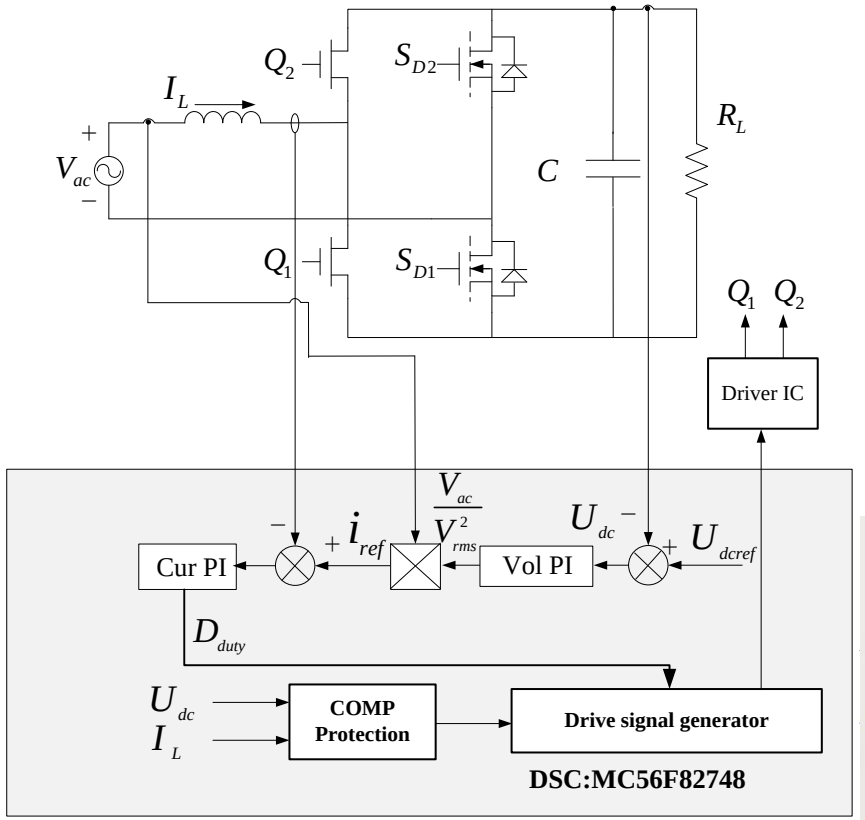
AC/DC Conversions

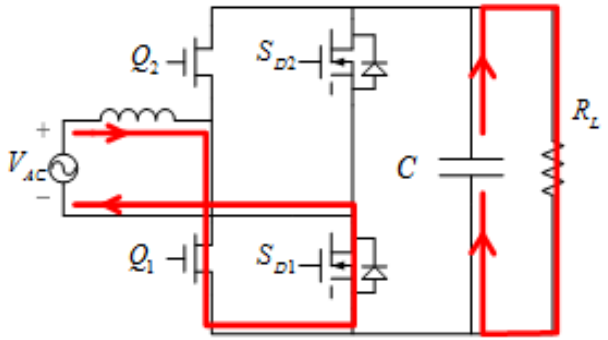
CCM TOTEM-POLE BRIDGELESS PFC

- Boost PFC

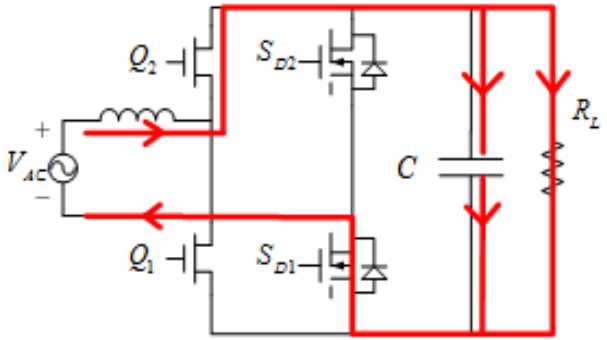


- CCM Totem-pole PFC



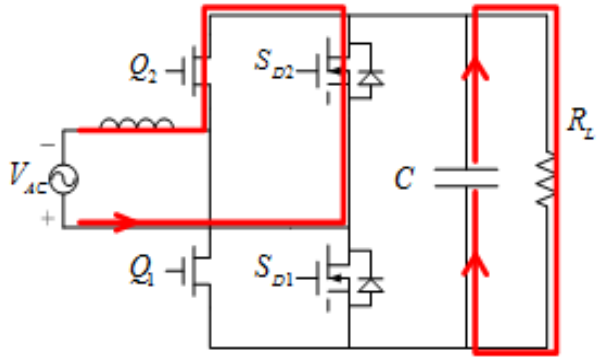


a) Positive cycle charging mode

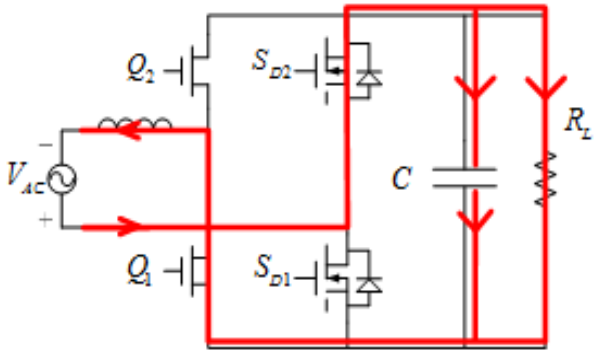


b) Positive cycle after-flow mode

- S_{D1} and S_{D2} are low frequency switches
- Q_1 and Q_2 are active switch and SyncFET



c) Negative cycle charging mode



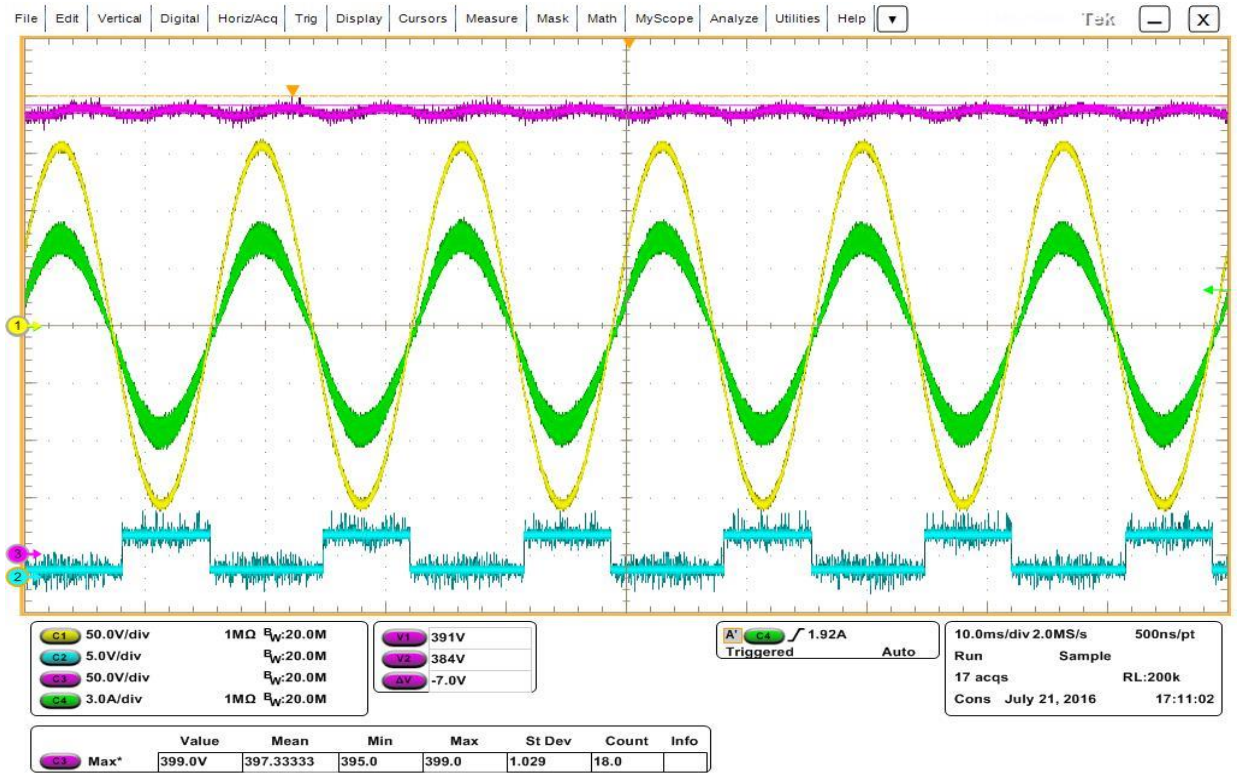
d) Negative cycle after-flow mode

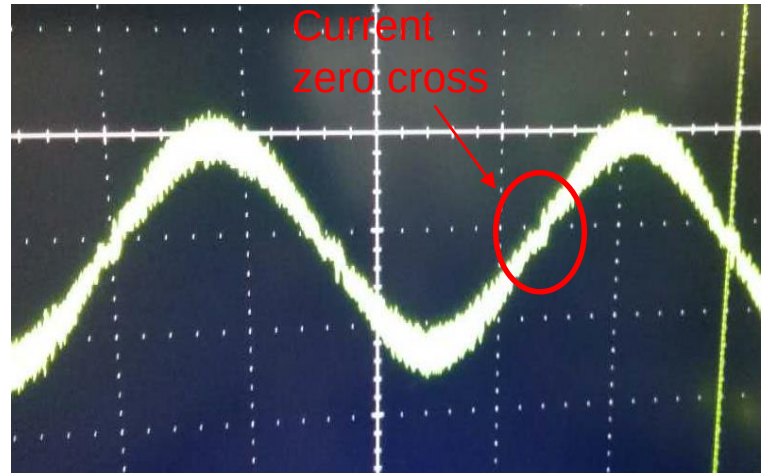
DEVICE COMPARISON OF CONVENTIONAL PFC AND TOTEM-POLE PFC

	Low speed diode	High speed diode	Switch device	Conduction path on/(off)
Conventional PFC	4	1	1	2 low speed diode+ 1switch/(2 low speed diode+1 high speed diode)
Totem-Pole Bridgeless PFC	2(Si MOSFET)	0	2(GaN)	1 Si MOSFET+1 switch(GaN)

Summary of Totem-pole PFC Advantages
1.Fewer semi-conductor devices in all
2.Fewer semi-conductor devices in its conduction path
3.Lower on-resistance

PFC CONVERTER -- STEADY STATE



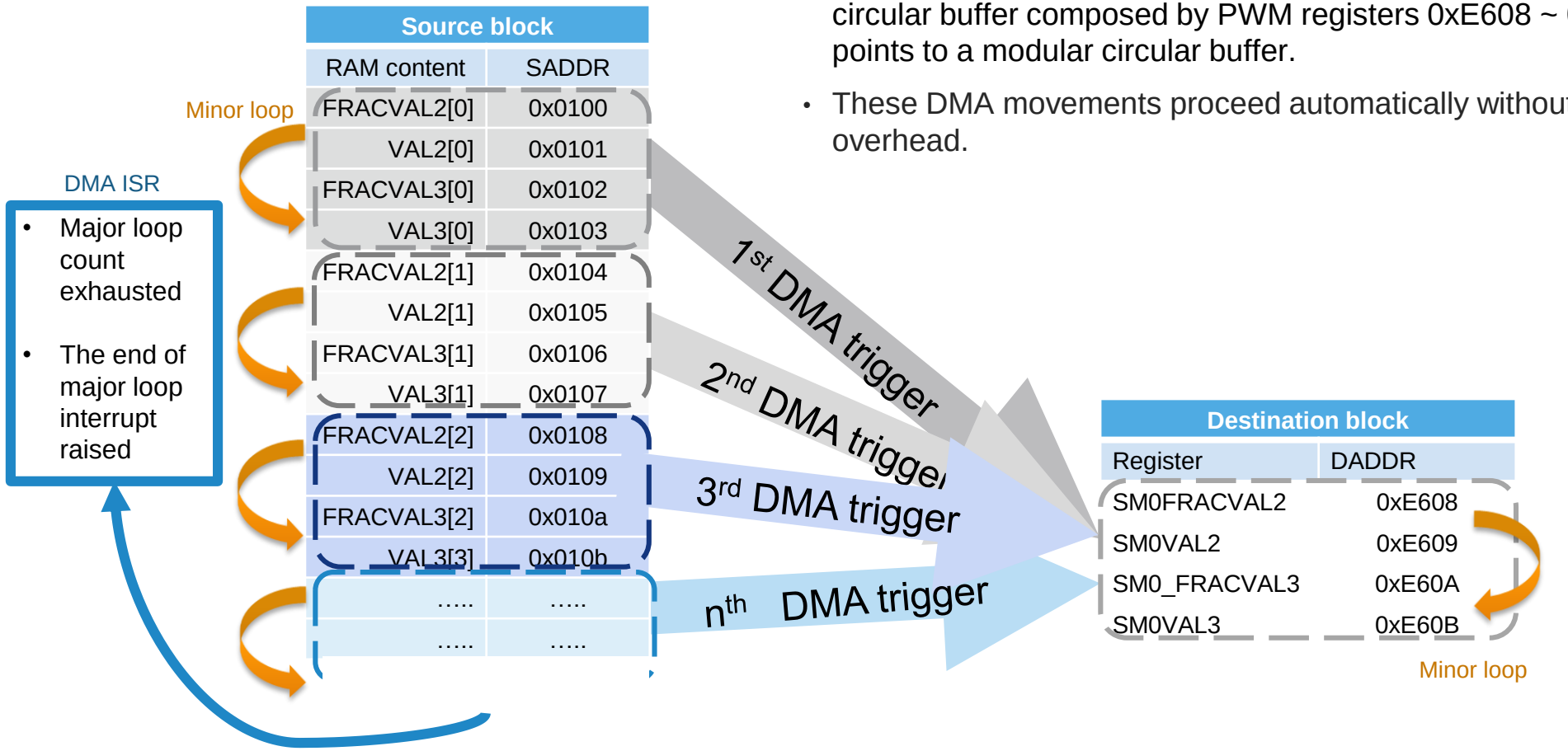


CH1:Input AC voltage;CH2:PWM gate for SD2;

CH3:PFC Output voltage; CH4:Input current

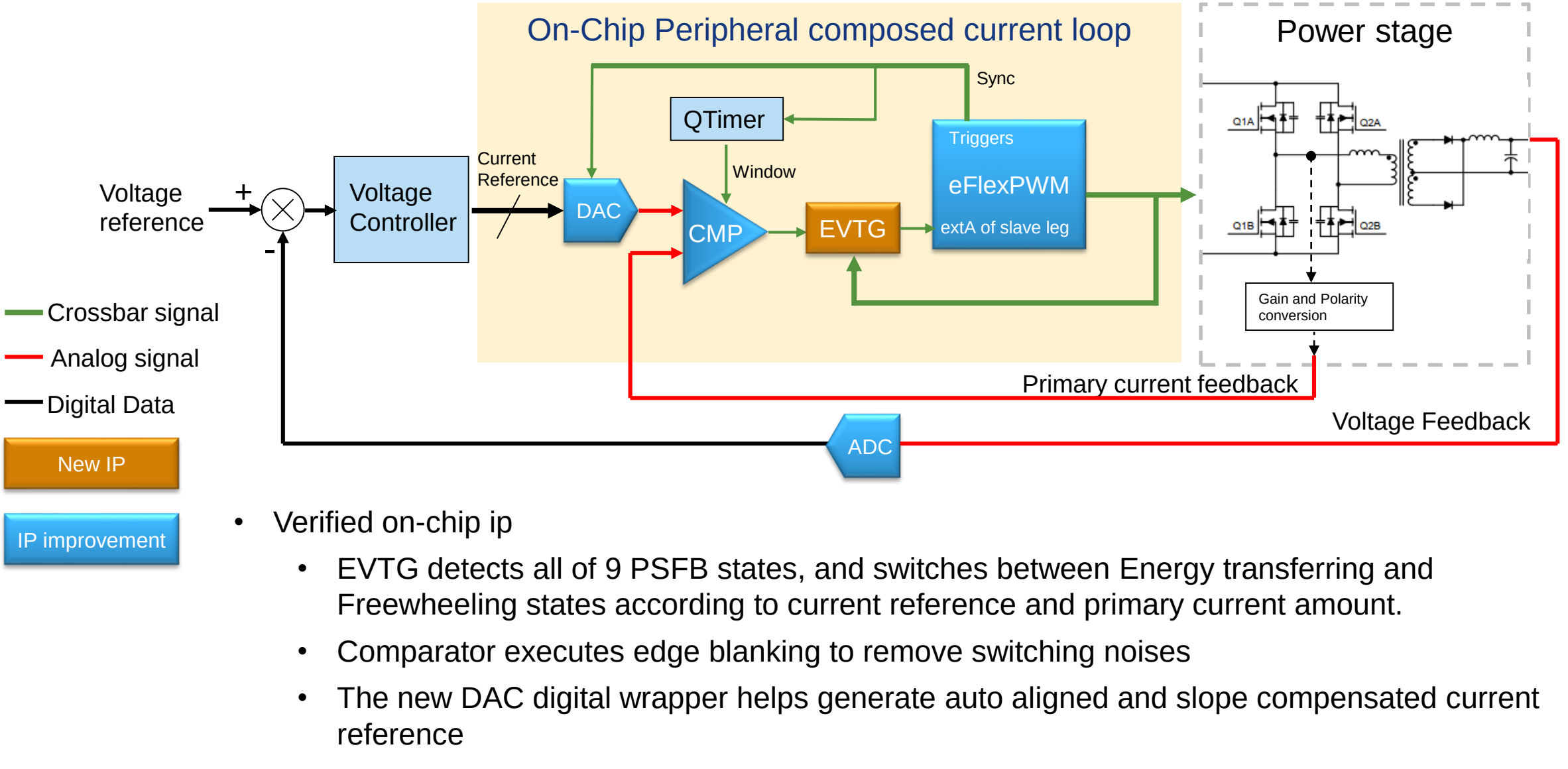
APPLICATION INSTANCE 2: PWM DUTY AUTO UPDATE

- In this application, DMA helps to load 4 continuous eFlexPWM registers in every PWM period. This is useful when PWM frequency is so high that CPU can't fulfill the task of updating duty cycle by cycle. The DADDR points to a circular buffer composed by PWM registers 0xE608 ~ 0xE60B. The SADDR points to a modular circular buffer.
- These DMA movements proceed automatically without any software overhead.



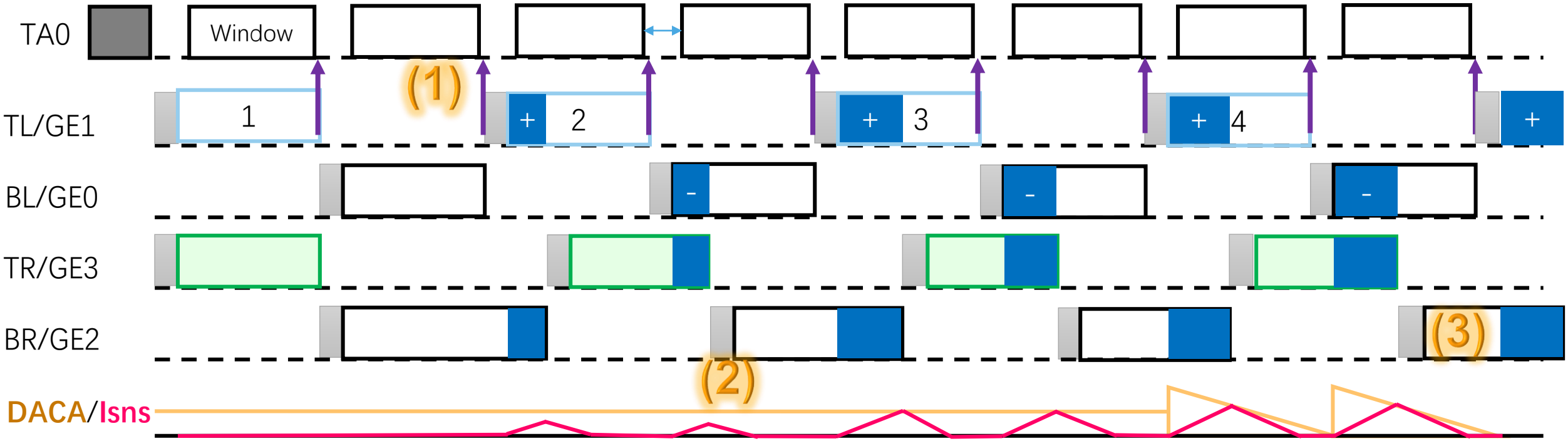
DC/DC Convertors

PEAK CURRENT CONTROL MODE PSFB

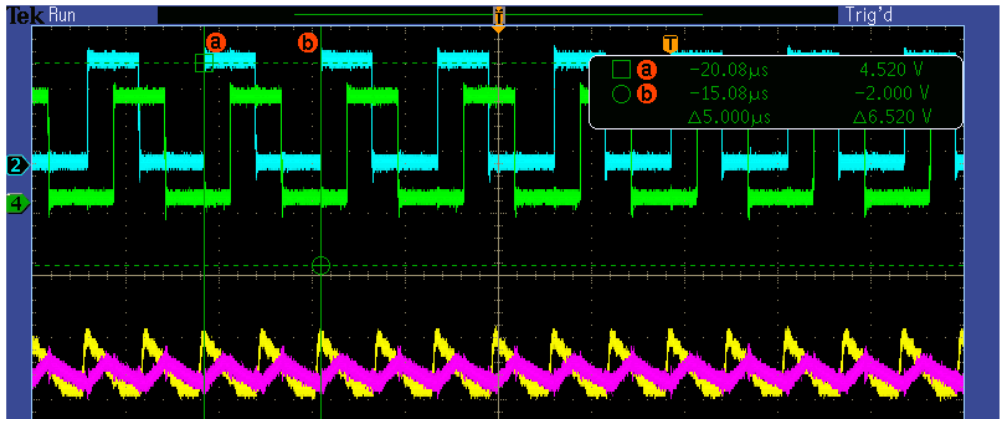


- Verified on-chip ip
  - EVTG detects all of 9 PSFB states, and switches between Energy transferring and Freewheeling states according to current reference and primary current amount.
  - Comparator executes edge blanking to remove switching noises
  - The new DAC digital wrapper helps generate auto aligned and slope compensated current reference

PEAK CURRENT CONTROL MODE PSFB, CONT.



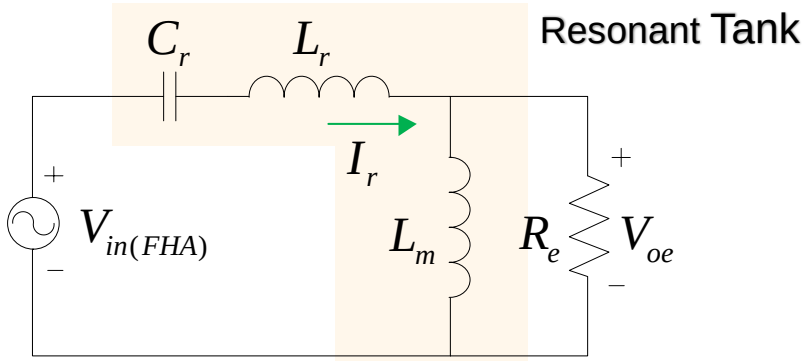
1. Programmable Edge-blanking location and width
2. End of transfer period force switching
3. PSFB state lock after energy transfer stage



PFM (Pulse Frequency Modulation)

Complementary pulse signals with 50% duty cycle drive the upper and lower arm switch and regulate the output voltage/current by adjusting the switching frequency.

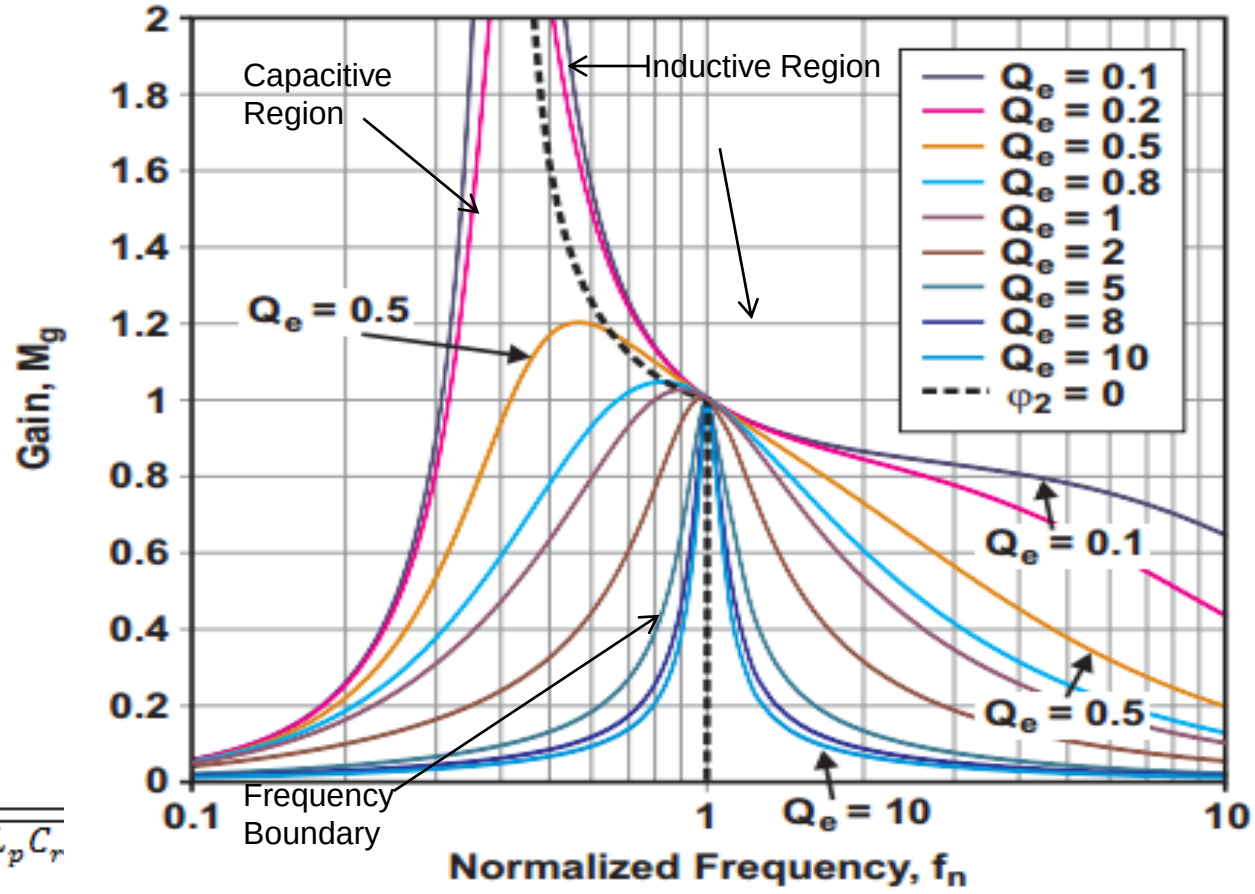
first harmonic approximation



Equivalent circuit of LLC resonant converter

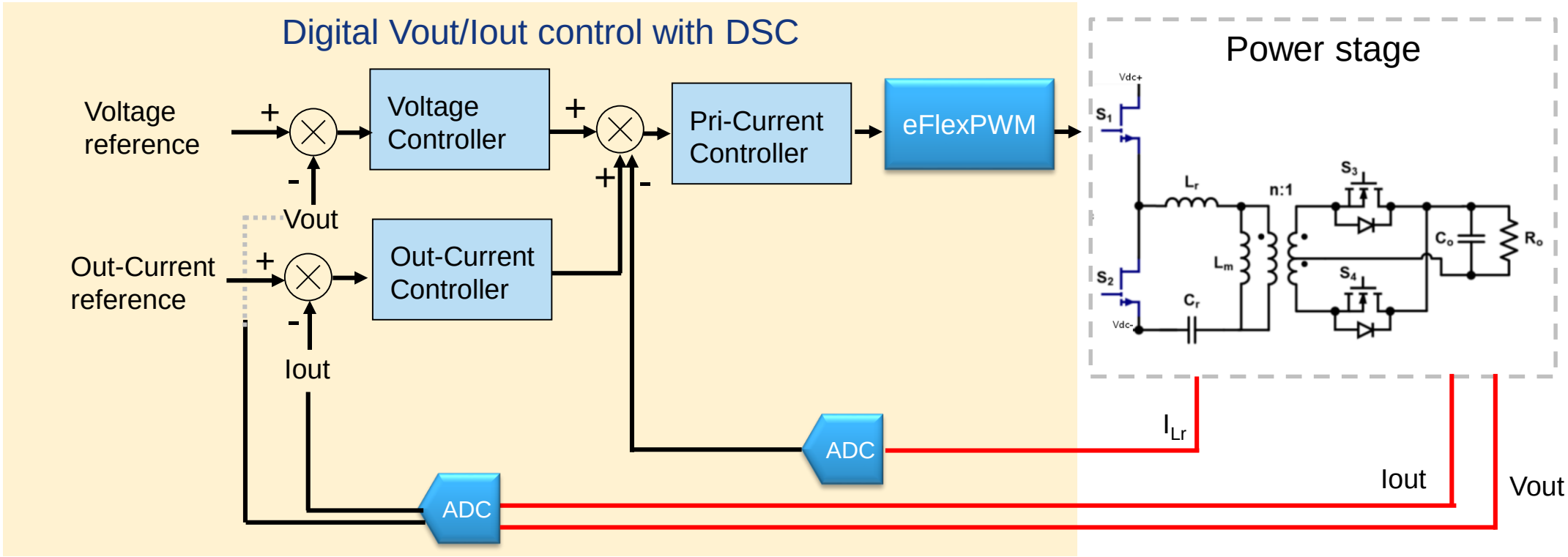
$$M_{PFM} = \frac{2nV_0}{V_{DC}} = \left| \frac{mf_n^2}{[(m+1)f_n^2 - 1] + jQ_e mf_n(f_n^2 - 1)} \right|$$

$$Q_e = \frac{1}{R_e}\sqrt{\frac{L_r}{C_r}}, m = \frac{L_p}{L_r}, f_n = \frac{f_{sw}}{f_0}, f_0 = \frac{1}{2\pi\sqrt{L_r C_r}}, f_p = \frac{1}{2\pi\sqrt{L_p C_r}}$$



The variation range of M is narrow when fn>1.

HALF BRIDGE LLC CONVERTER

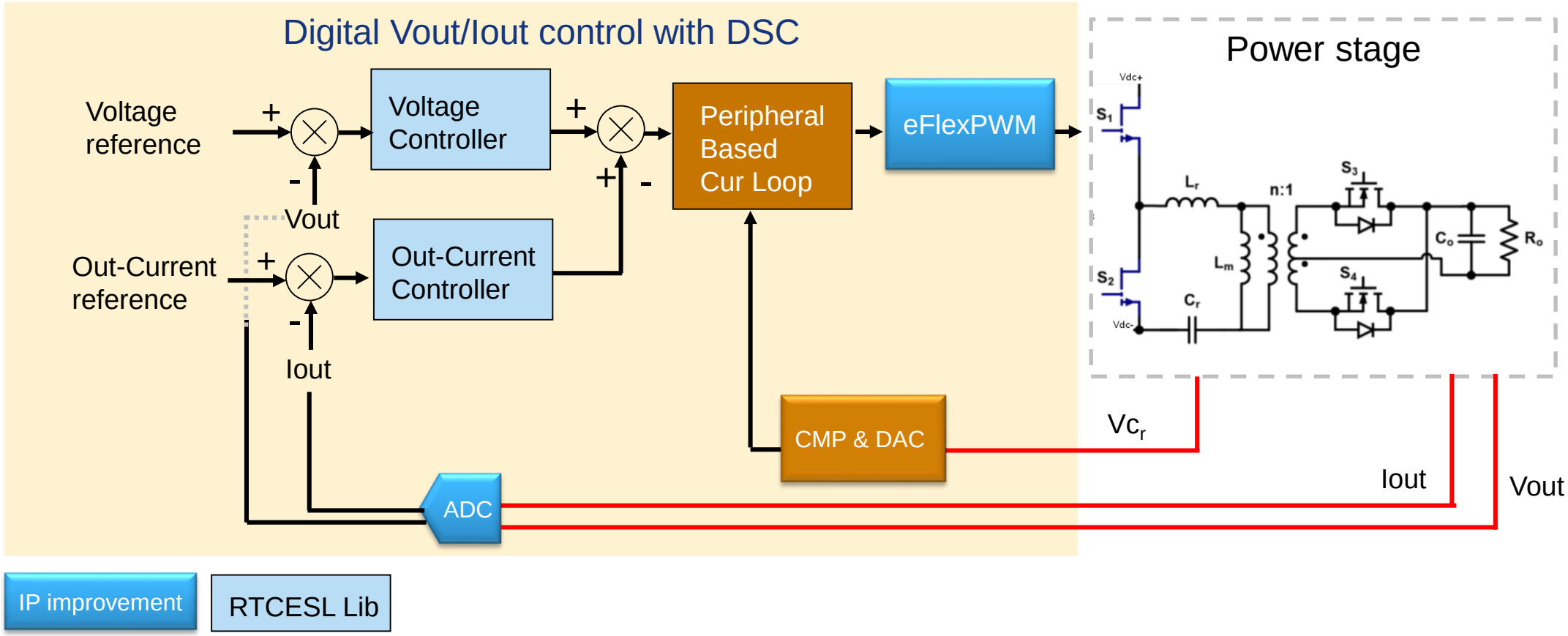


IP improvement

RTCESL Lib

- **Voltage single loop: Constant output voltage control with single loop;**
- **CCM/CVM outer loops: concurrent output voltage or current control with primary current inner loop**
- **Support 50% HB PWM duty lock, IP level PFM range limitation for charge control mode**

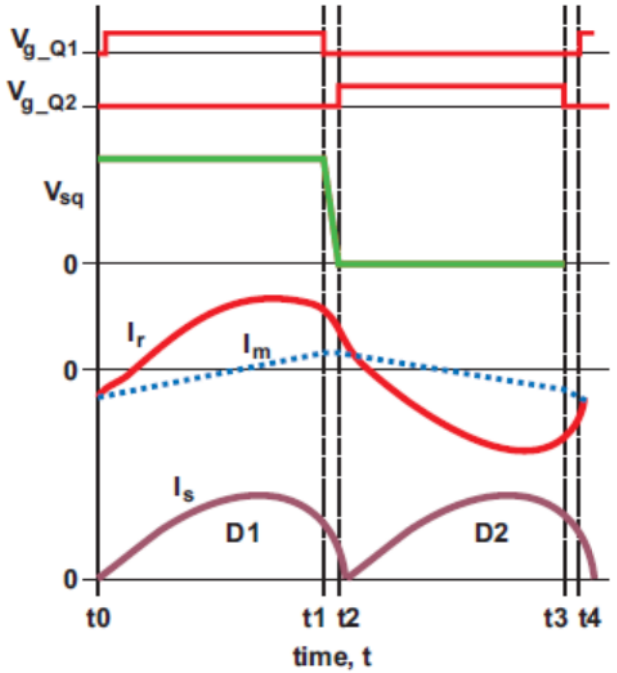
HHC MODE LLC CONVERTER,



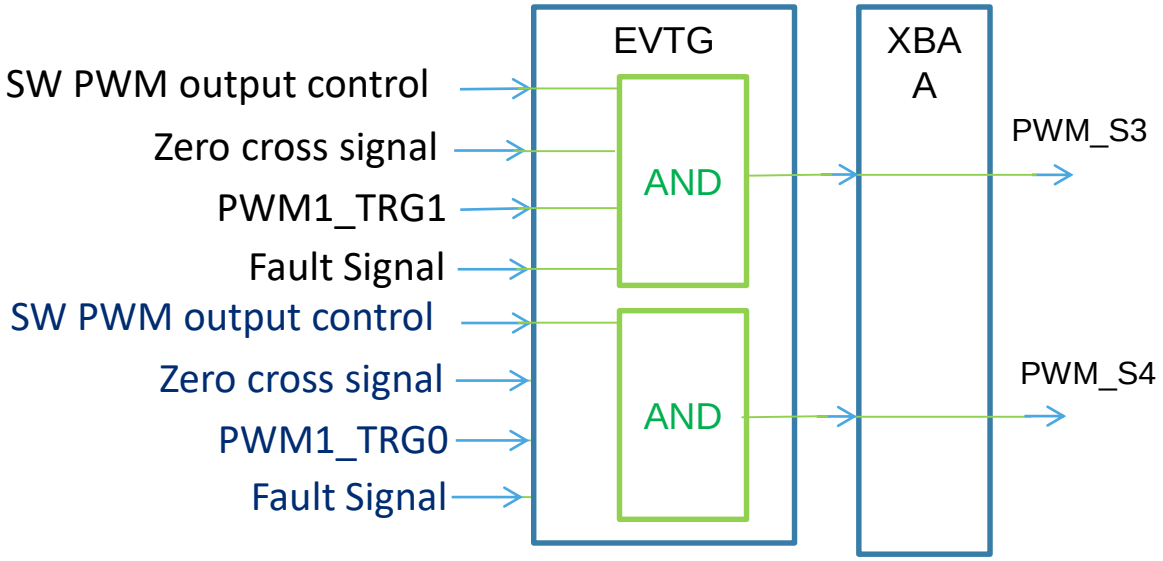
- **Support 50% HB PWM duty lock, IP level PFM range limitation for charge control mode**

SYNCHRONOUS RECTIFICATION DRIVE SIGNAL

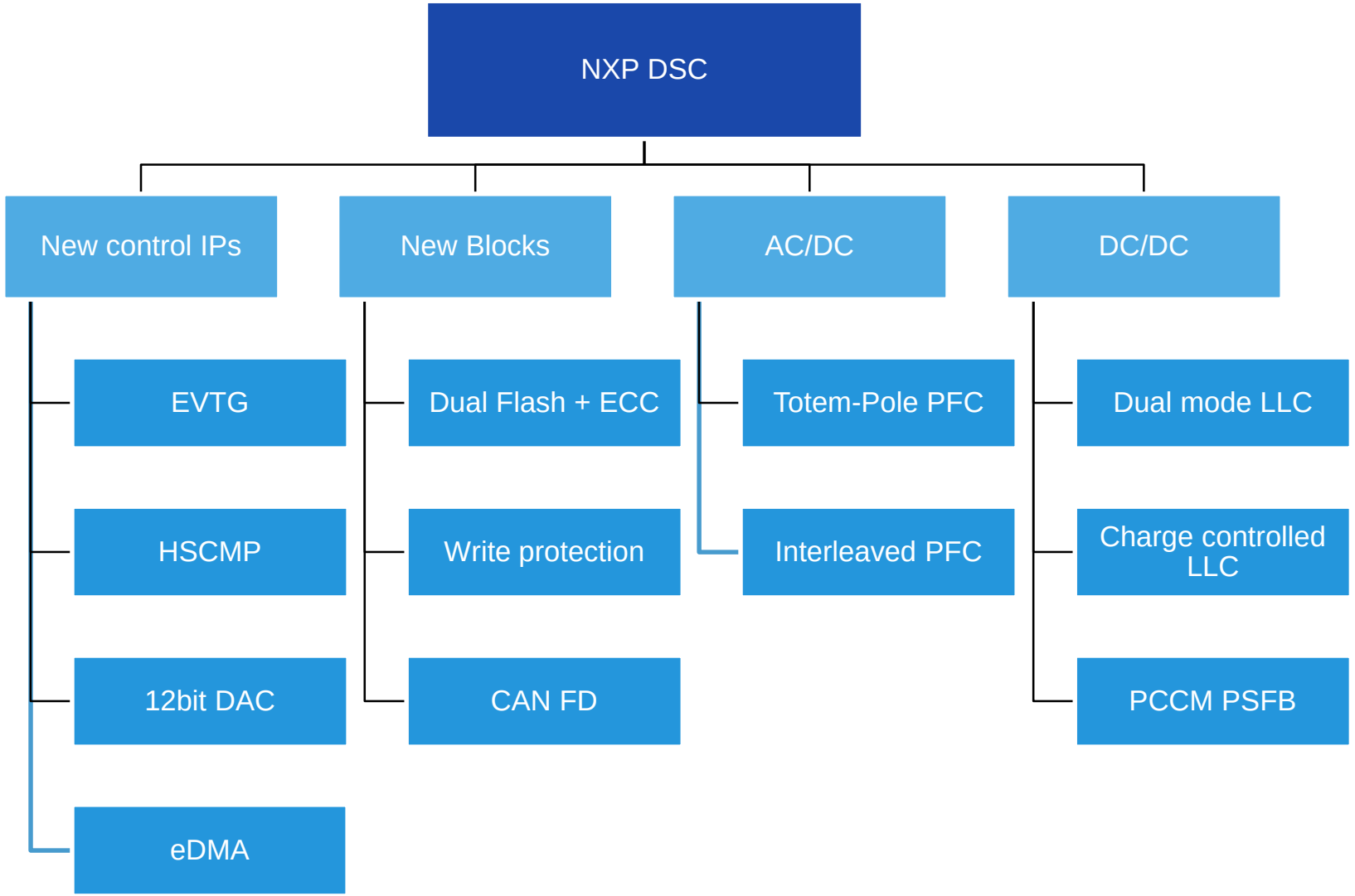
$$f_{sw} > f_0$$

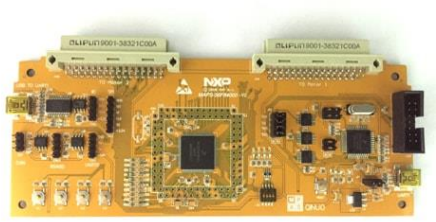


synchronous rectification MOSFET driver =
PWM1 output & zero cross signal & Fault signal



SUMMARY


NXP DSC
New control IPs
New Blocks
AC/DC
DC/DC
EVTG
HSCMP
12bit DAC
eDMA
Dual Flash + ECC
Write protection
CAN FD
Totem-Pole PFC
Interleaved PFC
Dual mode LLC
Charge controlled LLC
PCCM PSFB



REFERENCES

- Product page
  - https://www.nxp.com/DSC
- Developer's Resources (IDE, Libraries, EVK, Reference design)
  - https://www.nxp.com/design/dsc-developer-resources:DSC-DEVELOPER
- LLC Resonant Converter with Sync Rectifier
  - https://www.nxp.com/design/designs/llc-resonant-converter-with-sync-rectifier:RDLLC56F82748
- Totem-Pole Bridge less PFC
  - https://www.nxp.com/design/designs/totem-pole-bridgeless-pfc-converter:RDPFC56F82748
- High-Voltage Development platform
  - https://www.nxp.com/products/processors-and-microcontrollers/arm-microcontrollers/general-purpose-mcus/kv-series-cortex-m4-m0-plus-m7/high-voltage-development-platform:HVP-MC3PH

ONLINE SUPPORT THROUGH TIC

What is TIC?

-Online support, comprised of specialized engineers and communities, designed to answer NXP customers‘ questions
-Serves all customers using web and chat
-Has team of 50+ engineers doing only support
-Specialists, not generalists

Scope of Support?

-Remote, focus on mass market products, not all products
-Engineers work based on written questions
-English and Chinese are standard languages

Covered Product Families		Support through		Language support	
		Ticket System	Communities	English	Chinese
MPU	i.MX	x	x	x	x
	Digital Networking	x	x	x	
MCU	i.MXRT, Kinetis & FSL Legacy MCU, LPC	x	x	x	x
	Auto 32bit MPC5xxx	x	x	x	
	Auto 16bit (S12)	x	x	x	
	Auto 32bit S32K	x	x	x	x
Misc	Analog & Sensors	x	(x)	x	x
	RF (Power & Small Signal)	x		x	
	NFC (Readers, NTAG, MIFARE)	x	x	x	x
	SIP (Interfaces, Connectivity)	x		x	x
	Security and Authentication (Mass market)	x		x	x

How to reach the TIC?

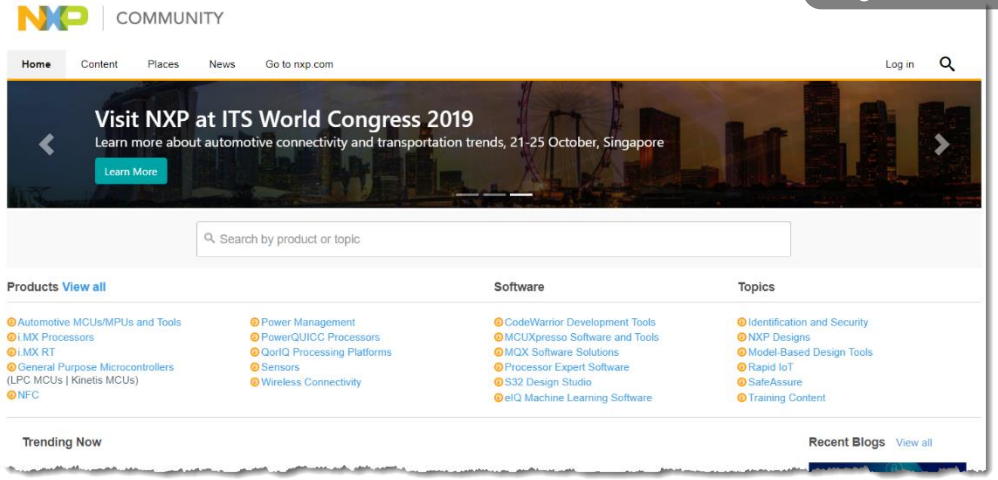
1. **Login to the Online Ticket System** (www.nxp.com/support)

For: Technical Questions
When: can´t be shared publicly
Login: Need

For: Technical Questions
When: non-confidential technical issues
Login: Need

For: Generic non-technical questions
Login: No Need

2. **NXP Community System** (https://community.nxp.com)
✓ **Login: Need**



3. **External NXP Community System** (恩智浦中文社区 http://www.nxpic.org/)
✓ **Login: Need**
✓ **Only support Chinese**
✓ **Support product range: i.MX MPU & i.MX RT & LPC & Kinetis**

SECURE CONNECTIONS
FOR A SMARTER WORLD