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An FM/IF system for DECT and other high-speed GFSK applications

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Info	Content
Keywords	High-speed digital wireless PCS applications, Digital European Cordless Telephone (DECT), FM/IF system
Abstract	An NXP low-voltage high-performance monolithic FM/IF system, the SA639 is introduced to meet the increasing demand for high-speed digital wireless PCS applications. In order to assist the system design, a SA639-based performance evaluation board has been developed according to the Digital European Cordless Telephone (DECT) specifications. This application note presents detailed descriptions of the SA639 FM/IF system, evaluation board, and design information including circuit diagram, component list, and the board layout. The experimental performance evaluation procedures, measured bit error rate (BER), sensitivity to frequency offset, and sensitivity to FM deviation variation of this system are also presented. Results indicate that the low-voltage SA639 FM/IF system provides superior performance for high-speed digital wireless applications.

Revision history

Rev	Date	Description
3.0	20140724	Application note; third release • The format of this application note has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.
2.0	20040114	Application note; second release
1.0	19970820	Application note; initial release

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1. Introduction

To achieve the goal of wireless personal communications, allowing users access to the capabilities of the global communications network at any time without regard to location and mobility, cellular and cordless telephony have been taken as two major approaches. Cellular systems are evolving towards smaller cells (micro cells) and lower power levels to provide higher overall capacity. Cordless telephones have evolved from home appliances towards widespread ‘universal’ low-power personal communications systems. With the advent of digital cordless telephony, cordless systems with enhanced functionality have been developed that can support higher data rates and more sophisticated applications such as wireless private branch exchanges (WPBX) and public-access Telepoint systems. One of the first digital cordless standards is the Digital European Cordless Telecommunications (DECT) system, a pan-European standard designed to connect all of Europe with a common digital cordless system. DECT is also a flexible standard for providing a wide range of services in small cells.

In this application note, the SA639, an NXP low-voltage FM/IF system with several important features such as post filter amplifier and active data switch, is proposed for DECT and other high-speed digital wireless applications. A SA639-based DECT receiver evaluation board has been developed. Detailed description of the SA639 FM/IF system, structure of the evaluation board, design information, and experimental evaluation results are presented.

2. Review of DECT standard

DECT is designed as a flexible interface to provide cost-effective communications services to high user densities in small cells. This standard is intended for the applications such as domestic cordless telephony, Telepoint, cordless PBXs, and Radio Local Loop (RLL). It supports multiple bearer channels for speech and data transmission (which can be set up and released during a call), hand over, location registration, and paging. Functionally, DECT is closer to a cellular system than to a classical cordless telephone. However, the interface to PSTN or ISDN remains the same as for a PBX or corded telephone. Table 1 is a summary of the key specifications of DECT and other digital cordless telephone systems.

DECT is based on Time Division Duplex (TDD) and Time Division Multiple Access (TDMA) with 10 carriers in the 1880 MHz to 1900 MHz band. Figure 1 illustrates the DECT TDD/TDMA frame structure.

The completed frame is 10 ms in duration with 24 time slots. The first 12 slots are allocated for the transmission from base station to handsets, and the other 12 slots are for the transmission from handsets to base station. Each slot is 417 µs long with 480 bits. The first 32 bits is a ‘1010...’ sequence for synchronization. The 32 kbit/s ADPCM CODEC is used for speech coding in DECT, which provides 320 bits during each 10 ms frame. When a call is made, two slots (one is in the first 12 slots, the other is in the last 12 slots) are assigned to the user for transmit and receive.

Table 1. Summary of digital cordless standards

Standard	CT2/CT2+	DECT	PHS	PACS
Region	Europe/Canada	Europe	Japan	USA
Frequency band (MHz)	CT2: 864 - 868 CT2+: 944 - 948	1880 - 1900	1895 - 1918	Tx: 1850 - 1910 Rx: 1930 - 1990
Duplex	TDD	TDD	TDD	FDD
Multiple access	TDMA	TDMA	TDMA	TDMA
Number of channels	40	10	77	16 pairs
Channel spacing (kHz)	100	1728	300	300
Users/channel	1	12	4	8/pair
Modulation	GFSK (FM dev: 14 kHz to 25 kHz)	GFSK (FM dev: 288 kHz)	π/4-DQPSK	π/4-DQPSK
Bit rate	72 kbit/s	1.152 Mbit/s	32 kbit/s ADPCM	32 kbit/s ADPCM
Speech coding	32 kbit/s ADPCM	32 kbit/s ADPCM	32 kbit/s ADPCM	32 kbit/s ADPCM
Frame duration	2 ms	10 ms	5 ms	2.5 ms
Peak power	10 mW	250 mW	80 mW	200 mW

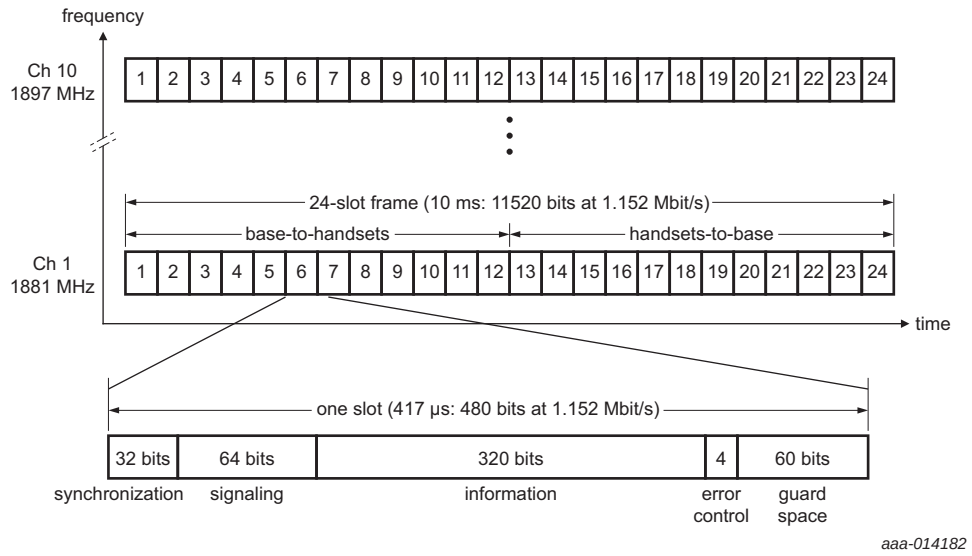


Fig 1. DECT TDD/TDMA frame structure

Gaussian filtered FSK (GFSK) modulation scheme is employed in DECT. GFSK is a premodulation Gaussian filtered digital FM scheme. Figure 2 shows the block diagram of a GFSK modulator. The advantages of GFSK can be summarized as follows:

Constant envelope nature — This allows GFSK modulated signal to be operated with class-C power amplifier without introducing spectrum regeneration. Therefore, lower power consumption and higher power efficiency can be achieved.

Narrow power spectrum — Narrow main lobe and low spectral tails keep the adjacent channel interference to low levels and achieve higher spectral efficiency.

Non-coherent detection — GFSK modulated signal can be demodulated by the limiter/discriminator receiver as shown in Figure 3. This simple structure leads to low-cost GFSK receivers.

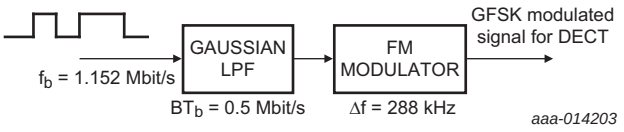


Fig 2. Block diagram of GFSK modulator

Fig 3. Block diagram of GFSK demodulator

3. The SA639 FM/IF system

The SA639 is a low-voltage high performance monolithic FM/IF system with high-speed RSSI incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, fast RSSI op amps, post detection filter amplifier, and a data switch. The block diagram of SA639 is presented in Figure 4. The SA639 was designed specially for high data rate portable communications applications and functions down to 2.7 V. The data output provides a minimum bandwidth of 1 MHz to demodulate high-speed data, such as in DECT applications. Figure 5 presents the quad tank S-curve of SA639, which indicates the linear range to be about 2 MHz. The measured RSSI characteristic of SA639 is presented in Figure 6. With more than 75 dB dynamic range, the SA639 RSSI rise/fall time is 0.8/2.0 ms at −45 dBm RF level.

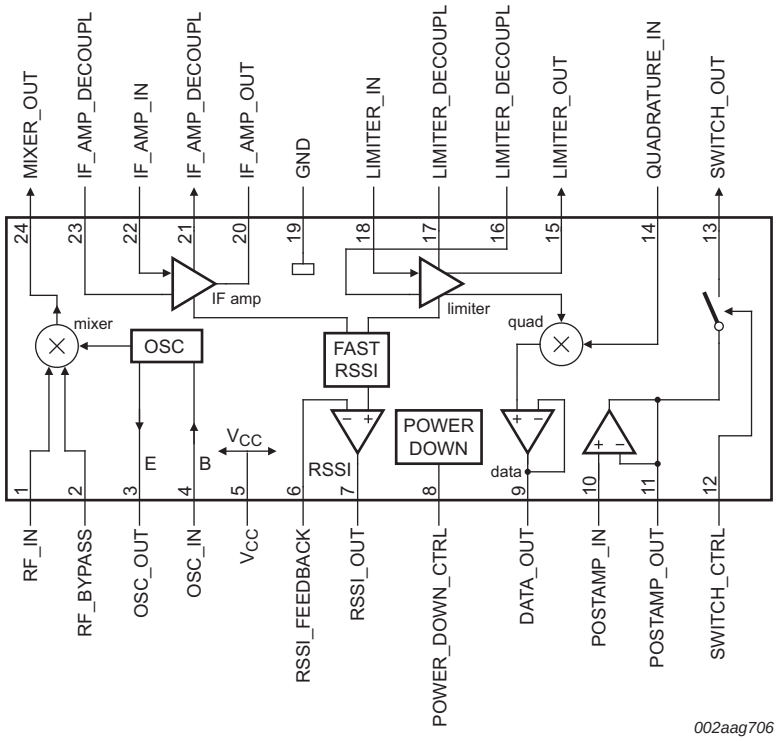


Fig 4. Block diagram of the SA639 FM/IF system

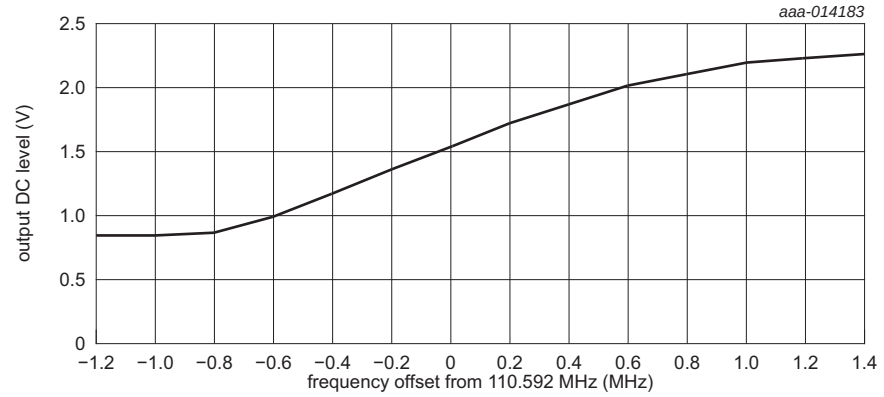


Fig 5. Quad tank S-curve of SA639 board

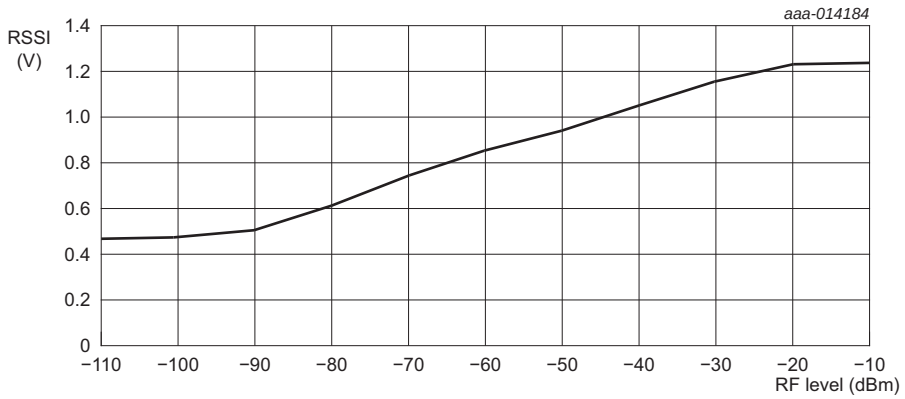


Fig 6. Measured RSSI characteristics of SA639

The post-detection amplifier may be used to realize a group delay optimized low-pass filter. To keep its frequency response influence on the filter group delay characteristics at a minimum, the filter amplifier provides 0 dB gain and has a 3 dB bandwidth of at least 4 MHz. It can be configured for Sallen and Key low-pass with Bessel characteristic and a 3 dB cut frequency of about 800 kHz.

The SA639 incorporates an active data switch to derive the data comparator reference voltage by means of routing a portion of data signal to an external integration circuit. The data switch is typically closed for 10 ms in the course of 32-bit synchronization sequence, and is open otherwise. The time constant of the external integration circuit is about 5 ms to 10 ms. This active switch provides excellent tracking behavior over a DC input range of 1.2 V to 2.0 V. The slew rate is better than 1 V/ms. When the switch is opened, the output is in a 3-state mode with a leakage current of less than 100 nA. This reduces the discharge of the external integration circuit. As compared to other similar FM/IF chips, another advantage of SA639 is that during power-down mode (between data bursts) the data switch outputs a reference of about 1.6 V to maintain a charge on the external RC circuit. This idea helps extract the reference voltage for the external capacitor in a shorter time and improves the accuracy of the voltage on the capacitor. The overall system is suited for battery operated high-quality products in digital wireless personal communications. Detailed specifications of SA639 can be found in Ref. 3.

4. Structure of the SA639 evaluation board

A SA639-based evaluation board has been developed based on DECT specifications. The structure of this board is illustrated in Figure 7 together with a VCO/FM discriminator-based GFSK modem (modulator/demodulator). The demo board contains the entire demodulator as well as the Gaussian low-pass filter (LPF) for the modulator. The DECT modulated signal, therefore, can be generated either by a standard DECT signal generator, or by sending a 1.152 Mbit/s data stream to the on-board Gaussian LPF (BT_b = 0.5), then applying the filtered baseband waveform to an FM signal generator with a modulation index of 0.5. The output is then the GFSK modulated signal (DECT). The schematic of the Gaussian LPF can be found in Figure 14. Baseband eye-diagram at the output of the Gaussian LPF is presented in Figure 8.

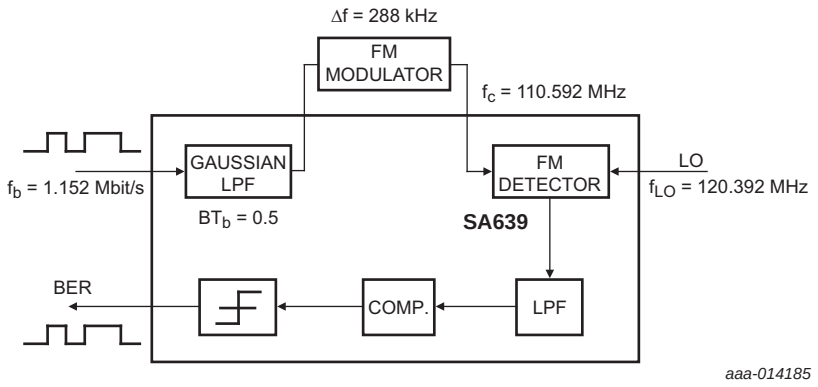


Fig 7. Structure of the SA639 GFSK evaluation board

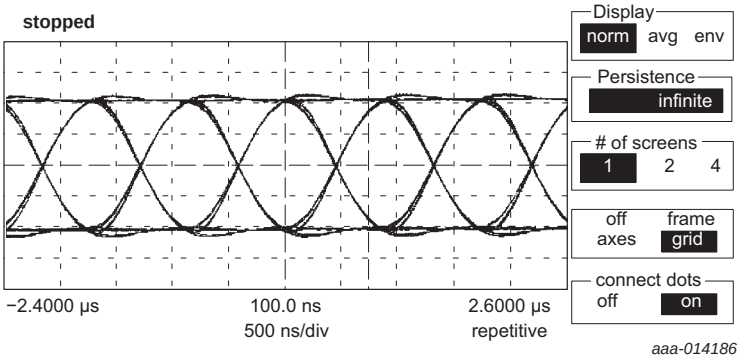


Fig 8. Measured eye-diagram at the output of Tx Gaussian LPF

At the output of the limit/frequency discriminator, the post-detection amplifier is configured as a Sallen and Key LPF to eliminate noise. For the convenience of operation, the evaluation board is designed in such a way that the reference voltage for the data comparator can be obtained either from the switch controlled DC extraction circuit, or directly from the power supply. If the DECT Burst Mode Control circuit is available, the active data switch can be used to extract and track DC level during the synchronization sequence. Otherwise the DC reference can be obtained from the power supply and manually adjusted for the comparator operation.

A two-level threshold detector with sampling time adjustment circuit is implemented on the board for data regeneration. The phase of data clock can be adjusted manually through a monostable multivibrator (74HC123) to achieve the optimal sampling time. The demo board is initially adjusted for a bit rate of 1.152 Mbit/s. If a different data rate is used, the sampling time must be re-adjusted. The output of the threshold detector is the regenerated binary data, which can be sent to a data error analyzer to evaluate the BER performance.

The symbol timing recovery (STR) circuit is not implemented on this evaluation board. Transmit data clock either hard-wire connected from the transmitter or from a separate STR circuit is required for the operation. The performance measurements presented in this application note were conducted with hard-wire connected data clock. However, BER degradation caused by STR should not be more than 1 dB (Ref. 6).

This SA639-based GFSK demo board is designed with DECT specifications at RF frequency of 110.592 MHz, LO frequency of 120.392 MHz, and intermediate frequency of 9.8 MHz. For different frequency plan applications, the step-by-step matching circuit design procedure can be found in Ref. 1. Table 2 and Table 3 present the SA639 RF/LO input impedance and mixer/limiter output impedance over frequency, respectively.

Table 2. SA639 RF/LO input impedance over frequency

Frequency	RF input	LO input
50 MHz	846 Ω || 4.52 pF	6900 Ω || 4.07 pF
110 MHz	687 Ω || 3.84 pF	4900 Ω || 4.09 pF
240 MHz	510 Ω || 3.69 pF	1900 Ω || 4.22 pF
500 MHz	190 Ω || 4.21 pF	245 Ω || 4.98 pF

Table 3. SA639 mixer/limiter output impedance over frequency

Frequency	RF input	LO input
0.5 MHz	395 Ω || 20.2 pF	438 Ω || 14.5 pF
10 MHz	350 Ω || 6.67 pF	383 Ω || 3.5 pF
21 MHz	339 Ω || 4.58 pF	393 Ω || 2.04 pF
50 MHz	326 Ω || 3.44 pF	391 Ω || 1.35 pF

5. Performance evaluation

Performance of this SA639 based DECT GFSK system including BER and sensitivity to frequency off-set and FM deviation variation is experimentally evaluated. Measurement procedures and the measured results are presented in this section.

Figure 9 illustrates the measurement set-up with the SA639 DECT evaluation board. A data error analyzer is employed to generate a pseudo random binary sequence (PRBS) with length of 10^9–1 at a data rate of 1.152 Mbit/s. This data sequence is sent to a DECT signal generator to generate a standard DECT modulated signal at 110.592 MHz. Another signal generator is employed to provide an LO signal at 120.392 MHz for the FM/IF system detection. The reference DC voltage for the data comparator is obtained from power supply for this evaluation. Data clock signal is directly from the data error analyzer. The sampling time is manually adjusted at the center of baseband eye diagram. Recovered data sequence is fed back to the Data Error Analyzer for BER measurement.

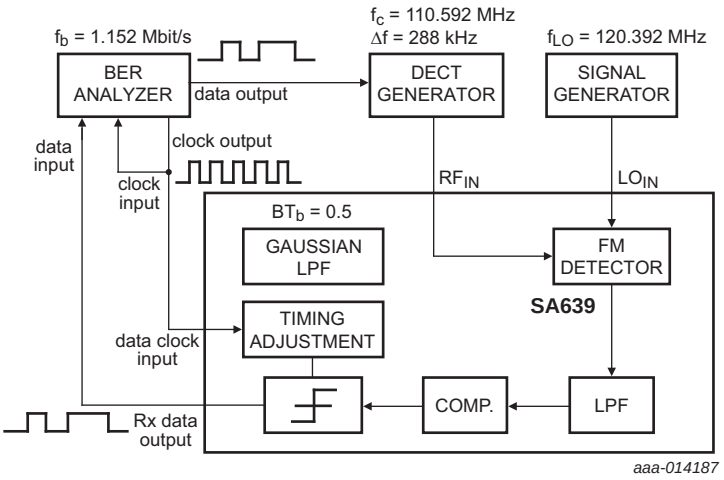


Fig 9. Block diagram of the BER evaluation setup

The BER measurement procedures can be summarized as follows:

- Build the measurement setup as shown in Figure 9.
- Measure SINAD at the data output of SA639:
  - RF = 110.592 MHz, fm = 1 kHz, Df = 288 kHz
  - LO = 120.392 MHz, –10 dBm
  - the typical sensitivity for 12 dB SINAD should be about –97 dBm
- Check SA639 output level: tune the quad tank circuit to have the least distorted eye-diagrams at the post op amp output. The DC level should be about 1.4 V to 1.7 V.
- Check the DC reference for the comparator: set the reference voltage at the DC level of the op amp output by adjusting VR1 in Figure 14.
- Adjust sampling position: set the up edge of the clock at pin 11 of 74HC74 to be at the center of the eye-diagram at pin 2 of LM311B by adjusting VR2 in Figure 14.
- Measure BER with high RF level: set RF input signal level at –60 dBm; LO signal level at –10 dBm: error free.

- Measure BER versus RF input level curve:
  - RF level: –76 dBm ~ –86 dBm
  - LO level: –10 dBm, at each point, at least 100 errors must be measured

The recovered baseband eye-diagram is shown in Figure 10, and the measured BER versus RF input level is presented in Figure 11. It can be seen that about –83 dBm RF power is needed to achieve the bit error rate of 10^{-3}. Since a typical front-end circuit has a better noise figure than FM/IF system, it is common to achieve more than 5 dB signal-to-noise ratio gain by the front-end circuit. Therefore, with the SA639 FM/IF the overall system sensitivity could be better than –88 dBm for the BER of 10^{-3}. Based on our measurements, by applying the Philips UAA2077AM 2 GHz image rejecting front-end to the SA639 FM/IF system, the overall system sensitivity is –91 dBm for the BER of 10^{-3}. This performance compares very well to the DECT specifications for public access equipment (–86 dBm for 10^{-3} BER).

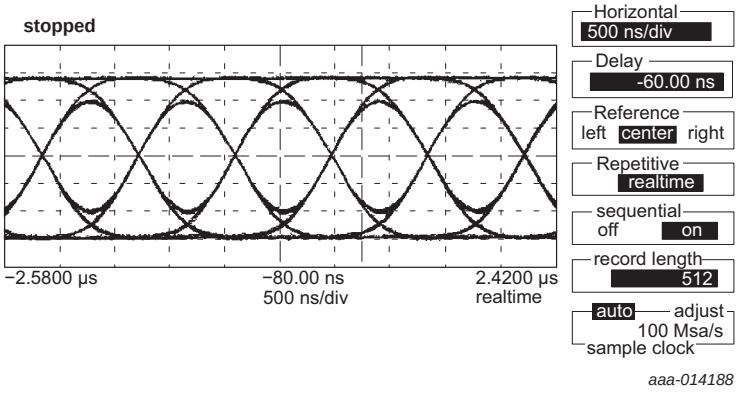
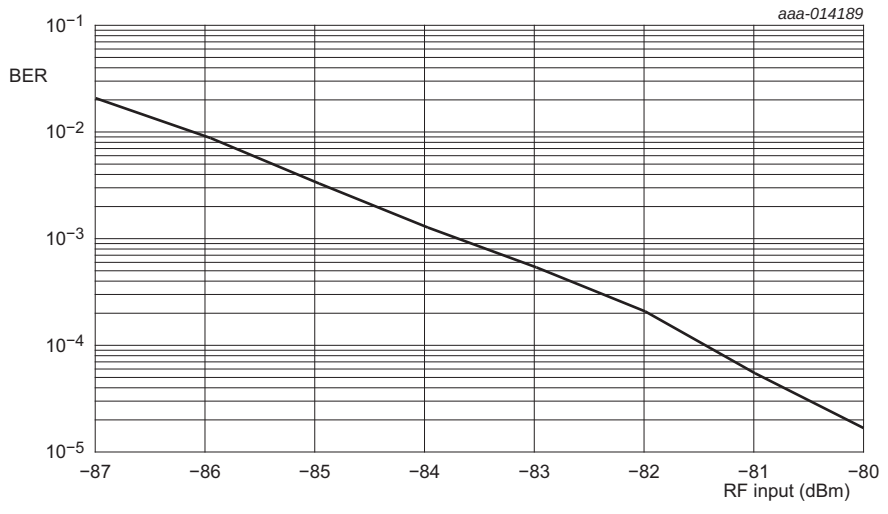


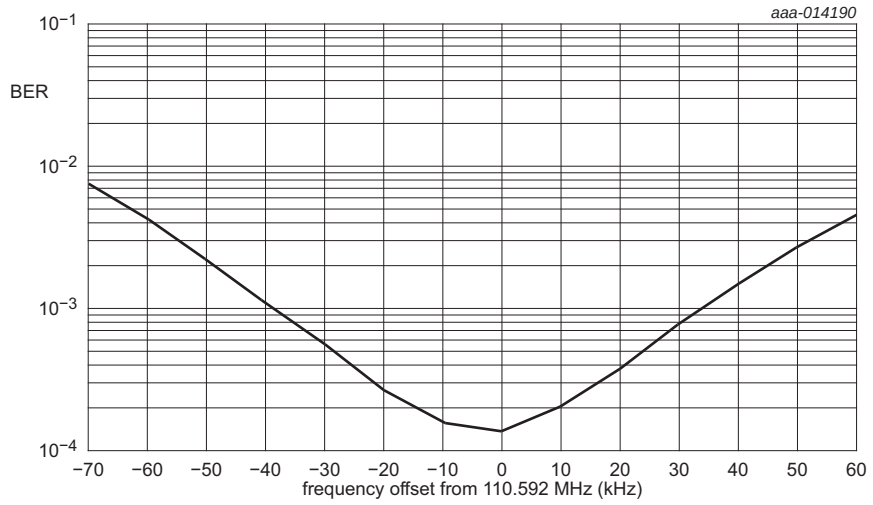
Fig 10. Recovered eye-diagram at the output of SA639



RF = 110.592 MHz; LO = 120.392 MHz; f_b = 1.152 Mbit/s

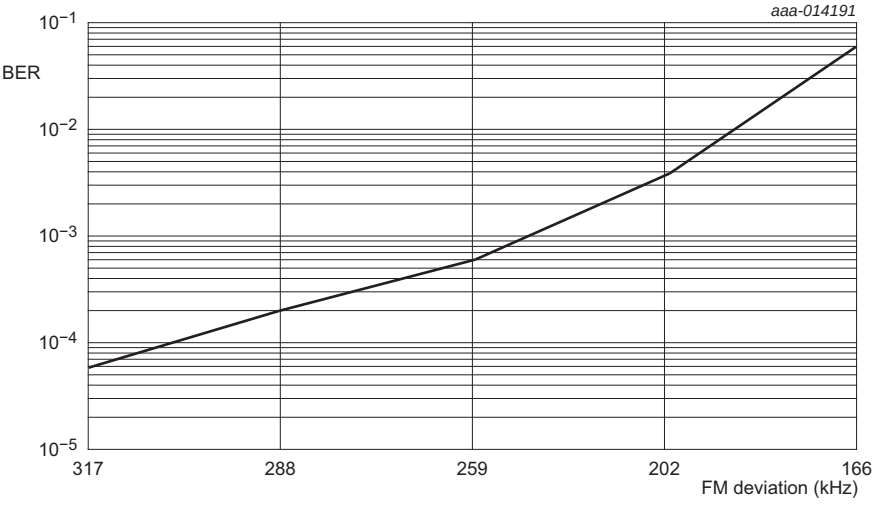
Fig 11. BER of the SA639 DECT demo board

The performance degradation caused by frequency off-set and the sensitivity to FM deviation variation of this system are also evaluated. Figure 12 presents the measured BER versus frequency offset. Even with 50 kHz offset, only minor degradation can be observed, and –82 dBm RF level is enough for 10^{-3} BER. The sensitivity of this system to FM deviation variation is illustrated in Figure 13. Even with 10 % deviation reduction (259 kHz), less than –82 dBm RF signal is needed to achieve the BER of 10^{-3}. These results indicate that the NXP SA639 FM/IF system provides superior performance for DECT and other high data rate GFSK applications.



RF = –82 dBm

Fig 12. BER degradation caused by frequency offset



RF = 110.592 MHz, –82 dBm; f_b = 1.152 Mbit/s

Fig 13. BER versus FM deviation

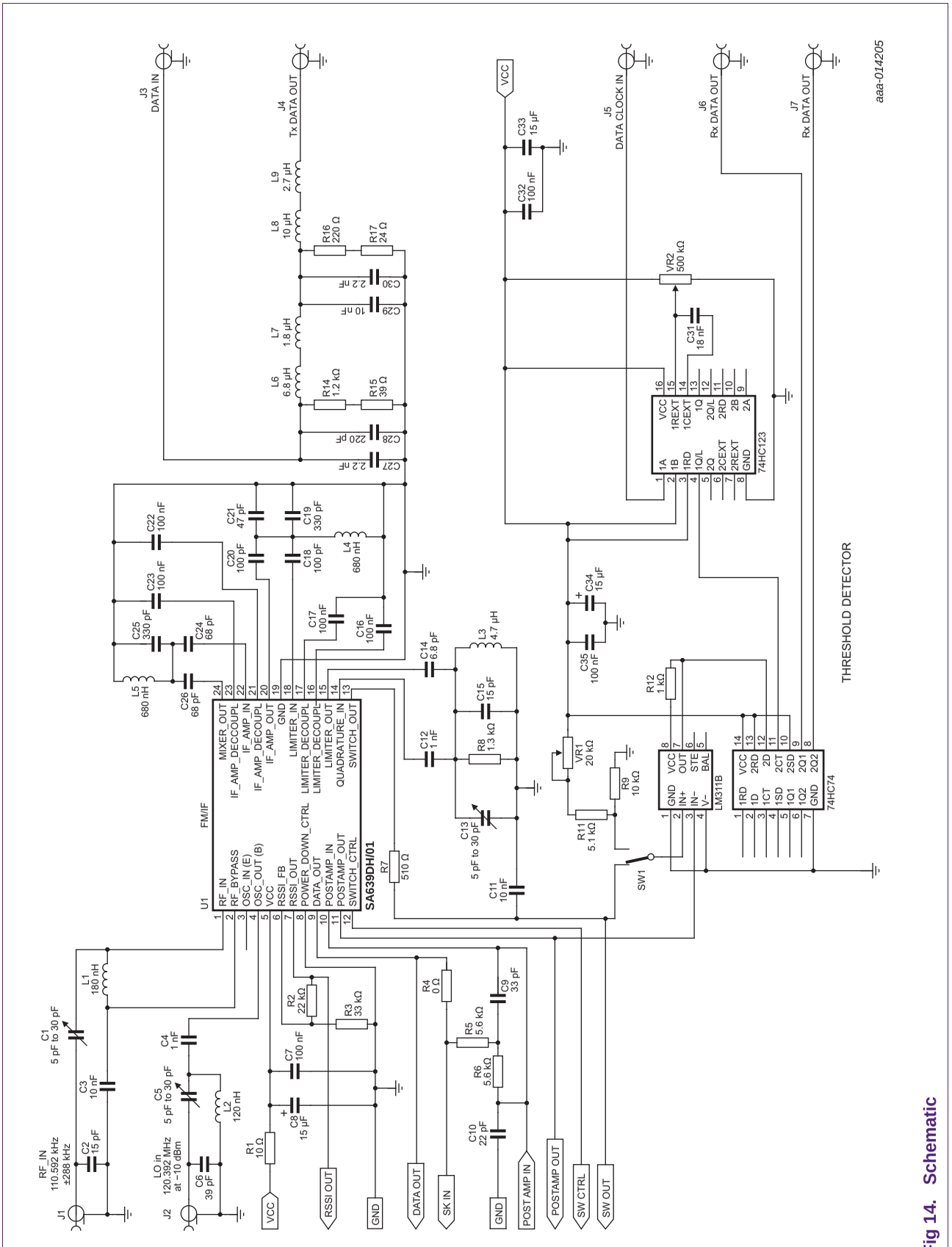


Fig 14. Schematic

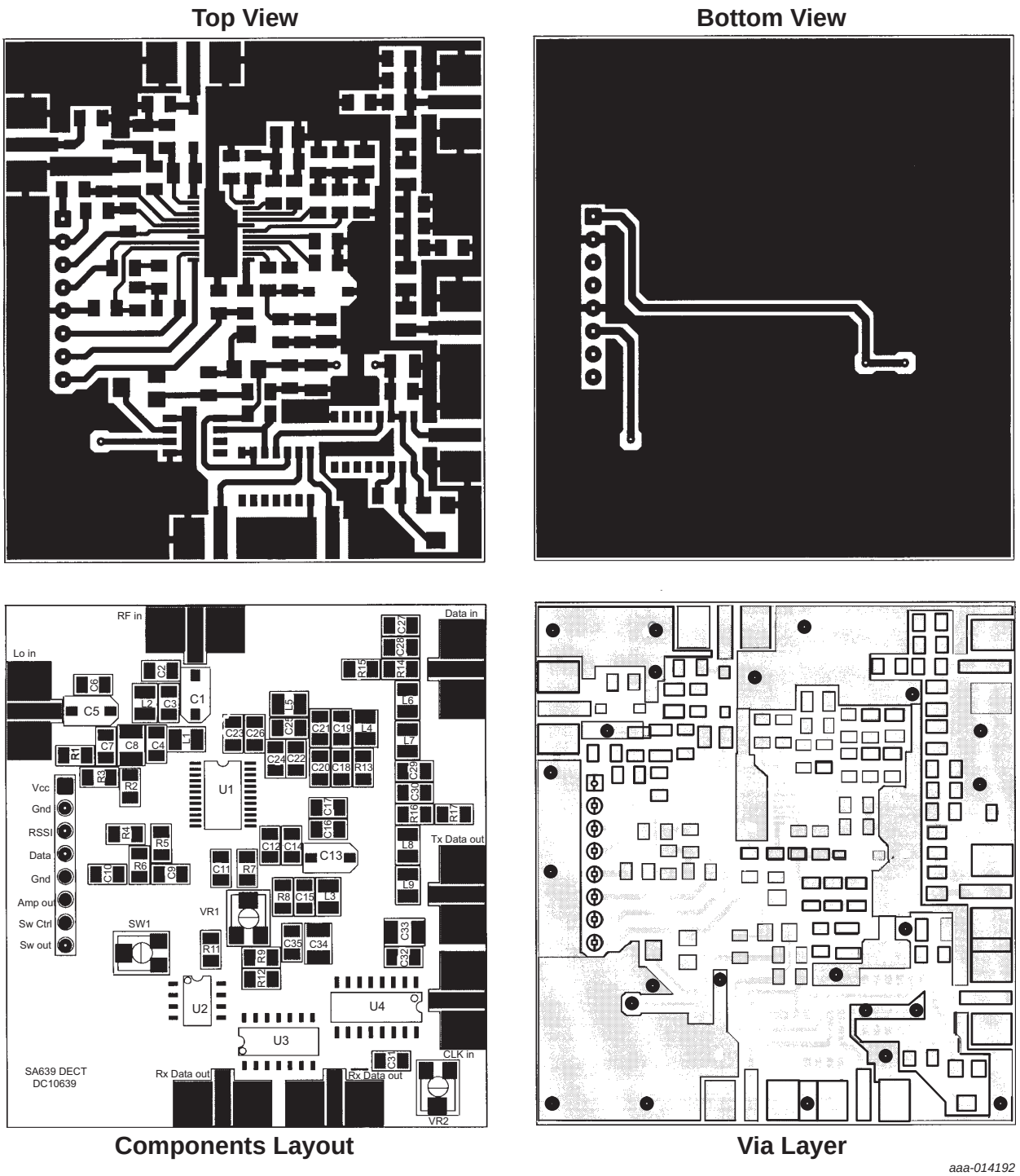


Fig 15. Board layout

Table 4. Customer application component list for GMSK/GFSK demo board

Quantity	Value	Voltage	Component	Description	Vendor	Manufacturer	Part number
Surface mount capacitors							
1	6.8 pF	50 V	C14	cap. cer. 1206 NPO ± 5 %	Garrett	Philips	1206CG689C9BB2
2	15 pF	50 V	C2, C15	cap. cer. 1206 NPO ± 5 %	Garrett	Philips	1206CG150J9BB2
1	18 pF	50 V	C31	cap. cer. 1206 NPO ± 5 %	Garrett	Philips	1206CG180J9BB2
1	22 pF	50 V	C10	cap. cer. 1206 NPO ± 5 %	Garrett	Philips	1206CG220J9BB2
1	33 pF	50 V	C9	cap. cer. 1206 NPO ± 5 %	Garrett	Philips	1206CG330J9BB2
1	39 pF	50 V	C6	cap. cer. 1206 NPO ± 5 %	Garrett	Philips	1206CG390J9BB2
1	47 pF	50 V	C21	cap. cer. 1206 NPO ± 5 %	Garrett	Philips	1206CG470J9BB2
2	68 pF	50 V	C24, C26	cap. cer. 1206 NPO ± 5 %	Garrett	Philips	1206CG680J9BB2
2	100 pF	50 V	C18, C20	cap. cer. 1206 NPO ± 5 %	Garrett	Philips	1206CG101J9BB2
1	220 pF	50 V	C28	cap. cer. 1206 NPO ± 5 %	Garrett	Philips	1206CG221J9BB2
2	330 pF	50 V	C19, C25	cap. cer. 1206 NPO ± 5 %	Garrett	Philips	1206CG331J9BB2
2	1000 pF	50 V	C4, C12	cap. cer. 1206 NPO ± 5 %	Garrett	Philips	1206CG102J9BB2
2	2200 pF	50 V	C27, C30	cap. cer. 1206 NPO ± 5 %	Garrett	Philips	1206CG222J9BB2
3	0.01 µF	50 V	C3, C11, C29	cer. cap. 1206 X7R ± 10 %	Garrett	Philips	12062R103K9BB2
7	0.1 µF	50 V	C7, C16, C17, C22, C23, C32, C35	cer. cap. 1206 X7R ± 10 %	Garrett	Philips	12062R104K9BB2
3	15 µF	10 V	C8, C33, C34	tantalum capacitor chips	Garrett	Philips	49MC106C006KOAS
Surface mount variable capacitors							
3	5 pF to 30 pF		C1, C5, C13	trimmer capacitor	Kent Elect	Kyocera	CTZ3S-30C-W1
Surface mount resistors							
1	0 Ω	50 V	R4	Res. chip 1206 ± 5 %	Garrett	ROHM	MCR18JW000E
1	10 Ω	50 V	R1	Res. chip 1206 ± 5 %	Garrett	ROHM	MCR18JW100E
1	24 Ω	50 V	R17	Res. chip 1206 ± 5 %	Garrett	ROHM	MCR18JW240E
1	39 Ω	50 V	R15	Res. chip 1206 ± 5 %	Garrett	ROHM	MCR18JW390
1	220 Ω	50 V	R16	Res. chip 1206 ± 5 %	Garrett	ROHM	MCR18JW221E
1	510 Ω	50 V	R7	Res. chip 1206 ± 5 %	Garrett	ROHM	MCR18JW511E
1	560 Ω	50 V	R13	Res. chip 1206 ± 5 %	Garrett	ROHM	MCR18JW561E
1	1 kΩ	50 V	R12	Res. chip 1206 ± 5 %	Garrett	ROHM	MCR18JW102E
1	1.2 kΩ	50 V	R14	Res. chip 1206 ± 5 %	Garrett	ROHM	MCR18JW122E
1	1.3 kΩ	50 V	R8	Res. chip 1206 ± 5 %	Garrett	ROHM	MCR18JW132E
1	5.1 kΩ	50 V	R11	Res. chip 1206 ± 5 %	Garrett	ROHM	MCR18JW512E
2	5.6 kΩ	50 V	R5, R6	Res. chip 1206 ± 5 %	Garrett	ROHM	MCR18JW562E
1	10 kΩ	50 V	R9	Res. chip 1206 ± 5 %	Garrett	ROHM	MCR18JW223E
1	22 kΩ	50 V	R2	Res. chip 1206 ± 5 %	Garrett	ROHM	MCR18JW223E
1	33 kΩ	50 V	R3	Res. chip 1206 ± 5 %	Garrett	ROHM	MCR18JW333E

Table 4. Customer application component list for GMSK/GFSK demo board *…continued*

Quantity	Value	Voltage	Component	Description	Vendor	Manufacturer	Part number
Surface mount variable resistors							
1	20 kΩ	50 V	VR1	trimmer resistor 0.25 W ± 20 %	Garrett	Philips	ST-4TA203
1	500 kΩ	50 V	VR2	trimmer resistor 0.25 W ± 20 %	Garrett	Philips	ST-4TA504
Surface mount switch							
1	SPDT		SW1	4 mm selector switch	Garret	Philips	CS-412YTA
Surface mount inductors							
1	120 nH		L2	chip inductor 1008 ± 10 %	Coilcraft	Coilcraft	1008CS-331XKBB
1	180 nH		L1	chip inductor 1008 ± 10 %	Coilcraft	Coilcraft	1008CS-331XKBB
2	680 nH		L4, L5	chip inductor 1008 ± 10 %	Digikey	TOKO	380NB-R68M
1	1.8 µH		L7	chip inductor 1210 ± 10 %	Garrett	J.W. Miller	PM20-1R8K
1	2.7 µH		L9	chip inductor 1210 ± 10 %	Garrett	J.W. Miller	PM20-2R7K
1	4.7 µH		L3	chip inductor 1210 ± 10 %	Garrett	J.W. Miller	PM20-4R7K
1	6.8 µH		L6	chip inductor 1210 ± 10 %	Garrett	J.W. Miller	PM20-6R8K
1	10 µH		L8	chip inductor 1210 ± 10 %	Garrett	J.W. Miller	PM20-100K
Surface mount integrated circuits							
1		5 V	U1	FM IF with filter switch	NXP	NXP	SA639
1		5 V	U2	voltage comparator	NXP	NXP	LM311B
1		5 V	U3	dual D-type flip-flop	NXP	NXP	74HC74
1		5 V	U4	dual retriggerable multivibrator	NXP	NXP	74HC123
Miscellaneous							
7			J1, J2, J3, J4, J5, J6, J7	SMA gold connector	Newark	EF Johnson	142-0701-801
1			JP1	8-pin header straight	Mouser	Molex	538-22-03-2081
1				Printed-circuit board	Excel	Philips	DC10639

6. Conclusions

An NXP low-voltage high-performance FM/IF system (SA639) based GFSK modem evaluation board is presented. Experimental performance evaluation including bit error rate (BER), sensitivity to frequency offset, and sensitivity to FM deviation variation of this system has been conducted based on DECT specifications. Results indicate that a superior performance can be achieved with the NXP FM/IF systems for high-speed digital wireless applications.

7. Abbreviations

Table 5. Abbreviations

Acronym	Description
ADPCM	Adaptive Differential Pulse Code Modulation
BER	Bit Error Rate
CODEC	COder-DECoder
DECT	Digital European Cordless Telephone
DQPSK	Differential Quadrature Phase Shift Keying
FDD	Frequency Division Duplex
FM	Frequency Modulation
GFSK	Gaussian filtered Frequency Shift Keying
IF	Intermediate Frequency
ISDN	Integrated Service Digital Network
LO	Local Oscillator
LPF	Low-Pass Filter
PACS	Personal Access Communications System
PBX	Public Branch eXchange
PCS	Physical Coding Sublayer
PHS	Personal Handyphone System
PRBS	Pseudo Random Binary Sequence
PSTN	Public Switched Telephone Network
RC	Resistor-Capacitor network
RLL	Radio Local Loop
RSSI	Received Signal Strength Indicator
SINAD	Signal-to-Noise And Distortion ratio
STR	Symbol Timing Recovery
TDD	Time Division Duplex
TDMA	Time Division Multiple Access
VCO	Voltage Controlled Oscillator
WPBX	Wireless Public Branch eXchange

8. References

[1] **AN1994, "Reviewing key areas when designing with the SA605" —** application note; NXP Semiconductors

[2] **AN1996, "Demodulation at 10.7 MHz IF with SA605/SA625" —** application note; NXP Semiconductors

[3] **SA639, Low voltage mixer FM IF system with filter amplifier and data switch —** Product data sheet; NXP Semiconductors; www.nxp.com/documents/data_sheet/SA639.pdf

[4] **AN1997, "NXP FM/IF systems for GMSK/GFSK receivers —** application note; NXP Semiconductors

[5] ***"GMSK modulation for digital mobile radio telephony" —*** K. Murota and K. Hirade; *IEEE Transactions on Communications*; July 1981

[6] ***"Digital Communications, Satellite/Earth Station Engineering" —*** Prentice Hall; 1983

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