

# X-S32K148EVBQ144/Q176

## CUSTOMER EVB

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Revisions				
Rev	Description	Designer	Date	Approved
X4	Schematic	J.Sanchez		TBD
A	First Release			

### CAUTION:

This schematic is provided for reference purposes only. As such, NXP does not make any warranty, implied or otherwise, as to the suitability of circuit design or component selection (type or value) used in these schematics for hardware design using the NXP S32K family of Microprocessors. Customers using any part of these schematics as a basis for hardware design, do so at their own risk and Freescale does not assume any liability for such a hardware design.

3 Different test points used in design:

TPVx - Through Hole Pad small

TPHx - Through Hole Pad Large (for standard 0.1" header). Also used on IO Matrix (IOMx)

TPX - Surface Mount Wire Loop

TPV?

TPH5

TP?


### Notes:

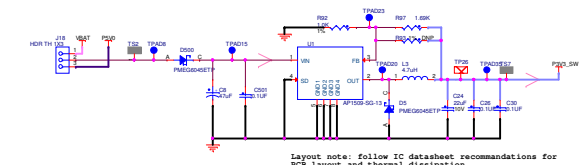
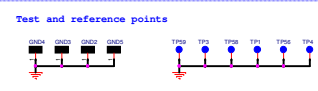
- All components and board processes are to be ROHS compliant
- All connectors and headers are denoted Jx/Px and are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2.
- 2 Pin jumpers generally have the "source" on pin 1.
- All switches are denoted SWx
- All test points (SMT wire loop style) are denoted TPx
- Test point Vias (just through hole pads) are denoted TPVx

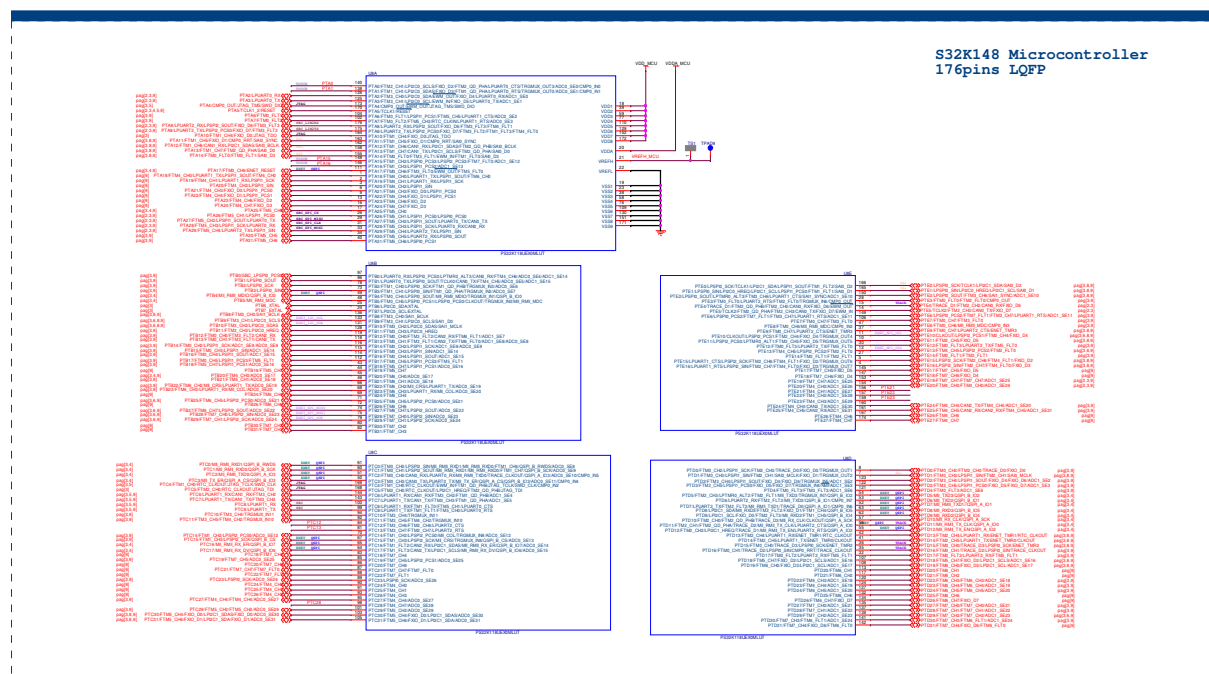
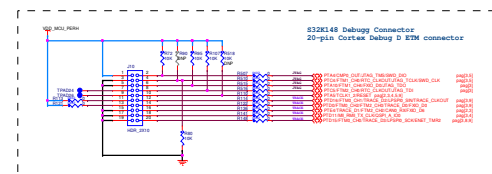
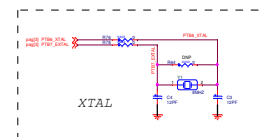
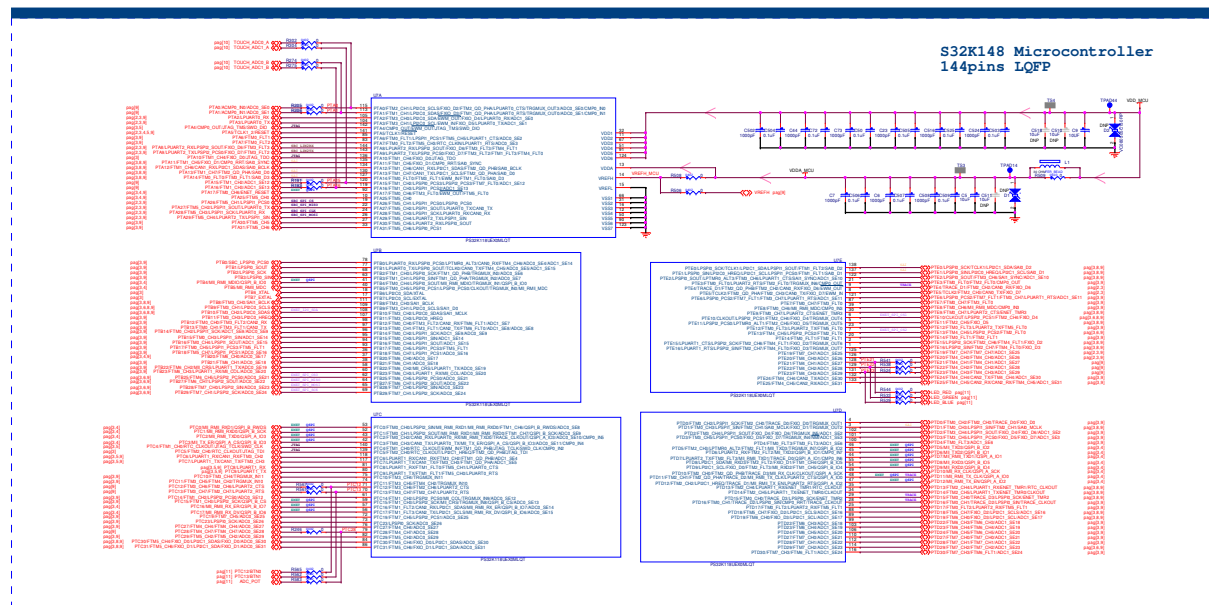
Signals (ports) have not been routed via busses as this makes it harder to determine where each signal goes.

User notes are given throughout the schematics.

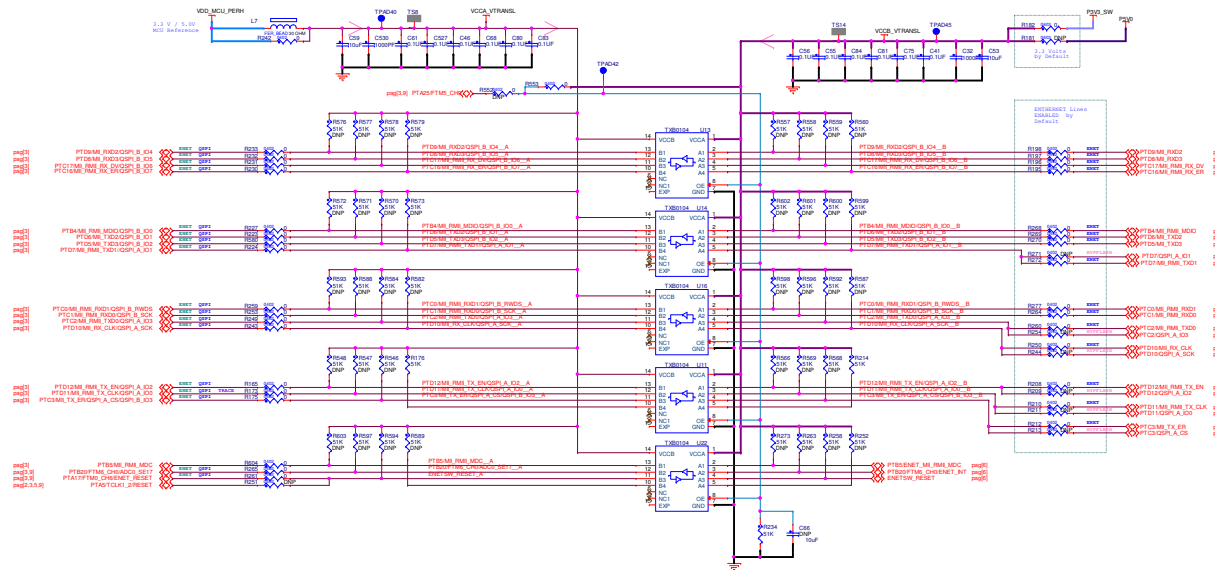
Specific PCB LAYOUT notes are detailed in ITALICS

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Approved: Juan Romero		Size B	Document Number SCH-29642 PDF: SPF-29642
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		Rev A	





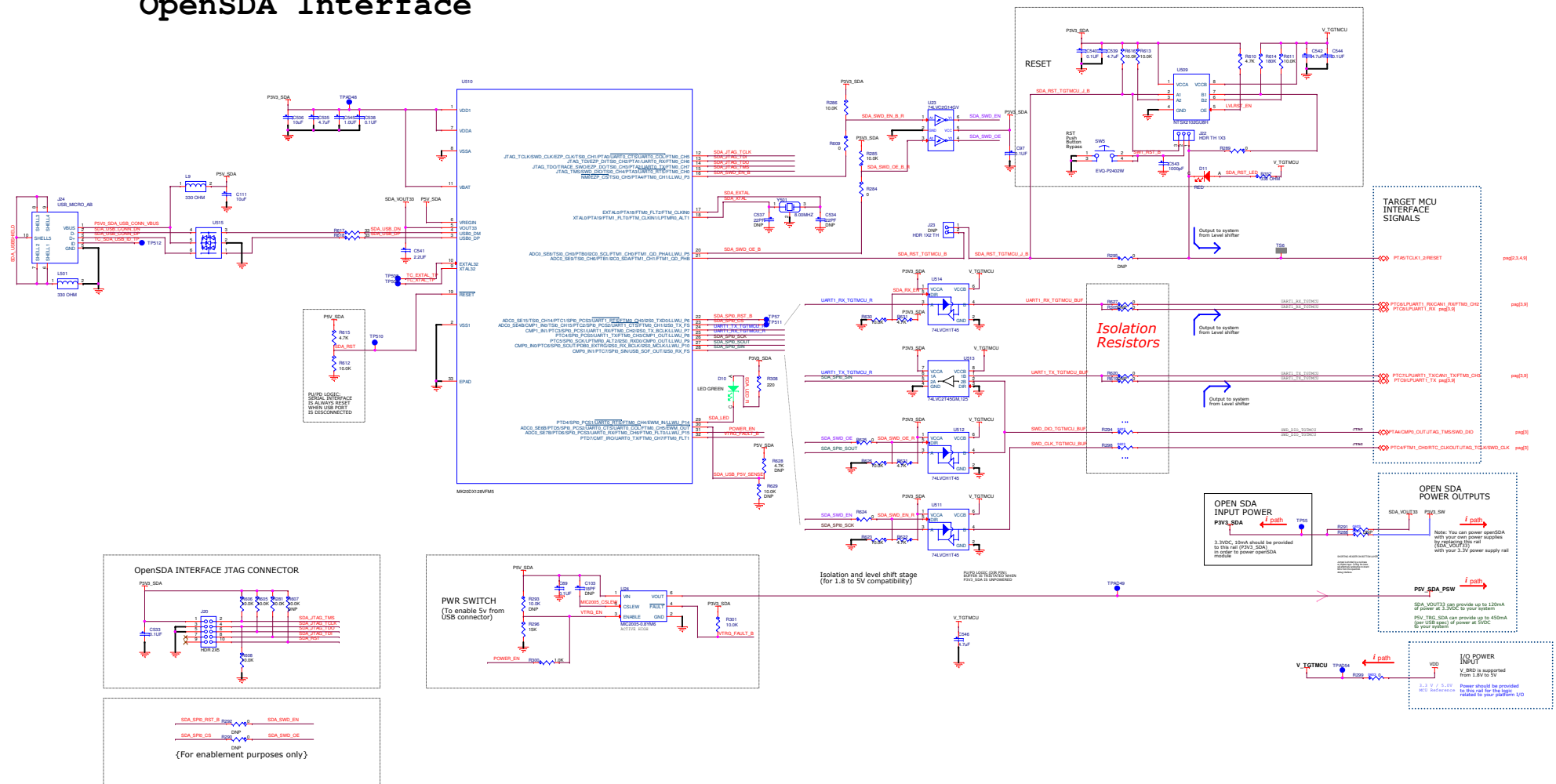
S32K148  
MCU SIGNALS




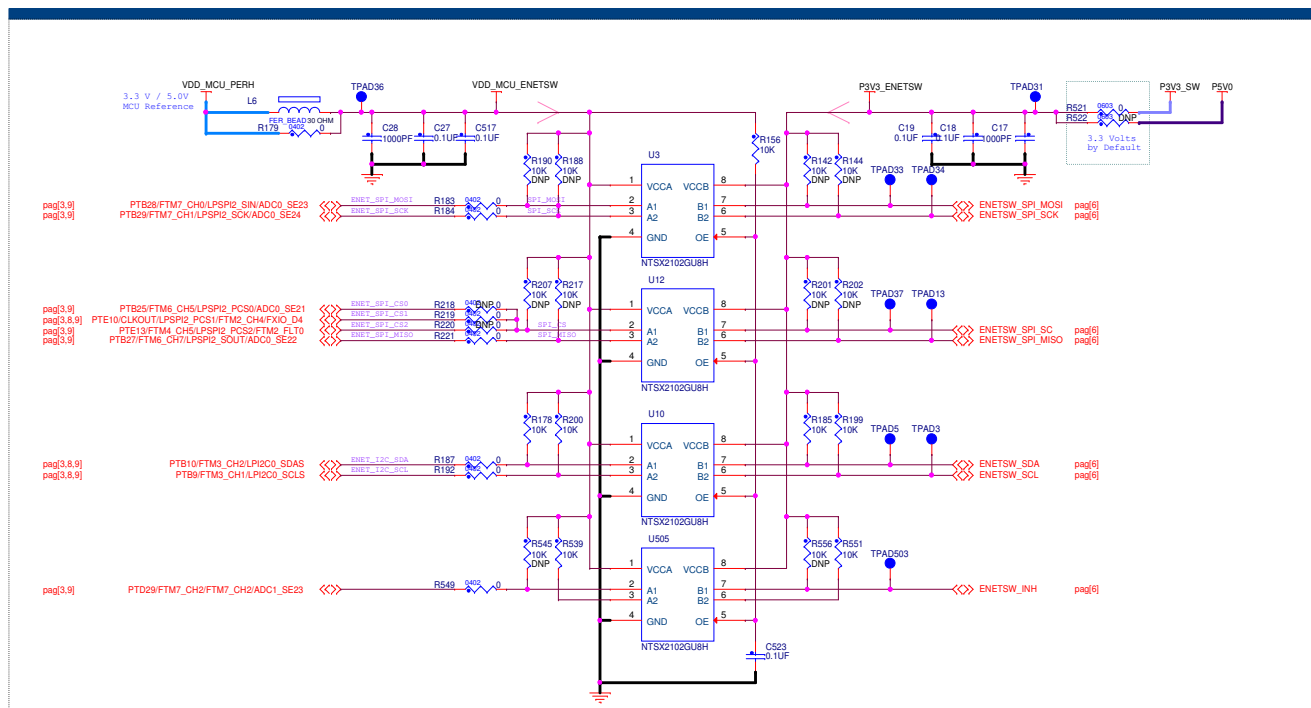
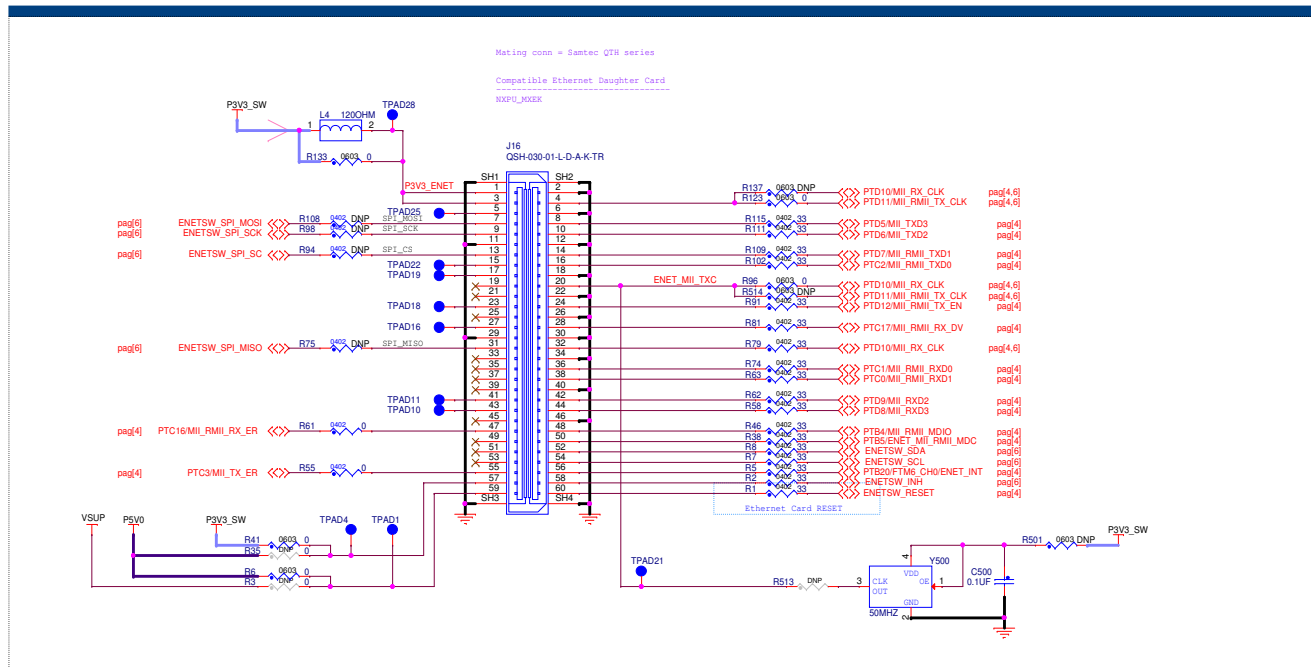
HyperFLASH &  
Ethernet Connector


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## OpenSDA Interface

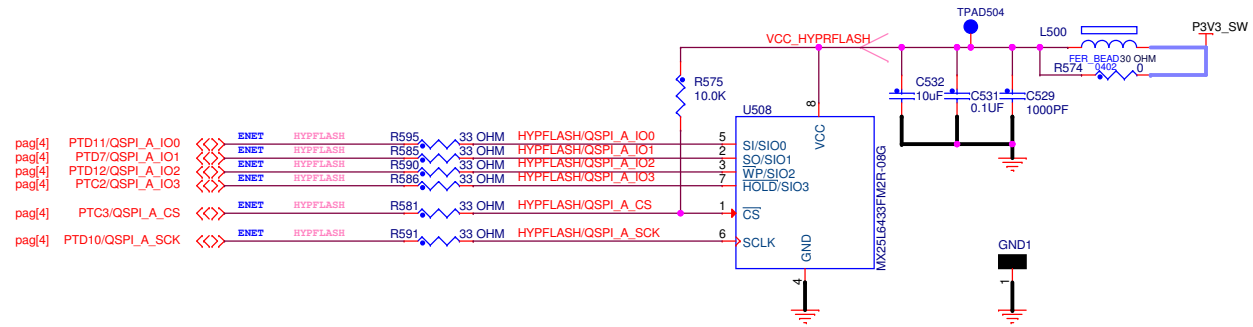


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# CMOS FLASH Memory 64M-BIT



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## SAI Audio

The diagram illustrates the SAI Audio interface configuration. The left side lists the pin functions, and the right side shows the physical pin connections to the P1 connector. The top right section details the power supply and decoupling circuitry.

Pin	Function	Connector Pin
pag[3,9]	PTA14/FTM0_FLT0/FTM3_FLT1/SAI0_D3	3
pag[3,9]	PTE0/LPSPI0_SCK/TCLK1/LP2C1_D2/SAI0_D2	5
pag[3,9]	PTE1/LPSPI0_SIN/LP2C0_HREQ/LP2C1_SCL/SAI0_D1	7
pag[3,9]	PTA13/FTM1_CH7/FTM2_QD_PHA/SAI0_D0	9
pag[3,9]	PTA12/FTM1_CH6/CAN1_RX/LP2C1_SDAS/SAI0_BCLK	11
pag[3,9]	PTA11/FTM1_CH5/FXIO_D1/CMP0_RRT/SAI0_SYNC	13
pag[3,9]	PTD1/FTM0_CH3/LPSPI1_SIN/FTM2_CH1/SAI0_MCLK	15
pag[3,9]	PTD14/FTM2_CH5/LPUART1_TX/ENET_TMR0/CLKOUT	17
pag[3,9]	PTD18/FTM5_CH7/FXIO_D2/LP2C1_SCLS/ADC1_SE16	19
pag[3,9]	PTC30/FTM5_CH4/FXIO_D0/LP2C1_SDAS/FXIO_D0/ADC0_SE30	21
pag[3,6,9]	PTB9/FTM3_CH1/LP2C0_SCLS	23
pag[3,9]	PTB8/FTM3_CH0/SAI1_BCLK	25
pag[3,9]	PTD13/FTM2_CH4/LPUART1_RX/ENET_TMR1/RTC_CLKOUT	27
pag[3,9]	PTE2/LPSPI0_SOUT/FTM3_CH6/SAI1_SYNC/ADC1_SE10	29
pag[3,6,9]	PTD19/FTM6_CH0/FXIO_D3/LP2C1_SCL/ADC1_SE17	31
pag[3,9]	PTC31/FTM5_CH6/FXIO_D1/LP2C1_SDA/FXIO_D1/ADC0_SE31	33
pag[3,9]	PTE15/LPSPI2_SCK/FTM2_CH6/FTM4_FLT1/FXIO_D2	35
pag[3,9]	PTE16/LPSPI2_SIN/FTM2_CH7/FTM4_FLT0/FXIO_D3	37
pag[3,6,9]	PTE10/CLKOUT/LPSPI2_PCS1/FTM2_CH4/FXIO_D4	39
pag[3,9]	PTD15/FTM0_CH0/TRACE_D3/LPSPI0_SCK/ENET_TMR2	41
pag[3,9]	PTE9/FTM0_CH7/LPUART2_CTS/ENET_TMR3	43
		45
		47
		49
		50

Power Supply and Decoupling:

- P5V0
- P3V3\_SW
- TPAD50
- TPAD51
- C104: 10uF
- C99: 0.1uF
- C113: 10uF
- C112: 0.1uF


Connector P1:

- 1
- 2
- 3
- 4
- 5
- 6
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Labels:

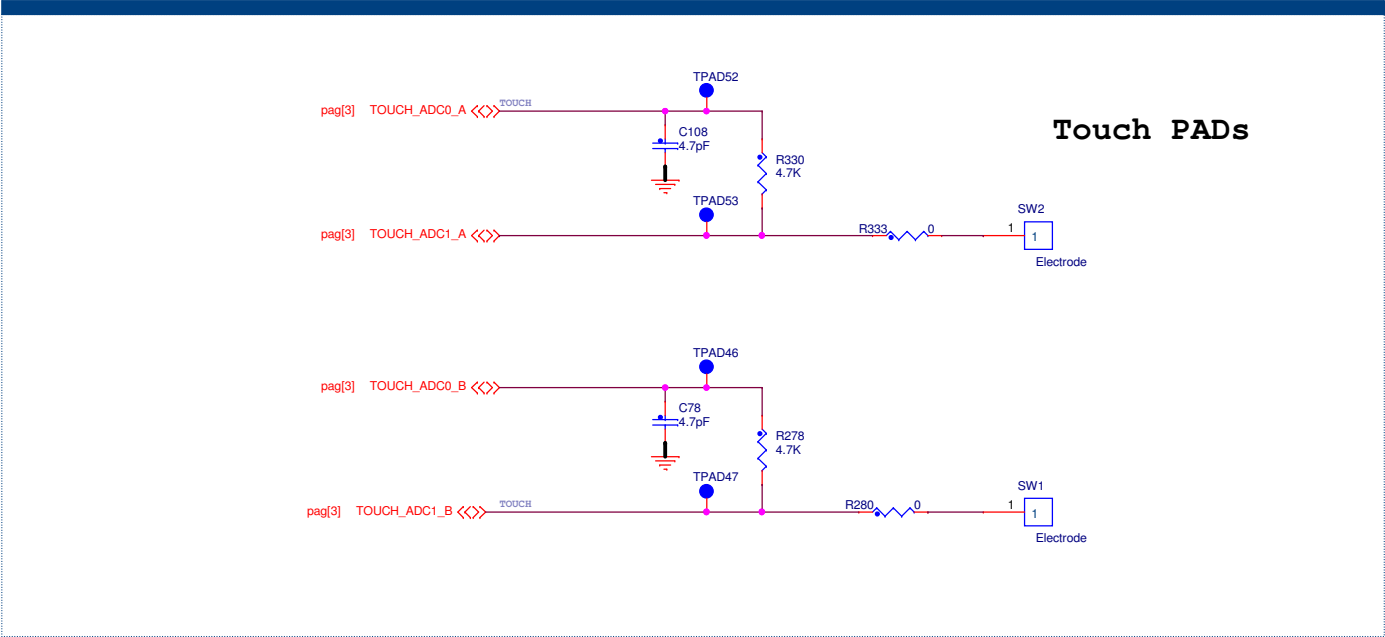
- SAI0\_DATA3
- SAI0\_DATA2
- SAI0\_DATA1
- SAI0\_DATA0
- SAI0\_BCLK
- SAI0\_SYNC
- SAI0\_MCLK
- ENET0\_TMR0
- I2C\_SCL3
- I2C\_SDA3
- SAI1\_DATA0
- SAI1\_BCLK
- SAI1\_SYNC
- SAI1\_MCLK
- I2C\_SDA2
- SAI2\_DATA0
- SAI2\_BCLK
- SAI2\_SYNC
- SAI2\_MCLK
- ENET0\_TMR2
- GPIO\_Controll

HDR\_2X25

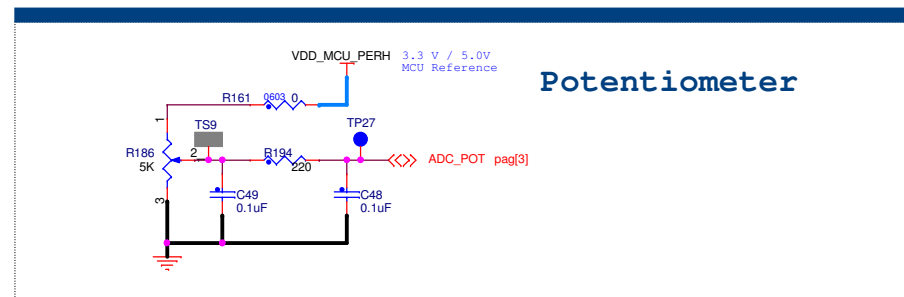
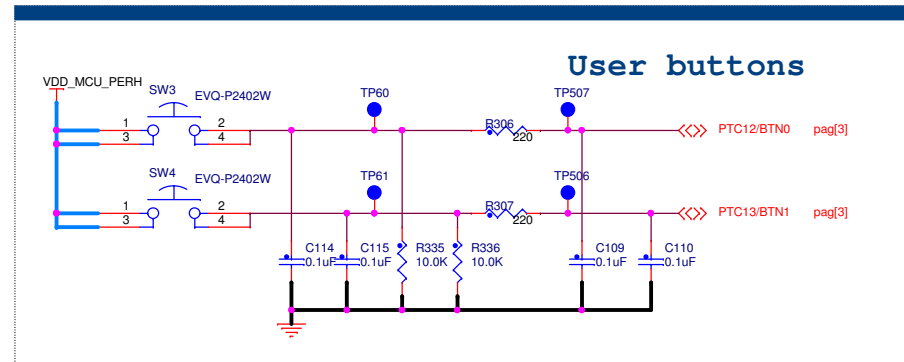
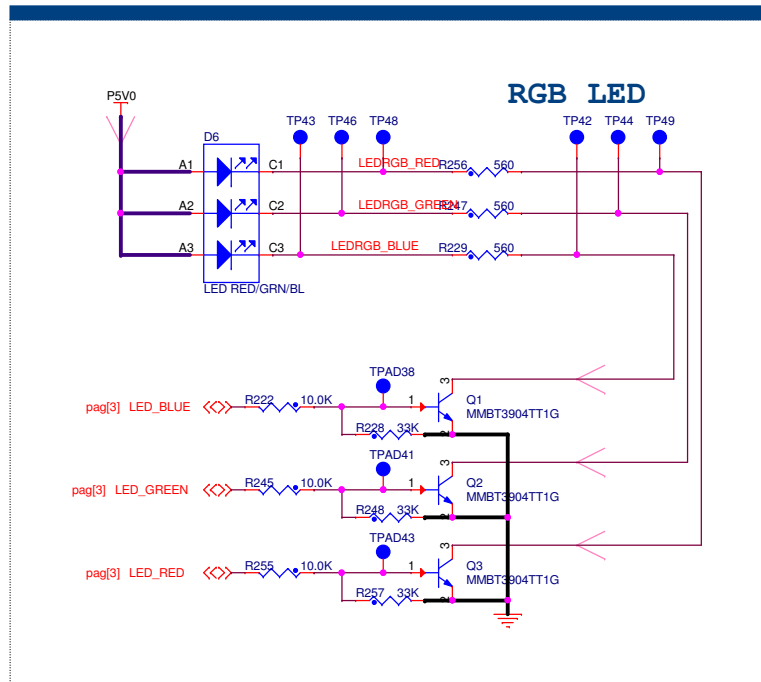
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