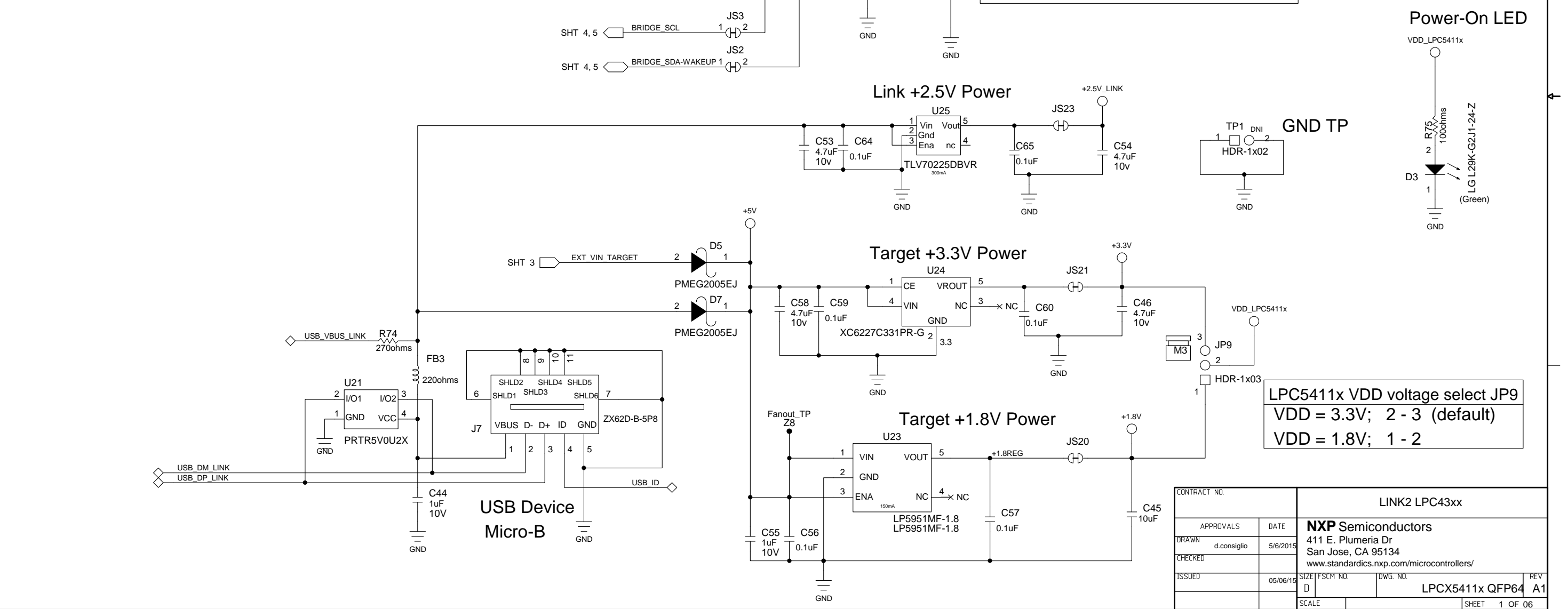
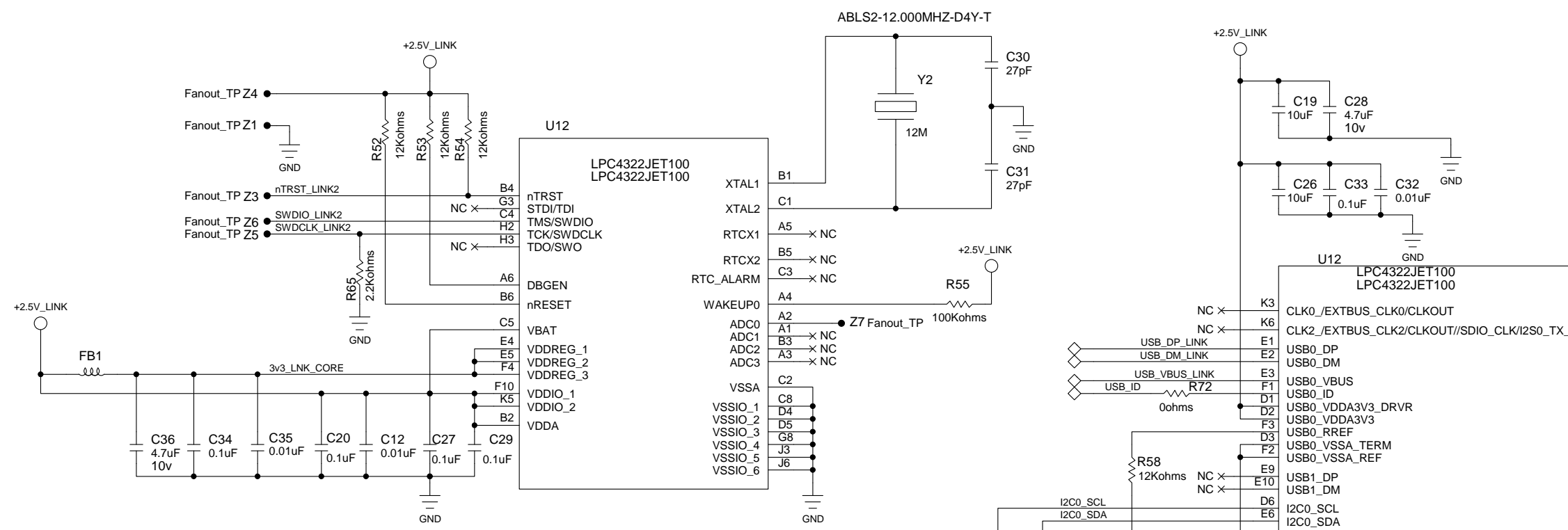


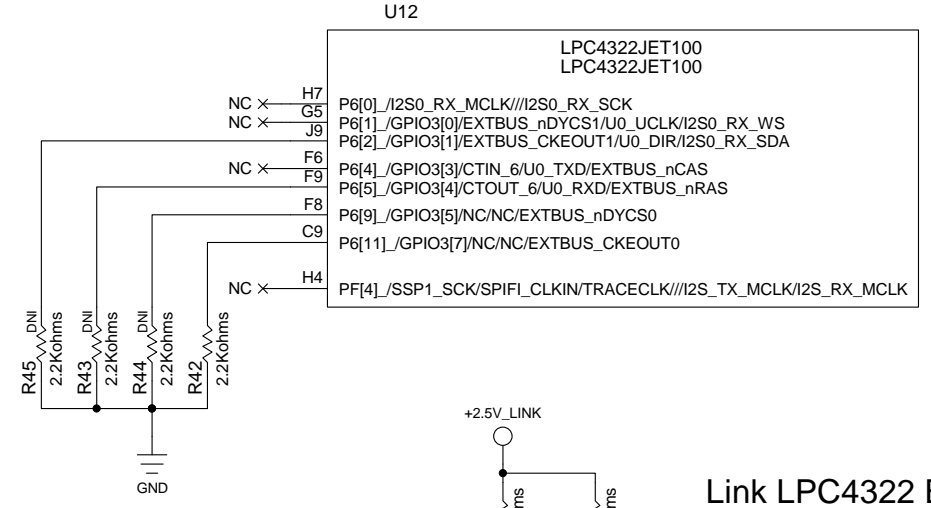
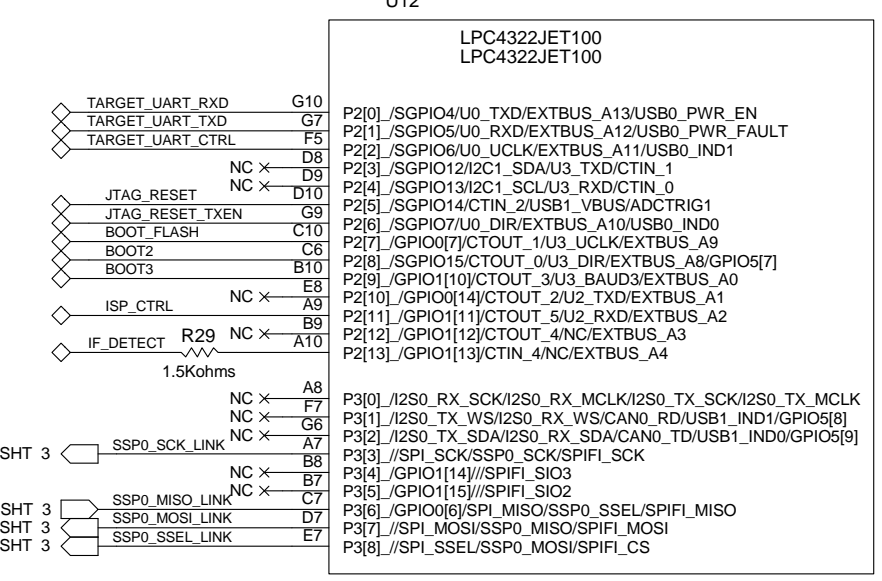
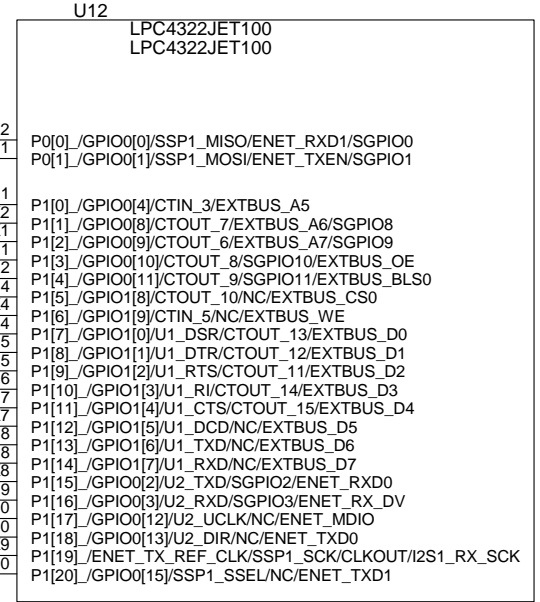
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	- Chng R19 to 4.12ohm; sht 3. - Chng JS10 to R80 4.12ohm; sht 3. - Add hdr & shunt at JP3; sht 3. - Add JS28, JS29, JS30; sht 2.	04/20/2015	
A1	- Chng C8 to 2.2uF; sht 3.	05/06/2015	



LPC5411x VDD voltage select JP9
 VDD = 3.3V; 2 - 3 (default)
 VDD = 1.8V; 1 - 2

CONTRACT NO.		LINK2 LPC43xx	
APPROVALS	DATE	NXP Semiconductors	
DRAWN	5/6/2015	411 E. Plumeria Dr	
CHECKED		San Jose, CA 95134	
ISSUED	05/06/15	www.standardics.nxp.com/microcontrollers/	
SCALE		SIZE	REV
		D	D
		DWG. NO.	LPCX5411x QFP64 A1
		SHEET	1 OF 06

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



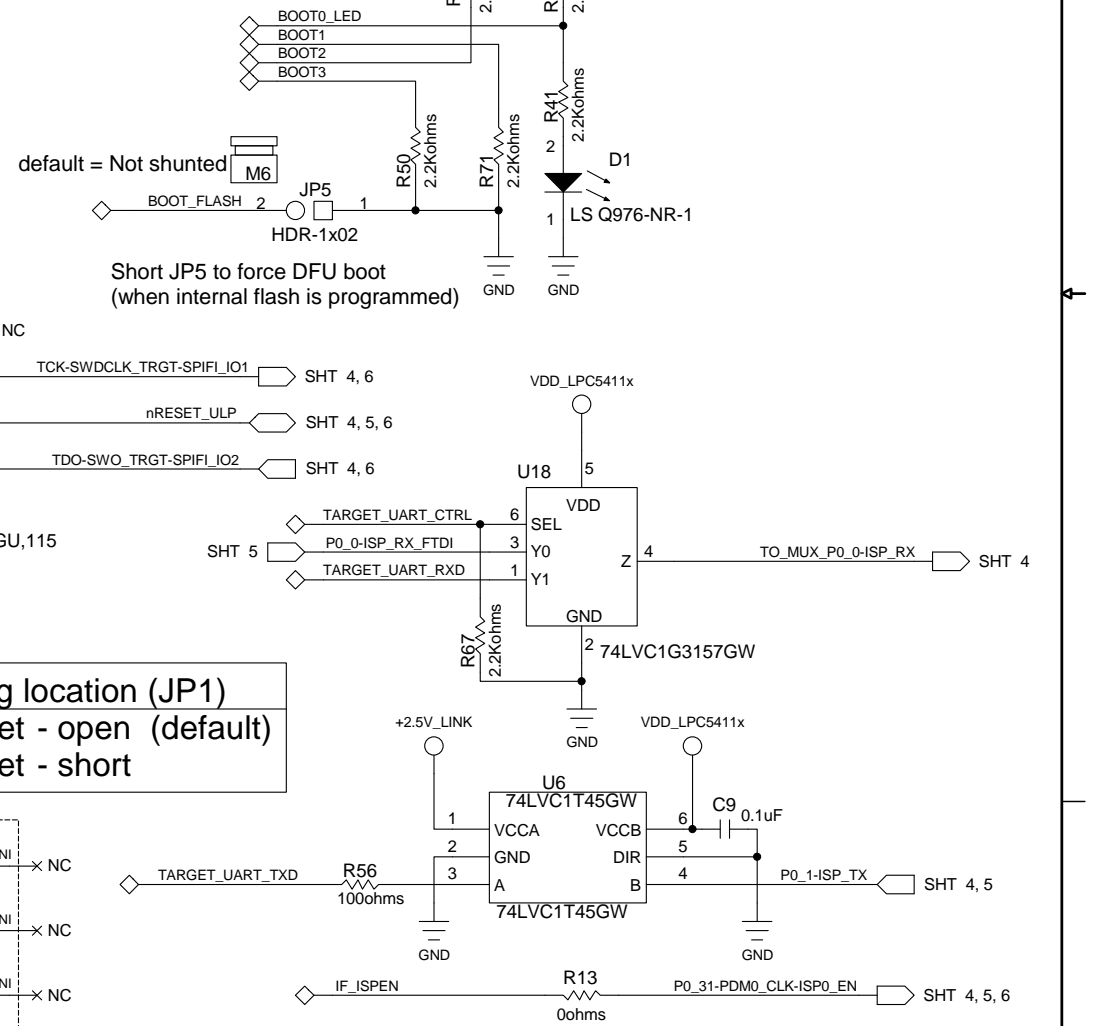
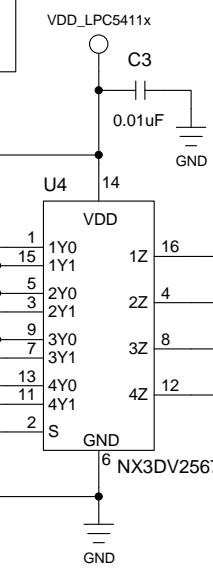
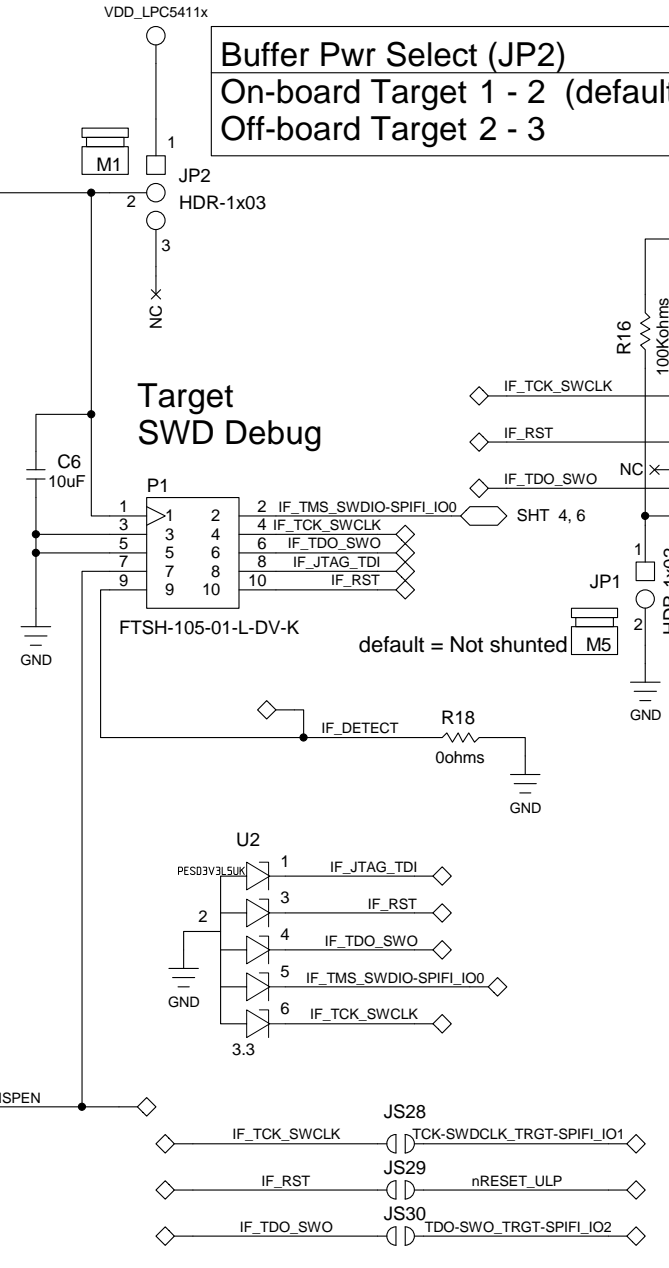
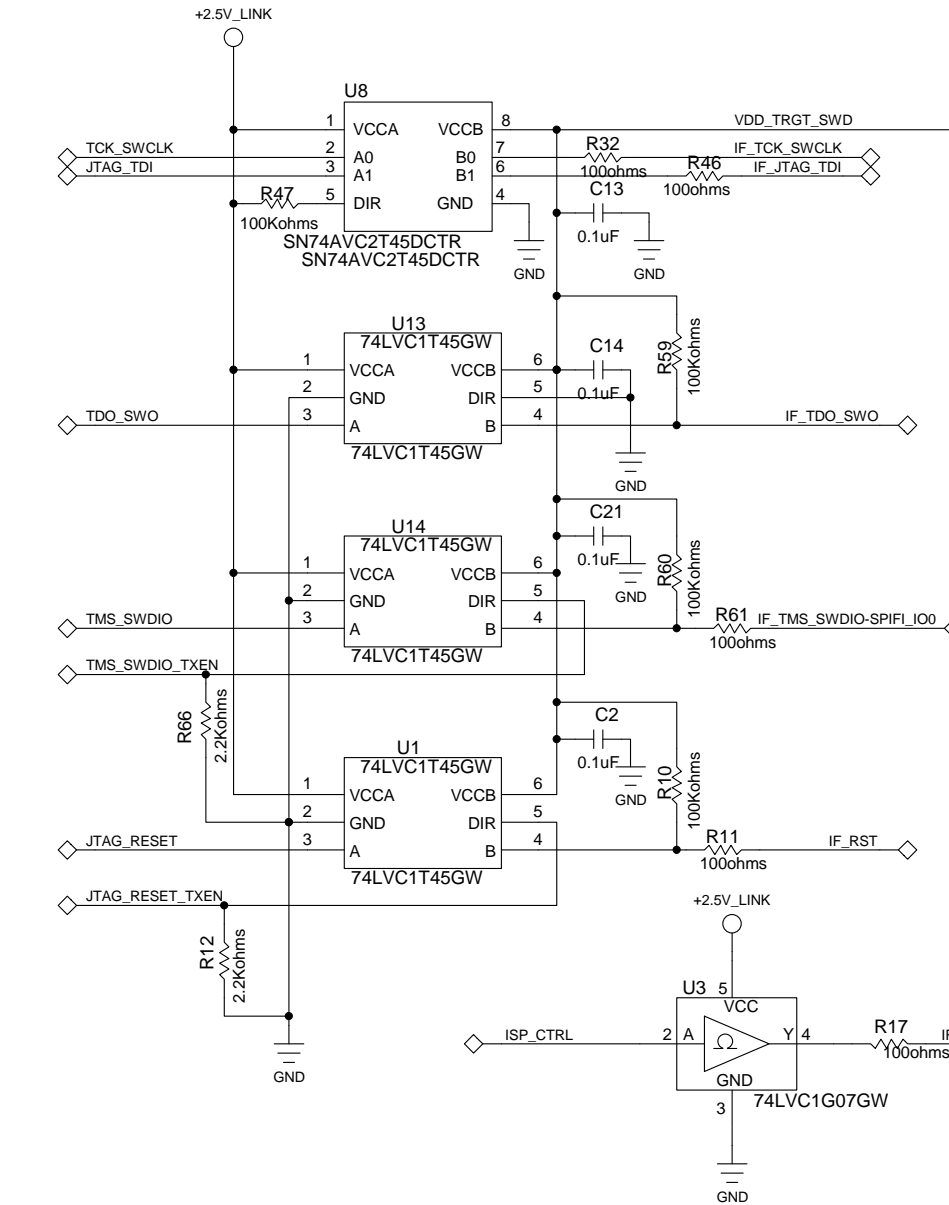
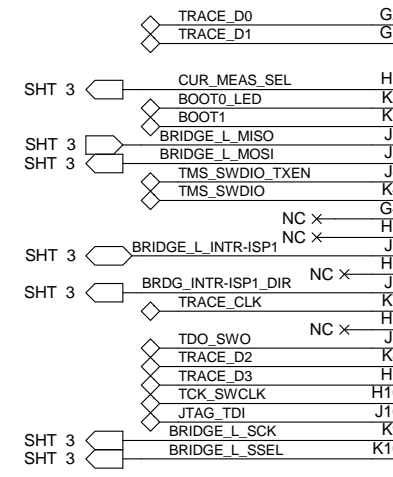
Link LPC4322 Boot mode
DFU USB0 = B3:0 = 0101

Buffer Pwr Select (JP2)
On-board Target 1 - 2 (default)
Off-board Target 2 - 3

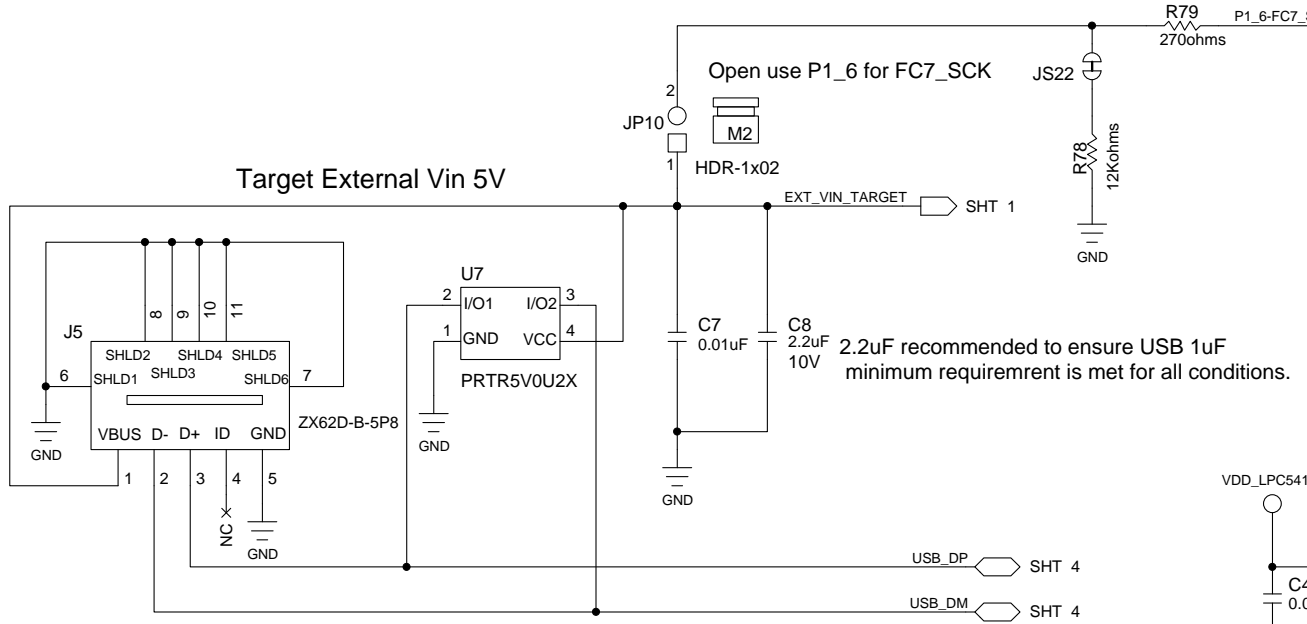
default = Not shunted
Short JP5 to force DFU boot
(when internal flash is programmed)

Target to debug location (JP1)
On-board Target - open (default)
Off-board Target - short

LPC-5411x Target
does not have trace.

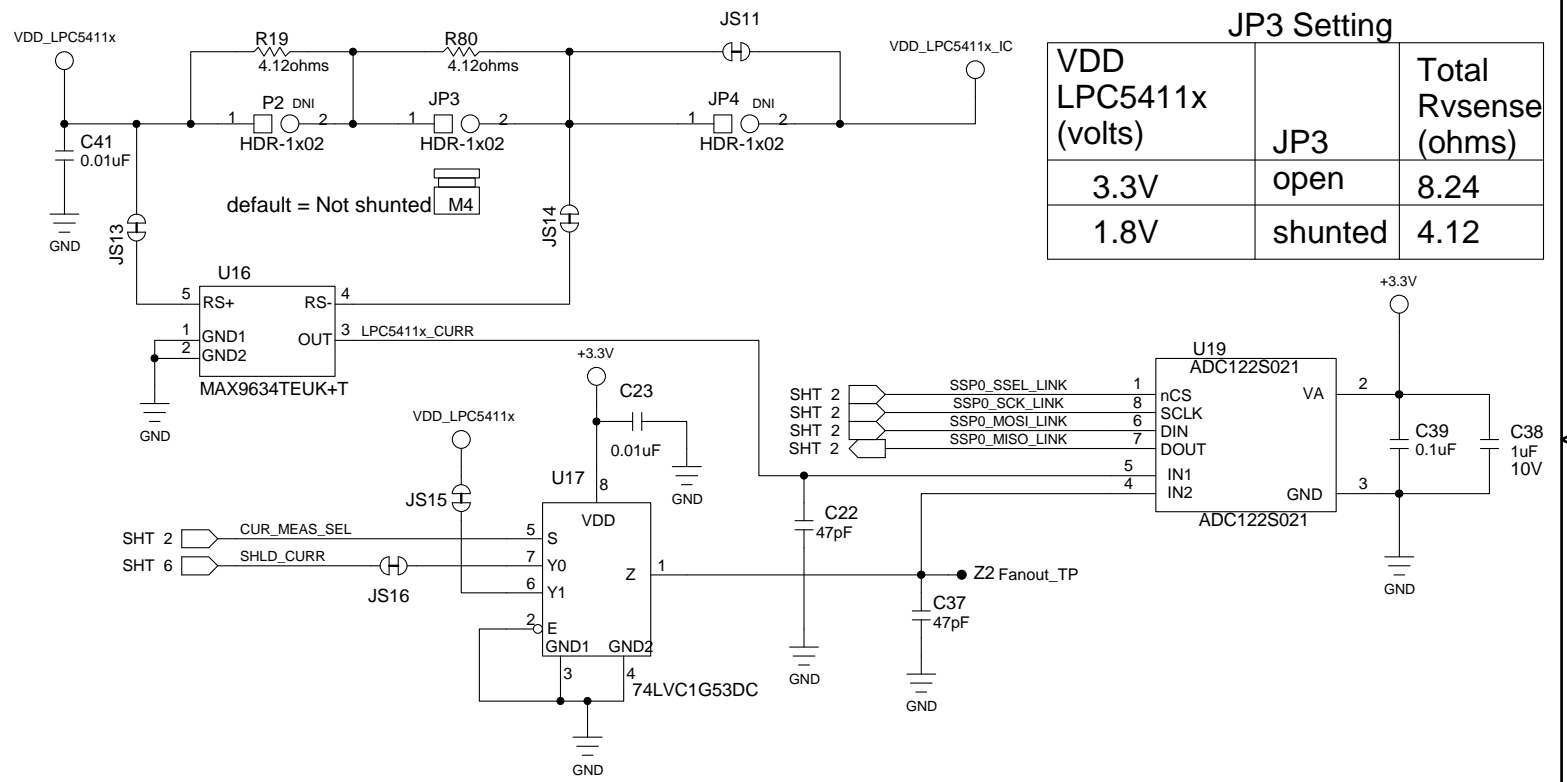


CONTRACT NO.		Link2 LPC43xx Peripheral	
APPROVALS	DATE	NXP Semiconductors	
DRAWN d.consiglio	4/21/2015	411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
CHECKED		SIZE/FSCM NO.	DWG. NO.
ISSUED	05/06/15	D	LPCX5411x QFP64 A1
		SCALE	SHEET 2 OF 06



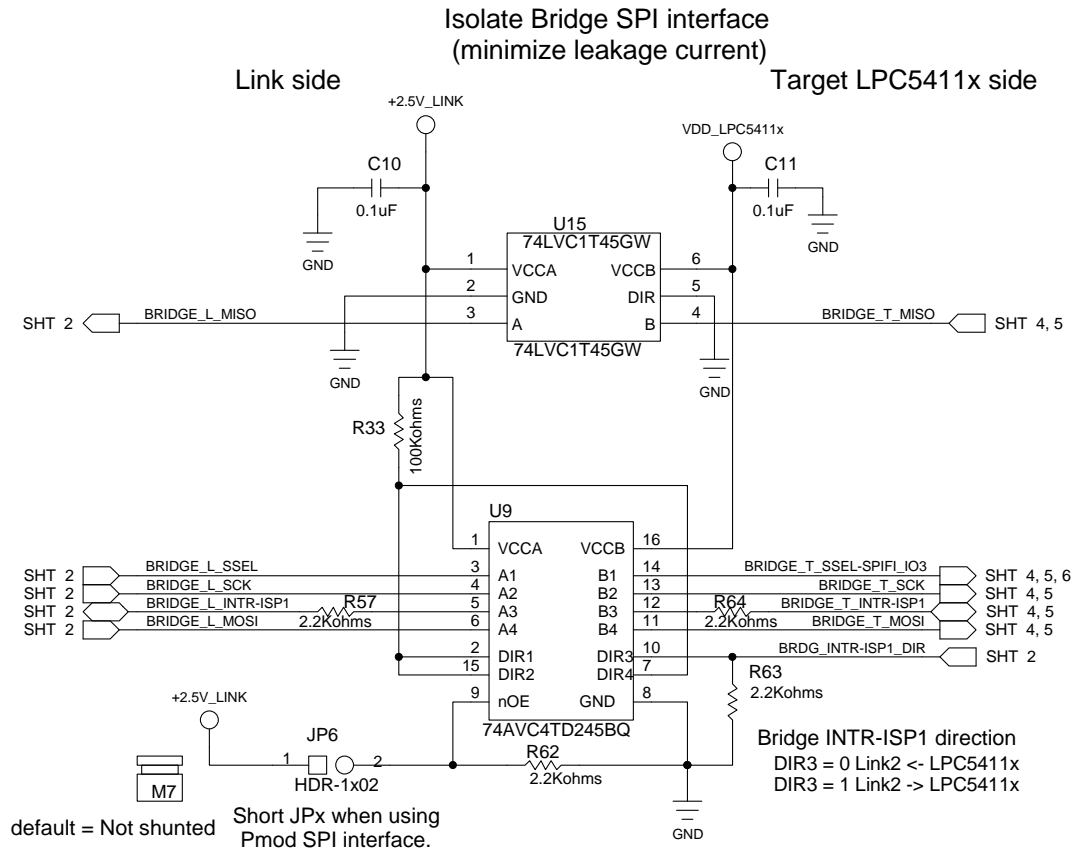
LPC5411x Current measurement				ADC111S021 12bit ADC	
LPC5411x				ADC111S021 12bit ADC	
Vsense (1) voltage 1-lsb	JP3 open LPC5411x Current 1-lsb	JP3 shunted LPC5411x Current 1-lsb	maximum current	ADC input 1-lsb 800uV	
32uV	3.88uA	7.77uA	16mA		

(1) Vsense voltage is between U16 RS+ to RS-. Total Rvsense = R19 + (JS10 || JP3).



JP3 Setting

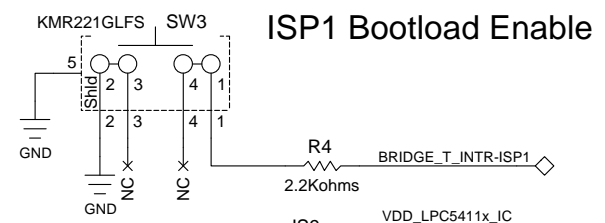
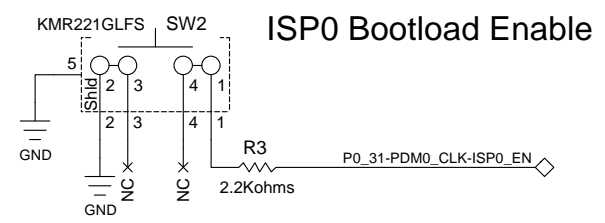
VDD LPC5411x (volts)	JP3	Total Rvsense (ohms)
3.3V	open	8.24
1.8V	shunted	4.12



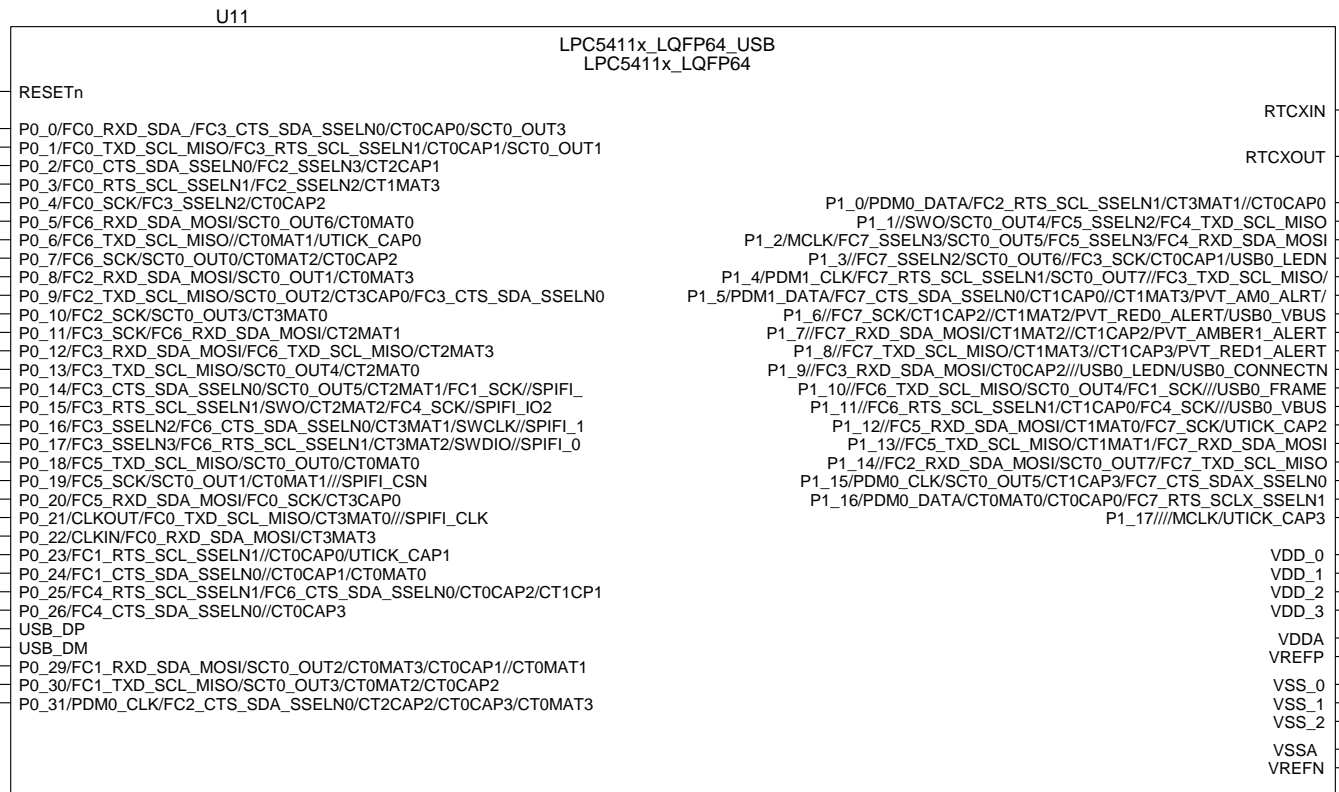
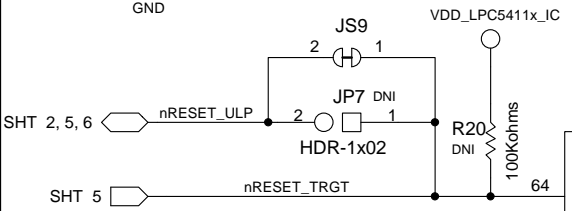
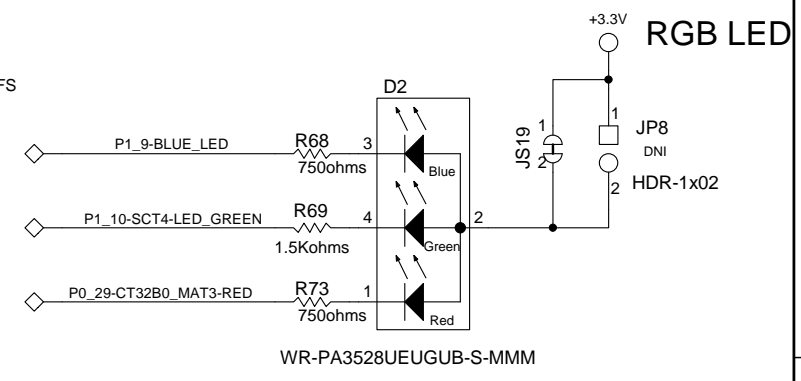
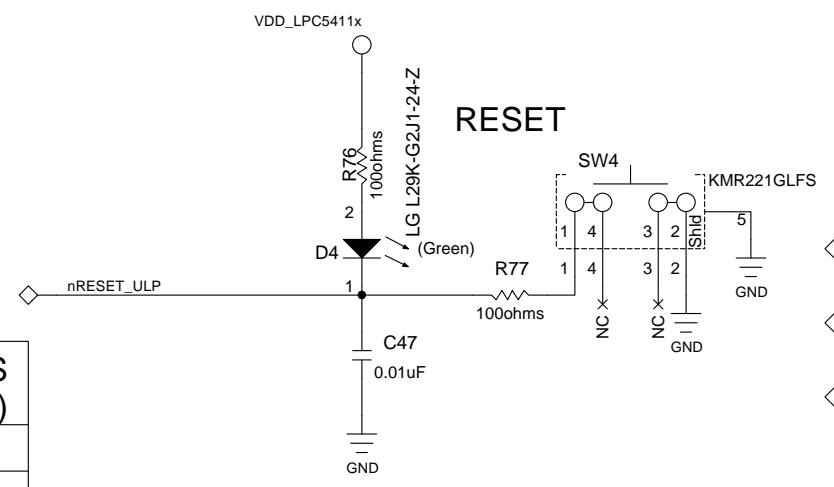
Bridge INTR-ISP1 direction
 DIR3 = 0 Link2 <- LPC5411x
 DIR3 = 1 Link2 -> LPC5411x

APPROVALS		DATE	LPC5411x current measurement; Link2 SPI isolation transceiver		
DRAWN	d.consiglio	5/6/2015	NXP Semiconductors		
CHECKED			411 E. Plumeria Dr		
ISSUED		05/06/15	San Jose, CA 95134		
			www.standardics.nxp.com/microcontrollers/		
			SIZE	FSCM NO.	DWG. NO.
			D		LPCX5411x QFP64 A1
			SCALE		SHEET 3 OF 06

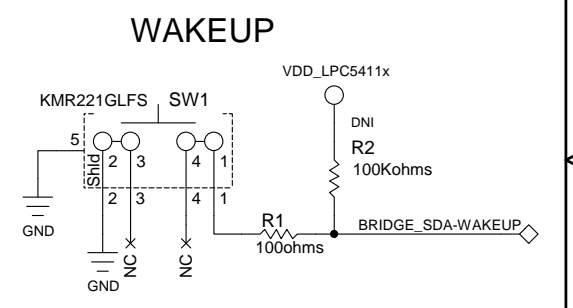
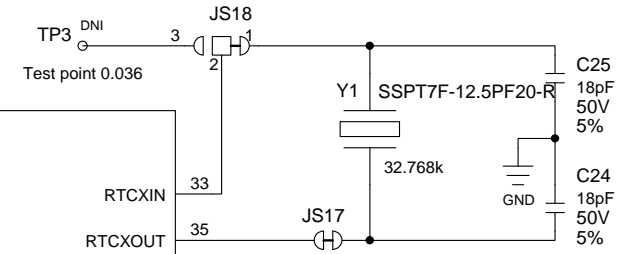
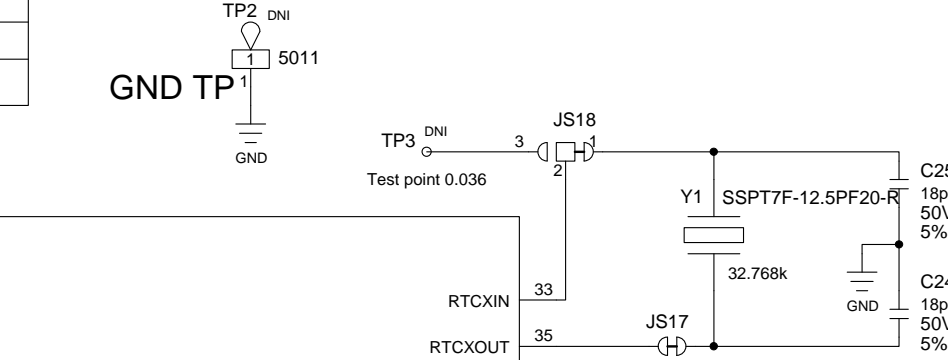
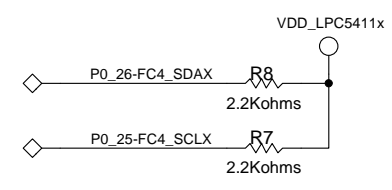
REVISIONS		DATE	APPROVED
REV	DESCRIPTION		



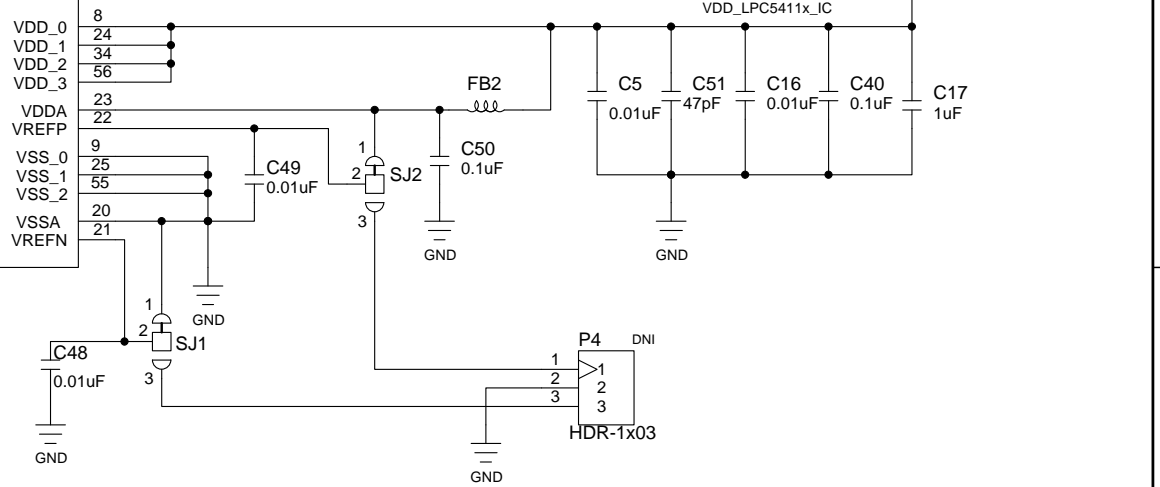
Boot Modes	ISP0 (P0.31)	ISP1 (P0.4)	VBUS (P1.6)
I2C/SPI boot	0	0	X
UART boot	0	1	0
USB MSC boot	0	1	1
FLASH boot	1	X	X



SHT	Pin	Signal	Pin	Signal
SHT 2, 5, 6	1	nRESET_ULP	64	RESETn
SHT 5	2	nRESET_TRGT	31	P0_0/FC0_RXD_SDA /FC3_CTS_SDA_SSELN0/CT0CAP0/SCT0_OUT3
SHT 2	3	TO_MUX_P0_0-ISP_RX	32	P0_1/FC0_TXD_SCL_MISO/FC3_RTS_SCL_SSELN1/CT0CAP1/SCT0_OUT1
SHT 2, 5	4	P0_1-ISP_TX	36	P0_2/FC0_CTS_SDA_SSELN0/FC2_SSELN3/CT2CAP1
SHT 6	5	P0_2-GPIO_SPI_CS	37	P0_3/FC0_RTS_SCL_SSELN1/FC2_SSELN2/CT1MAT3
SHT 6	6	P0_3-GPIO_SPI_CS	38	BRIDGE_T_INTR-ISP1
SHT 3, 5	7	BRIDGE_T_INTR-ISP1	39	P0_4/FC0_SCK/FC3_SSELN2/CT0CAP2
SHT 6	8	P0_5-FC6_RXD_SDA_MOSI_DATA	40	P0_5/FC6_RXD_SDA_MOSI/SCT0_OUT6/CT0MAT0
SHT 6	9	P0_6-FC6_TXD_SCL_MISO_FRAME	41	P0_6/FC6_TXD_SCL_MISO/CT0MAT1/UTICK_CAP0
SHT 6	10	P0_7-FC6_SCK	43	P0_7/FC6_SCK/SCT0_OUT0/CT0MAT2/CT0CAP2
SHT 6	11	P0_8-FC2_RXD_SDA_MOSI	44	P0_8/FC2_RXD_SDA_MOSI/SCT0_OUT1/CT0MAT3
SHT 6	12	P0_9-FC2_TXD_SCL_MISO	45	P0_9/FC2_TXD_SCL_MISO/SCT0_OUT2/CT3CAP0/FC3_CTS_SDA_SSELN0
SHT 6	13	P0_10-FC2_SCK-CT32B3_MAT0	46	P0_10/FC2_SCK/SCT0_OUT3/CT3MAT0
SHT 3, 5	14	BRIDGE_T_SCK	47	P0_11/FC3_SCK/FC6_RXD_SDA_MOSI/CT2MAT1
SHT 3, 5	15	BRIDGE_T_MOSI	48	P0_12/FC3_RXD_SDA_MOSI/FC6_TXD_SCL_MISO/CT2MAT3
SHT 3, 5	16	BRIDGE_T_MISO	49	P0_13/FC3_TXD_SCL_MISO/SCT0_OUT4/CT2MAT0
SHT 3, 5, 6	17	BRIDGE_T_SSEL-SPIFI_IO3	50	P0_14/FC3_CTS_SDA_SSELN0/SCT0_OUT5/CT2MAT1/FC1_SCK/SPIFI_
SHT 2, 6	18	TDO-SWO_TRGT-SPIFI_IO2	52	P0_15/FC3_RTS_SCL_SSELN1/SWO/CT2MAT2/FC4_SCK/SPIFI_IO2
SHT 2, 6	19	TCK-SWDCLK_TRGT-SPIFI_IO1	53	P0_16/FC3_SSELN2/FC6_CTS_SDA_SSELN0/CT3MAT1/SWCLK/SPIFI_1
SHT 2, 6	20	IF_TMS_SWDIO-SPIFI_IO0	58	P0_17/FC3_SSELN3/FC6_RTS_SCL_SSELN1/CT3MAT2/SWDIO/SPIFI_0
SHT 2, 6	21	P0_18-FC5_TXD_SCL_MISO	59	P0_18/FC5_TXD_SCL_MISO/SCT0_OUT0/CT0MAT0
SHT 2, 6	22	P0_19-FC5_SCK-SPIFI_CSn	60	P0_19/FC5_SCK/SCT0_OUT1/CT0MAT1/SPIFI_CSN
SHT 2, 6	23	P0_20-FC5_RXD_SDA_MOSI	61	P0_20/FC5_RXD_SDA_MOSI/FC0_SCK/CT3CAP0
SHT 2, 6	24	P0_21-CLKOUT-SPIFI_CLK	63	P0_21/CLKOUT/FC0_TXD_SCL_MISO/CT3MAT0/SPIFI_CLK
SHT 2, 6	25	P0_22-BRIDGE_GPIO	63	P0_22/CLKIN/FC0_RXD_SDA_MOSI/CT3MAT3
SHT 1, 5	26	BRIDGE_SCL	1	P0_23/FC1_RTS_SCL_SSELN1/CT0CAP0/UTICK_CAP1
SHT 1, 5	27	BRIDGE_SDA-WAKEUP	2	P0_24/FC1_CTS_SDA_SSELN0/CT0CAP1/CT0MAT0
SHT 1, 5	28	P0_25-FC4_SCLX	3	P0_25/FC4_RTS_SCL_SSELN1/FC6_CTS_SDA_SSELN0/CT0CAP2/CT1CP1
SHT 5, 6	29	P0_26-FC4_SDAX	4	P0_26/FC4_CTS_SDA_SSELN0/CT0CAP3
SHT 5, 6	30	USB_DP	5	USB_DM
SHT 3	31	USB_DM	6	USB_DM
SHT 3	32	P0_29-CT32B0_MAT3-RED	11	P0_29/FC1_RXD_SDA_MOSI/SCT0_OUT2/CT0MAT3/CT0CAP1/CT0MAT1
SHT 6	33	P0_30-ADC1	12	P0_30/FC1_TXD_SCL_MISO/SCT0_OUT3/CT0MAT2/CT0CAP2
SHT 2, 5, 6	34	P0_31-PDM0_CLK-ISP0_EN	13	P0_31/PDM0_CLK/FC2_CTS_SDA_SSELN0/CT2CAP2/CT0CAP3/CT0MAT3



Pin	Signal	SHT
14	P1_0-PDM0_DATA/FC2_RTS_SCL_SSELN1/CT3MAT1/CT0CAP0	SHT 6
15	P1_1/SWO/SCT0_OUT4/FC5_SSELN2/FC4_TXD_SCL_MISO	SHT 6
16	P1_2/MCLK/FC7_SSELN3/SCT0_OUT5/FC5_SSELN3/FC4_RXD_SDA_MOSI	SHT 6
17	P1_3/FC7_SSELN2/SCT0_OUT6/FC3_SCK/CT0CAP1/USB0_LEDN	SHT 6
18	P1_4/PDM1_CLK/FC7_RTS_SCL_SSELN1/SCT0_OUT7/FC3_TXD_SCL_MISO	SHT 6
19	P1_5/PDM1_DATA/FC7_CTS_SDA_SSELN0/CT1CAP0/CT1MAT3/PVT_AMO_ALERT/	SHT 6
26	P1_6/FC7_SCK/CT1CAP2/CT1MAT2/PVT_RED0_ALERT/USB0_VBUS	SHT 3, 6
27	P1_7/FC7_RXD_SDA_MOSI/CT1CAP2/PVT_AMBER1_ALERT	SHT 6
28	P1_8/FC7_TXD_SCL_MISO/CT1MAT3/CT1CAP3/PVT_RED1_ALERT	SHT 6
29	P1_9/FC3_RXD_SDA_MOSI/CT0CAP2/USB0_LEDN/USB0_CONNECTN	SHT 6
30	P1_10/FC6_TXD_SCL_MISO/SCT0_OUT4/FC1_SCK/USB0_FRAME	SHT 6
42	P1_11/FC6_RTS_SCL_SSELN1/CT1CAP0/FC4_SCK/USB0_VBUS	SHT 6
51	P1_12/FC5_RXD_SDA_MOSI/CT1MAT0/FC7_SCK/UTICK_CAP2	SHT 6
54	P1_13/FC5_TXD_SCL_MISO/CT1MAT1/FC7_RXD_SDA_MOSI	SHT 6
57	P1_14/FC2_RXD_SDA_MOSI/SCT0_OUT7/FC7_TXD_SCL_MISO	SHT 6
62	P1_15-SCT05-FC7_CTS	SHT 6
7	P1_16-CT32B0_MAT0-GYRO_INT1	SHT 6
10	P1_17-IR_LEARN_EN	SHT 6



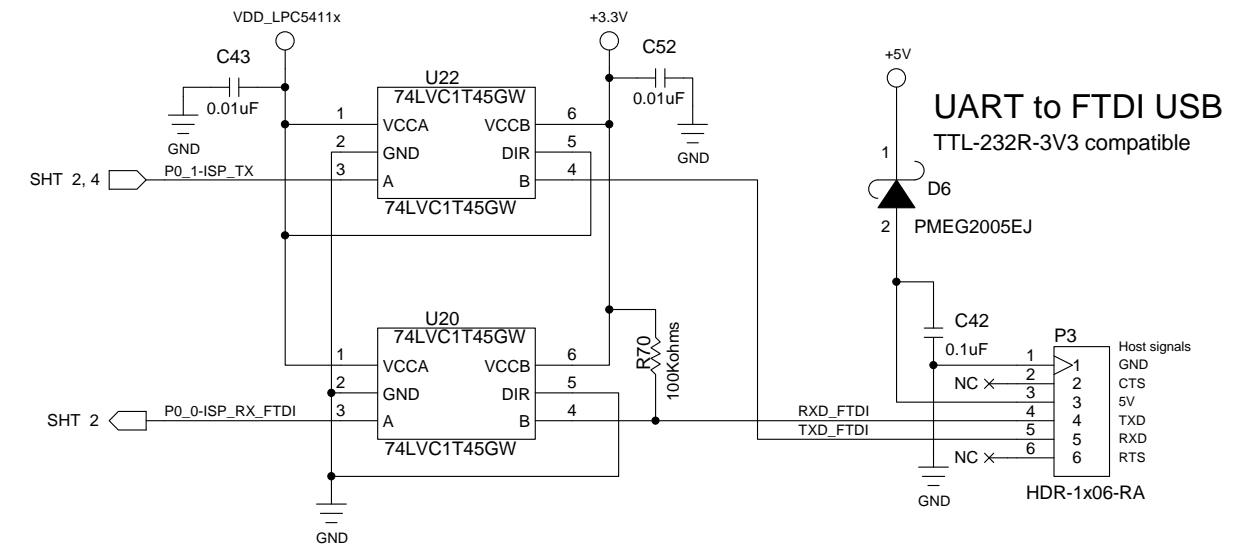
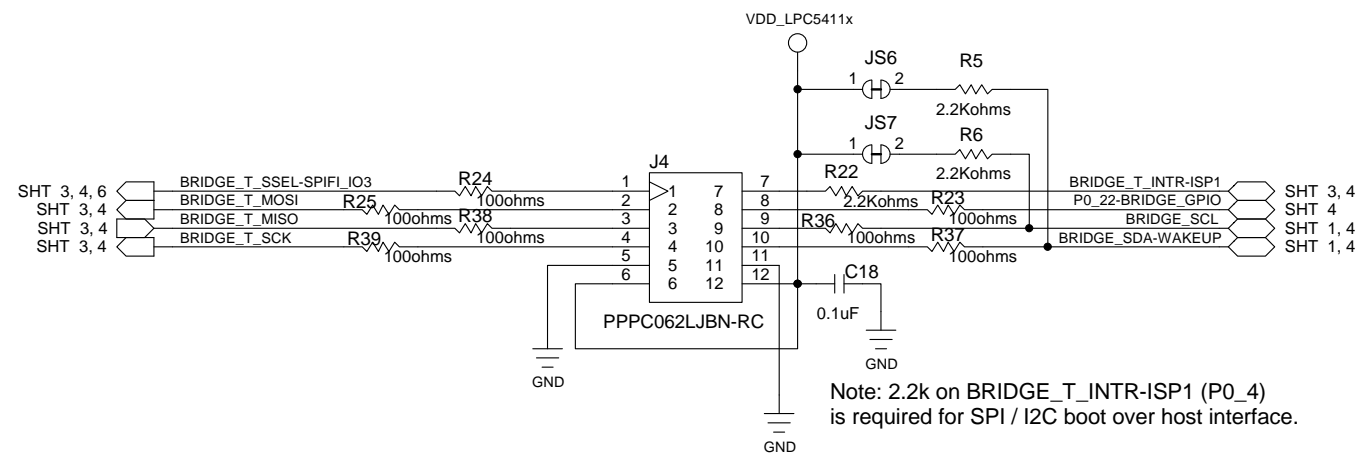
CONTRACT NO.		Target LPC5411x LQFP64	
APPROVALS	DATE	NXP Semiconductors	
DRAWN d.consiglio	4/21/2015	411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
CHECKED		SIZE	DWG. NO.
ISSUED	05/06/15	D	LPCX5411x QFP64
		SCALE	REV A1
			SHEET 4 OF 06

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REV	DESCRIPTION	DATE	APPROVED

LPC5411x AP control port
(AP must drive open-drain)

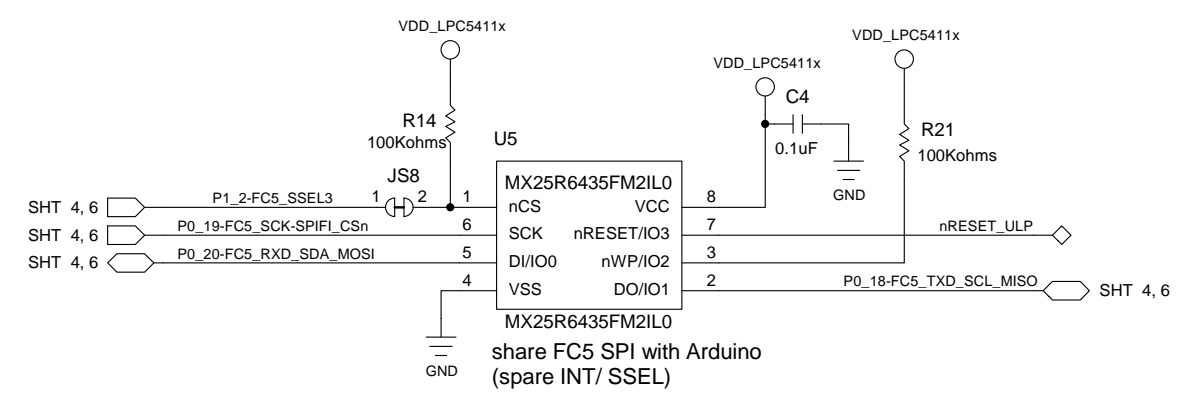
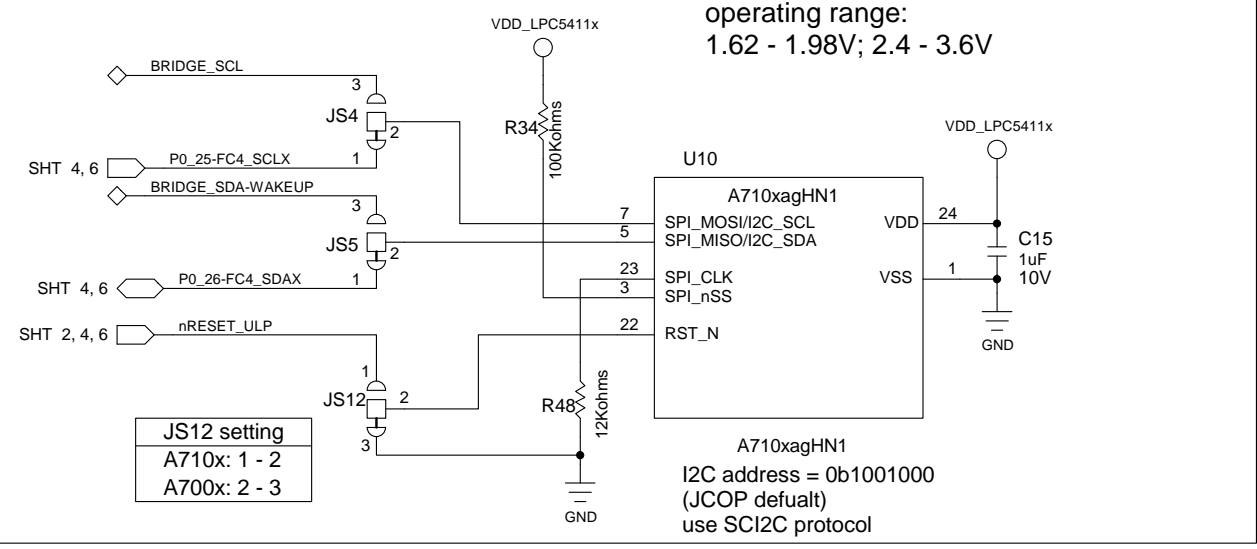


SPI / I2C bridge header (Pmod compatible)



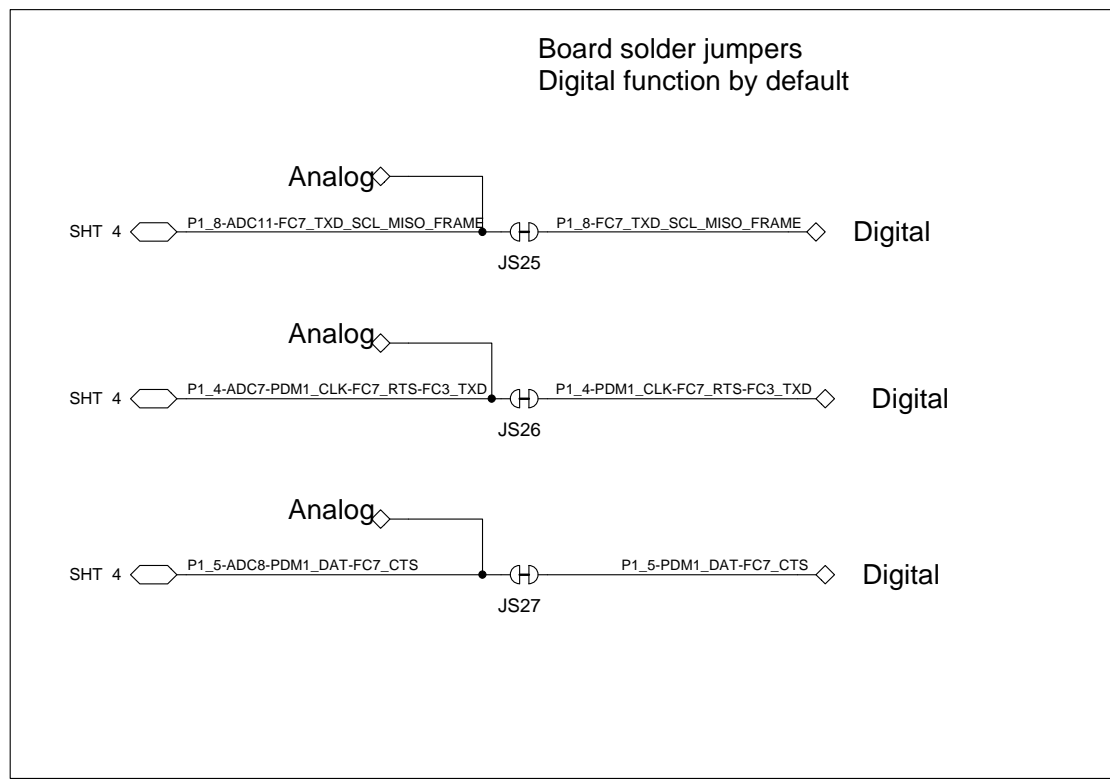
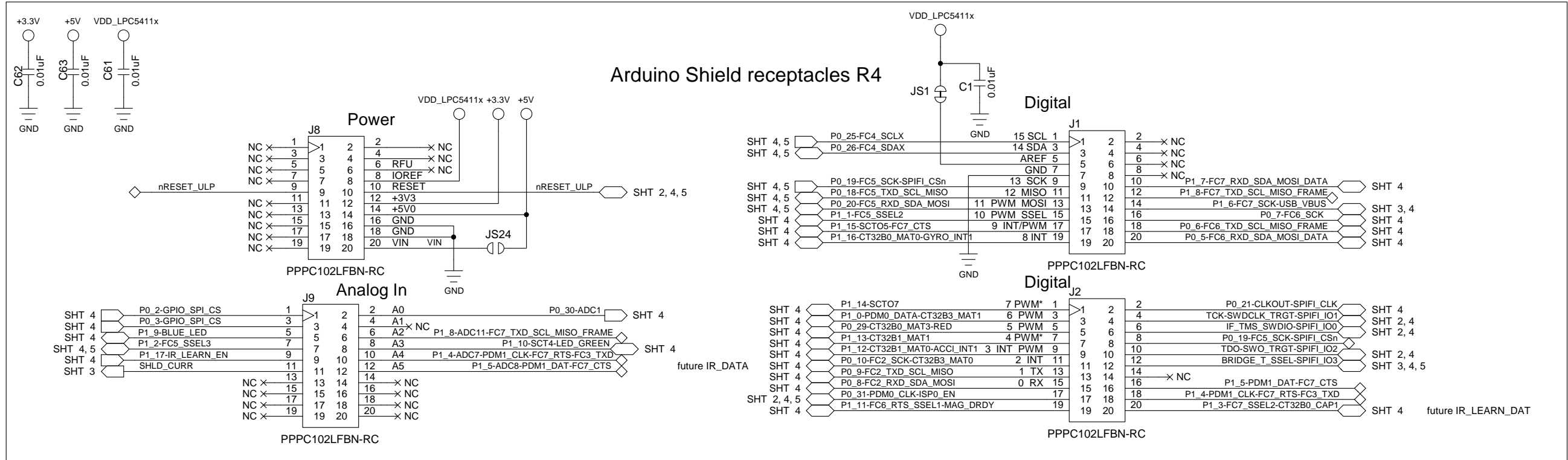
NXP A700x / A71x secure MCU

operating range:
1.62 - 1.98V; 2.4 - 3.6V



CONTRACT NO.		Pmod / FTDI / SecElem / SPI Flash	
APPROVALS	DATE	NXP Semiconductors	
DRAWN d.consiglio	4/21/2015	411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
CHECKED		SIZE	DWG. NO.
ISSUED	05/06/15	D	LPCX5411x QFP64 A1
SCALE		SHEET 5 OF 06	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



CONTRACT NO.		Arduino Interface		
APPROVALS	DATE	NXP Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/		
DRAWN	d.consiglio			4/21/2015
CHECKED				
ISSUED	05/06/15	SIZE	D	
		FSCM NO.		
		DWG. NO.	LPCX5411x QFP64	
		REV	A1	
		SCALE	SHEET 6 OF 06	