

1 General description

The PF5300, PF5301 and PF5302 integrate high-performance buck converters, 12 A, 8 A, and 15 A, respectively, to power high-end automotive and industrial processors. With adaptive voltage positioning and a high bandwidth loop, they offer excellent transient regulation to minimize capacitor requirements.

Clock synchronization and spread-spectrum features reduce EMC issues in the system. The PF5300/PF5301/PF5302 can operate as stand-alone point-of-load regulator ICs or as companion chips to a larger PMIC.

2 Features and benefits

- Low Rdson Internal FETs
- 2.2 MHz switching frequency
- Dynamic Voltage Scaling
- Programmable AVP (droop)
- XFAILB interface for synchronization with NXP PF-PMICs
- Over temperature protection
- I2C Interface for monitoring and control
- Watchdog Timer

3 Applications

- Gateway
- Infotainment / Cluster / Driver Awareness
- Telematics
- V2X
- Radar
- Vision
- ADAS
- Sensor fusion



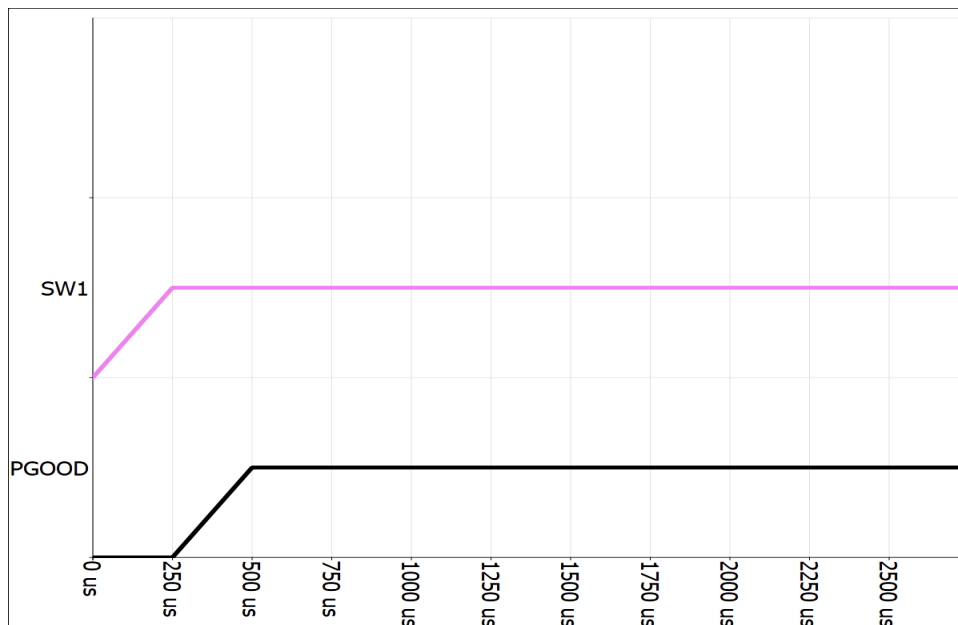
4 Ordering information

Table 1. Ordering information

| Type number ^[1] | Package | | |
|----------------------------|--------------|--|-----------------|
| | Name | Description | Version |
| MPF5300AMMAMES | H-FC-PQFN-24 | No leads, step-cut wettable flank, plastic thermal enhanced very thin quad flat pack; 24 terminals, 0.5 mm pitch, 4.5 mm x 3.5 mm x 0.75 mm body | SOT2090 - 1(SC) |

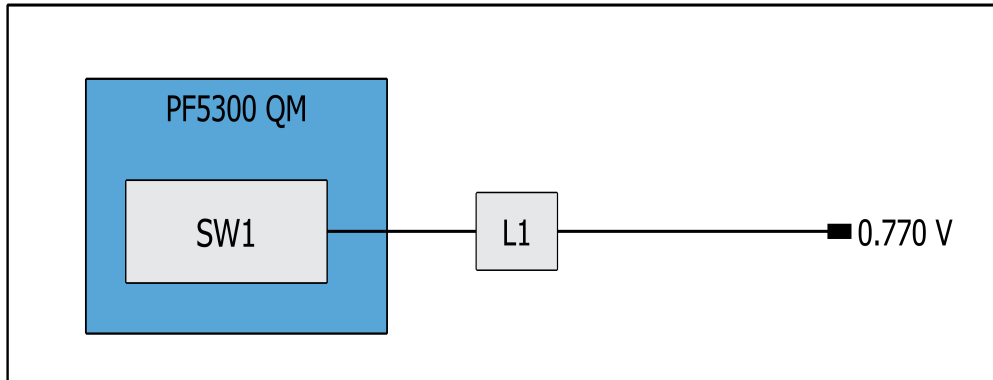
[1] To order parts in tape and reel, add the R2 suffix to the part number.

5 Power-up sequence summary



The signals depicted above are enable signals for each regulator. They don't represent the actual ramp voltage.

6 Hardware configuration diagram



7 OTP configuration

See PF5300 datasheet for parametric details. The OTP configuration summary for AM sequence ID is provided in Tables below.

Table 2. Device OTP configuration

| Functional block | Feature | OTP selection |
|----------------------|-----------------------|---------------------------|
| System Configuration | I2C Address | 0x29 |
| | Maximum Fault Counter | 15 Faults |
| I/O Configuration | Standby Polarity | Standby pin is logic High |
| | Standby Delay | No delay |
| | XFAIL Operation | Disabled |
| | ULP OFF Control | Goto ULPOFF at turn off |

Configuration report for QM OTP program ID: AM rev A

| | | |
|------------------|-----------------------------|-----------------------|
| Clock Management | Nominal Switching Frequency | 18 MHz |
| | SYNCIN Range | 2000 kHz to 3000 kHz |
| | Frequency Spread Spectrum | Enabled |
| | FSS Select | Triangular Modulation |
| | SYNCIN Mode | STANDBY input |
| | SW1 PLL Enable | SW PLL is enabled |

Table 3. Power Sequencer configuration

| Functional block | Feature | OTP selection |
|-------------------|-----------------------|---------------|
| Power Up Sequence | Sequence Time Base | 250 us |
| | SW1 Sequence Slot | Slot 0 |
| | PGOOD Sequence Slot | Slot 1 |
| | Post Power Down Delay | 0 ms |
| | Turn Off Delay | 0 us |

Table 4. SW Regulator configuration

| Functional block | Feature | OTP selection |
|------------------|------------------------|------------------------|
| SW1 | SW1 Output Voltage | 0.770 V |
| | SW1 Standby Voltage | 0.770 V |
| | SW1 Output Inductor | 100 nH |
| | SW1 Discharge Resistor | PD resistor discharged |
| | SW1 Soft Start | 8 mV/us |

Configuration report for QM OTP program ID: AM rev A

| | | |
|------------------|-----------------------------|--|
| | SW1 AVP | 0 mV/A (disabled) |
| | SW1 AVP Filter | 238 kHz |
| | SW1 Run Mode | PWM Mode |
| | SW1 Standby Mode | OFF |
| | SW1 Diode Emulation | Disable diode emulation |
| | SW1 Diode Braking Threshold | 5.0 mV |
| | SW1 HIZ OFF | SW1 is actively discharged |
| | SW1 Discharge | 8 mV/us |
| | SW1 DVS MAX | 1.200 V |
| | SW1 DVS MIN | 0.500 V |
| | SW1 TON Dominant | Disable |
| | SW1 TON Slave | Disable |
| SW1 State | SW1 OV Bypass | No impact due to SW1 OV on fault counter |
| | SW1 UV Bypass | No impact due to SW1 UV on fault counter |
| | SW1 ILIM Bypass | No impact due to SW1 ILIM on fault counter |
| VMON and PGOOD | VMON Overvoltage Threshold | 105.0 % |
| | VMON Undervoltage Threshold | 95.0 % |
| | VMON OV Debounce | 5 us |
| | VMON UV Debounce | 5 us |
| | PGOOD SW1 OV | No PGOOD assertion |
| | PGOOD SW1 UV | No PGOOD assertion |
| SW1 Compensation | SW1 Gain Margin | 113 us |
| | SW1 Compensation Resistor | 174 kOhm |
| | SW1 Compensation Capacitor | 25 pF |

Configuration report for QM OTP program ID: AM rev A

Table 5. Program ID

| Functional block | Feature | OTP selection |
|------------------|-----------------|---------------|
| Program ID | Program ID High | A |
| | Program ID Low | M |

8 Legal information

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