NOTES (UNLESS OTHERWISE SPECIFIED):

1. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-6012 CLASS 2 (LATEST REVISION).

2. THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.

3. BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101D-26, 83 or 98
   Tg - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
   Td - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.

4. COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A'

5. CHARACTERISTIC IMPEDANCE - SEE DETAIL 'B'

6. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE 4.00 mils / 3.00 mils

7. PLATING FINISH: A. BOTH SIDES ENIG: TO MEET THE REQUIREMENTS OF IPC-4552 (LATEST REVISION).

8. ALL THROUGH HOLE VIAS MAY BE PLATED SHUT.

9. SOLDERMASK - TO MEET THE REQUIREMENTS OF IPC-SM-840E (OR LATEST REVISION).
   GREEN COLOR, BOTH SIDES. MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM NXP.
   TYPE: LDI - OR EQUIVALENT.
   A. LOCATION = +/-.001" OF PLATED PADS.
   B. DIAMETER OR SIZE = +/-.001 OF ORIGINAL DATA

10. SILKSCREEN - WHITE EPOXY OR ACRYLIC INK, BOTH SIDES. NO SILKSCREEN ON ANY EXPOSED COPPER FEATURE.

11. ELECTRICAL TEST - 100% IPCD356.

12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.

13. DFM CHECK MUST BE RUN ON BOARD DATA BEFORE BUILDING BOARDS, UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY NXP.

14. TEARDROPS MAY BE ADDED AT THE FAB HOUSE TO ALL SIGNAL LAYERS.

15. TWO SOLDER SAMPLES TO BE PROVIDED.

16. SUPPLIER MARKINGS - ON SECONDARY SIDE ONLY, WHERE SHOWN.
   - MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0

17. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (P6)

18. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)

19. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP. ALL HOLE LOCATION TOLERANCES ARE TO BE +/-.002 IN REFERENCE TO THE PRIMARY DATUM UNLESS OTHERWISE SPECIFIED.

20. FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURERS REQUIREMENTS. THE ADDITION OF RAILS AND .125" NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF CONTRACT MANUFACTURER. PANELIZATION MUST BE APPROVED BY CONTRACT MANUFACTURER.

21. THE MANUFACTURE HAS THE OPTION TO ADD COPPER THIEVING ON OUTER AND INNER LAYERS, KEEP A MINIMUM DISTANCE OF .100" FROM ANY BOARD FEATURES.

22. INTENTIONAL 28 SHORTS AT:

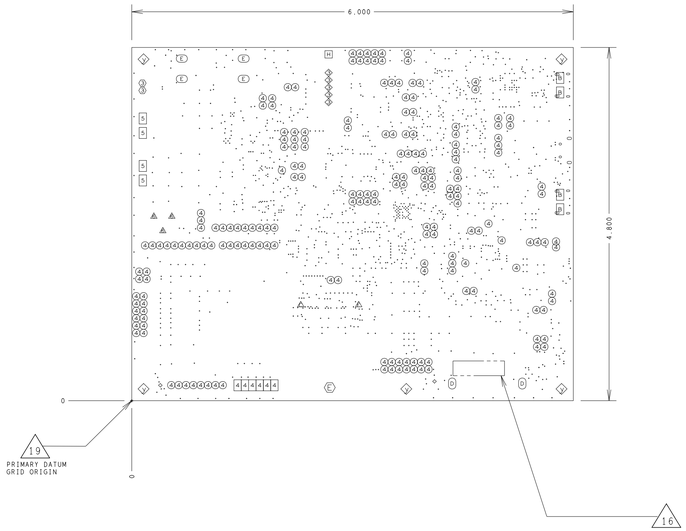
Location	RefDes	Net 1		Net 2
(1780.00 4010.76)	JS2	P1V8_CODEC	&	SW2_OUT
(1907.50 4010.00)	JS3	VDD_CODEC	&	SW2_OUT
(2209.50 3040.00)	JS9	VDD_PMOD	&	VDDIO1
(2209.50 3188.50)	JS7	VDDE_A	&	VDDIO1
(2435.00 4031.26)	SH21	N19798386	&	P0_22
(2435.00 4125.00)	SH20	N19798394	&	P0_23_I2S_DATA_TX
(2435.00 4235.00)	SH18	N19798410	&	P0_25
(2435.00 4181.26)	SH19	N19798402	&	P0_24
(2434.68 4431.26)	SH17	N19798378	&	P0_21
(2702.88 1639.56)	JS12	VDD_MEM	&	SW2_OUT
(2915.00 4250.00)	SH14	P2_26_SWDIO	&	N19799857
(2915.00 4356.26)	SH12	IF_TDO_SWO	&	N19799813
(2915.00 4305.00)	SH13	IF_TCK_SWCLK	&	N19799835
(2915.00 4410.00)	SH11	IF_RST	&	N19799787
(3438.82 3945.00)	SH3	N18526135	&	P0_18_FC2_SCL
(3438.54 4088.00)	SH2	N18526137	&	P0_17_FC2_SDA
(3751.00 4619.00)	JS1	GND	&	IF_DETECT
(3974.78 1765.50)	JS16	VDD_LDO_3V3	&	3V3_OUT_USB1
(4331.50 3028.60)	SH4	VDD_LDO_3V3	&	USB1_VDD3V3
(4427.00 3027.00)	JS8	2V5_OUT	&	+2.5V_LINK
(4645.00 1491.65)	JS14	USDHC_SPWR	&	3V3_OUT
(4614.00 2310.00)	JS11	LDO2_OUT	&	VDD_TARGET
(4980.00 3840.00)	JS5	I2PIO2_0-SDO_D(0)_SDA	&	P0_16_FC2_SDA
(5140.00 3840.00)	JS6	I2PIO2_0-SDO_D(0)_SCL	&	P0_15_FC2_SCL
(5606.38 837.87)	JS15	DCDC_3V3	&	VDD_LDO_3V3
(5596.38 1232.87)	JS17	N18503998	&	NRESET_POR
(5570.00 2810.00)	JS10	5V_SYS	&	+5V
(5710.88 1454.68)	JS13	V_LED	&	VDD_TARGET

23. RESISTORS MUST BE POPULATED PIN 1 TO PIN 2

REF_DES

R132, R300-307, R377-380, R384-398

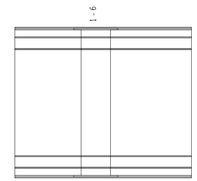
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
		ORIGINAL RELEASE		
	D	JP21, R146 and R147 added	07/01/19	A.Q.
	E	SCHEMATIC CHANGES	10/11/19	R.B.
	E1	DNP CHANGE AND BOARD NAME CHANGE	12/19/19	R.B.
	E2	SOLDERMASK OPENING TO U12.13.17	01/06/20	R.B.
	E3	REV CHANGE - SOLDERMASK FOR E1 BUILD	01/08/20	C.L.



DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	FINISHED_SIZE	TOLERANCE_DRILL	PLATED	QTY
8 △	6.0	+0.0/-6.0	PLATED	66
8 +	8.0	+0.0/-8.0	PLATED	1316
◈	35.0	+2.0/-2.0	PLATED	5
③	36.0	+3.0/-3.0	PLATED	2
④	40.0	+3.0/-3.0	PLATED	193
F	41.0	+3.0/-3.0	PLATED	6
B	51.0	+3.0/-3.0	PLATED	4
A	63.0	+3.0/-3.0	PLATED	3
E	166.0	+3.0/-3.0	PLATED	1
◇	15.0	+2.0/-2.0	NON-PLATED	2
H	31.0	+2.0/-2.0	NON-PLATED	4
△	43.0	+2.0/-2.0	NON-PLATED	1
D	59.0	+2.0/-2.0	NON-PLATED	2
A	63.0	+2.0/-2.0	NON-PLATED	1
E	67.0	+2.0/-2.0	NON-PLATED	4
H	94.0	+2.0/-2.0	NON-PLATED	1
◈	125.0	+2.0/-2.0	NON-PLATED	5
⬭	34.0x26.0	+3.0/-3.0	PLATED	2
⬭	47.0x22.0	+3.0/-3.0	PLATED	4
T	55.0x33.0	+3.0/-3.0	PLATED	4
⬭	59.0x33.0	+3.0/-3.0	PLATED	2

LAYERS	SE		DIFF						
	TRACE WIDTH	IMPEDANCE	TRACE WIDTH	TRACE SPACING	IMPEDANCE	TRACE WIDTH	TRACE SPACING	IMPEDANCE	REFERENCE LAYER
L1_PS	4.50	50.00	4.50	5.00	90.00	4.00	7.00	100.00	2
L3_IN1	4.50	50.00	4.50	5.00	90.00	4.00	7.00	100.00	2,5
L4_IN2	4.50	50.00	4.50	5.00	90.00	4.00	7.00	100.00	2,5
L6_SS	4.50	50.00	4.50	5.00	90.00	4.00	7.00	100.00	5

DETAIL B
IMPEDANCE REQUIREMENTS
IMPEDANCE TOLERANCE IS 10%



DESIGN CROSS SECTION CHART
TOTAL THICKNESS 62.4 MIL
TOLERANCE IS +/- 10%

___ PUBI (PUBLIC INFORMATION)
_X_ NIUO (NXP INTERNAL USE ONLY)
___ NCP (NXP CONFIDENTIAL PROPRIETARY)

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO NXP AND SHALL NOT BE USED FOR ENGINEERING DESIGN PROCUREMENT OR MANUFACTURE IN WHOLE OR IN PART WITHOUT THE CONSENT OF NXP.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES [MM]
TOLERANCES ARE:
DECIMALS ANGLES
.XX .01 .0-30"
.XXX .005
√ RMS ALL MACHINED SURFACES
BREAK ALL SHARP EDGES AND CORNERS. REMOVE BURRS.
UNDERLINED DIM. NOT TO SCALE.
THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.

APPROVALS	DATE
DRAWN DARRELL SLUPEK	01-08-20
CHECKED CLYDE LOVELACE	01-08-20
DESIGN ENGINEER ANTONIO QUIROZ	01-08-20
TEST MIGUEL C.	01-08-20

PART NO. 170-35099

NXP SEMICONDUCTORS
6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA

TITLE: PRINTED WIRING BOARD
MIMXRT685-EVK

SIZE	CAD FILE NAME	DWG. NO.	REV
D	LAY-35099	FAB-35099	E3

SCALE DO NOT SCALE DRAWING SHEET 1 OF 1

ART FILE = FAB.art