

MCIMX93-9x9 package Quick Start Board

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Preliminary - Subject to Change without Notice!

This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with i.MX processors. Although best design practices have been applied, some areas may not be suitable for a mass-production design.

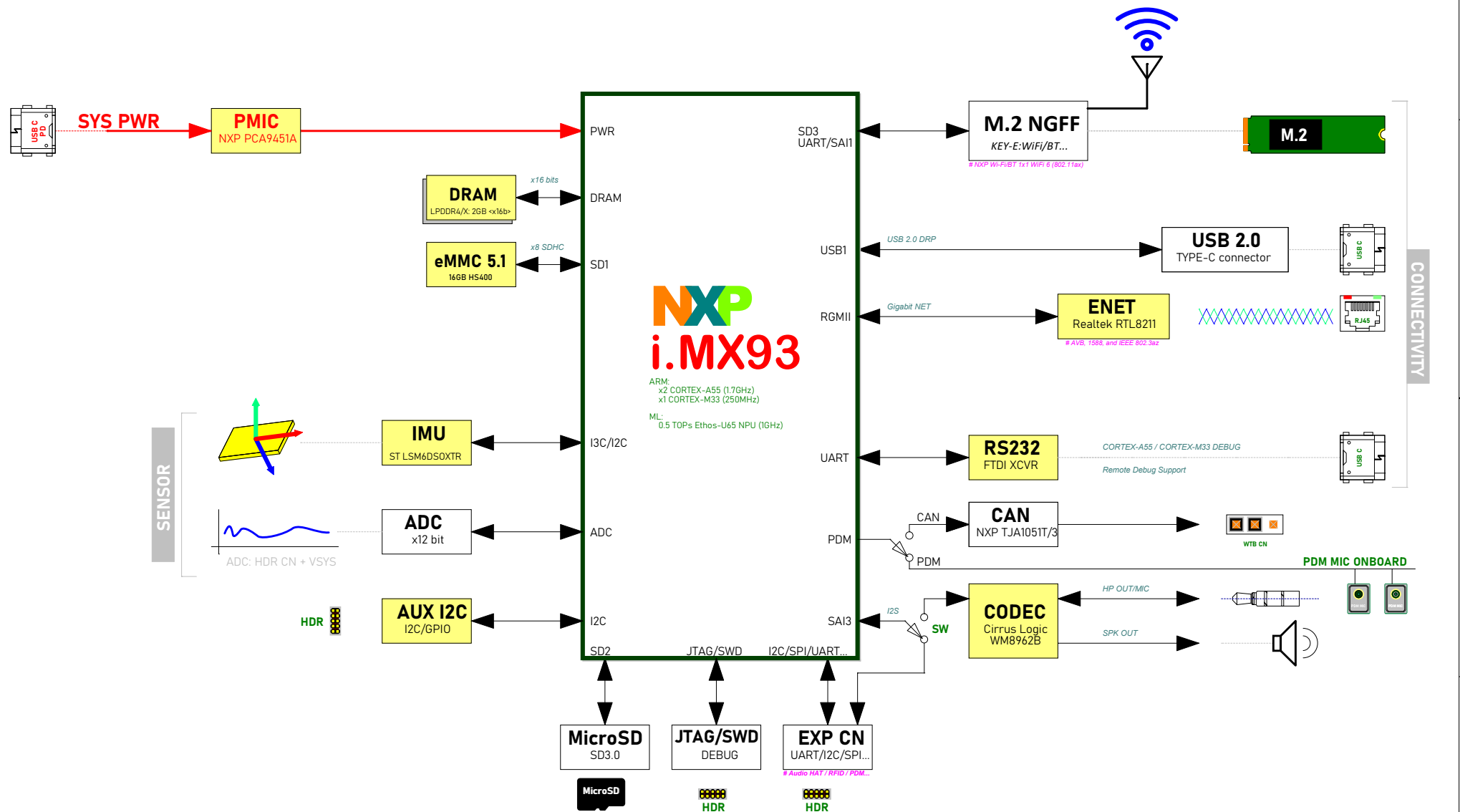
Revision History


MCIMX93-QSB

Rev. Code	Date	By	Description
A	2022-05-06	nxa13729	Initial version
A1	2022-09-01	nxa13729	DNP R1767, chang to 1.8V PU due to USB ID power domain is 1.8V Add R823 as USB TCPC shared interrupt to support level trigger mode Change R812 connected with HP_DET which used as audio jack detection Add R845 connected with AUD_nINT to maintain the SW compatible Add R1822, DNP R1203 as audio jack detection to GPIO IRQ path Add R956,R957 for M.2 compatible design Add U1004,D1011,D1012,R1072,R1073-R1085,C1021-C1024,BT1001,TP1015-TP1021 RTC module circuits Change L503,L504 to 0 OHM R530,R531 Add R958,R959 to use RTC_CLKO Add R1823 Add R745,R748, J1710,J1711, used for Audio Hat Board Remove TP1954, TP1955, TP1956,TP1958 Add R850,R851,R852,R853,R854 for backup DNP R1433,R1434,R1435 Add TEMP Sensor U915. R860,R861,R862,R863,C955,C956 PMIC PN Change from PCA9451 to PCA9451A, delete VLDO3_1V8 DNP C728 ADD R870, R871 for validation Add U908 level shift LSF0102 to replace the level shifter inside PMIC ADD TP218, TP219, TP220,TP221 for validation
A2	2023-06-25	nxa13729	Update U101 symbol for USB ID power domain Change VDD_SOC_0V8 to VDD_SOC_0V85, Remove R870, Add R111,Install C728 Change ADC power rail with more CAP+FB, install C720, change L102 to 1K OHM FB Add R211 to support LPDDR4/X w/ 2CS Add R102 to support 100-ball LPDDR4/X Default use PMIC internal Level shift for I2C1. Take U908 NTS0104GU12 as backup. Install R717,R719, R713,R712 Remove TP1959, Add R858, for GPIO EXP3V3_EN Add C931,C932,C933 for better performance Remove R314, C308. Delect the net of USB_GND_CHASSIS Remove the net name of HPL_ZOBEL Add C1230, C1231 for the power of WM8962. Install R1203 to keep WM8962B GPIO5 PU Change the symbol of GND Testloop: TP1901, TP1905,TP1906 Update J1101, J1708 USB Type C connector to longer pin length (footprint compatible) to improve the reliability of soldering Change R745 to 33ohm for better audio performance Remove J1711 and R748, Add R855 and R856
A3	2023-11-10	nxa13729	Using GPIO(U801.P0_2) to control power EXP_5V to fix LCD flicker issue Change R1420 to 1K (DNP default) due to mid-voltage caused by LSM6DSOXTR internal PD Remove TP1906 Update U101 symbol for pinname change (E10) Change the value of resistors R855 and R856 to 0R Add R360, D302 (DNP default) for USB PWR detection backup Update U502, U503 due to ESD EOL
A4	2024-06-27	-	change C102 from 0.22uF to 1.0uF change U201 DDR from MT53E1G16D1FW-046 AAT:A to MT53E1G16D1ZW-046 AAT:C due to EoF change U404 from SGM8709YN5G to MCP6546T-E/OT due to leakage all changes do not impact layout, this schematic version is paired with layout LAY-54852_A3
A5	2025-06-12	-	update part number of U101 update some design note or typo all changes do not impact layout, this schematic version is paired with layout LAY-54852_A3

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Drawn by: NXP SE	Page Title: Title and Rev History		
Approved: NXP SE	Size C	Document Number SCH-54852 PDF: SPF-54852	Rev A5
Date: Friday, June 13, 2025	Sheet 1	of 23	

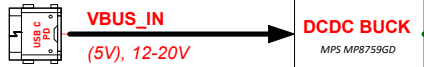
BLOCK DIAGRAM



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i.MX93 EVK PWR TREE

USB C SNK PD



PMIC: PCA9451AHN

SEQ		REGULATOR	VOL (V)	MAX I (mA)
1		LDO1	1.8	10
-				
2	T1	BUCK1/3 DP	0.85	4000
3	T2	LDO4	0.8	200
4				
5	T4	BUCK5	1.8	2000
6	T5	BUCK6	1.1	1500
7	T6	BUCK2	0.6	2000
8	T7	BUCK4	3.3	3000
8	T7	Load Switch	-	400
9	T8	LDO5	1.8/3.3	150
-				
12		POR_B	--	--

SoC: i.MX93

ITEM	PWR RAIL	TYP VOL(V)	REQ I (mA)
1	NVCC_BB5M_1V8	1.8	2
PMIC_ON_REQ			
2	VDD_S0C	DVS	Ref to DS
3	VDD_ANA_0P8	0.8	186
4			
4	VDD_ANA_1P8/NVCC_WAKEUP	1.8	389
5	VDD2_DDR/LPD4 VDDQ	1.1	676
6	VDDQ_DDR (0.6V for LPD4x)	0.6	360
7	NVCC_GPIO/VDD_USB_3P3	3.3	
7	SD_CARD	3.3	
8	NVCC_SD2	1.8/3.3	
-			
POR_B			

LPDDR4/X
VDD1 <1.8V>
VDD2 <1.1V>
VDDQ <0.6V/1.1V>

eMMC
VCCQ <1.8V>
VCC <3.3V>

MicroSD
VCC <3.3V>

Audio CODEC
AVDD/DVDD <3.3V>
SPKVDD <5V>

ETHERNET
DVDD_REG <1.8V>
AVDD/DVDD <3.3V>

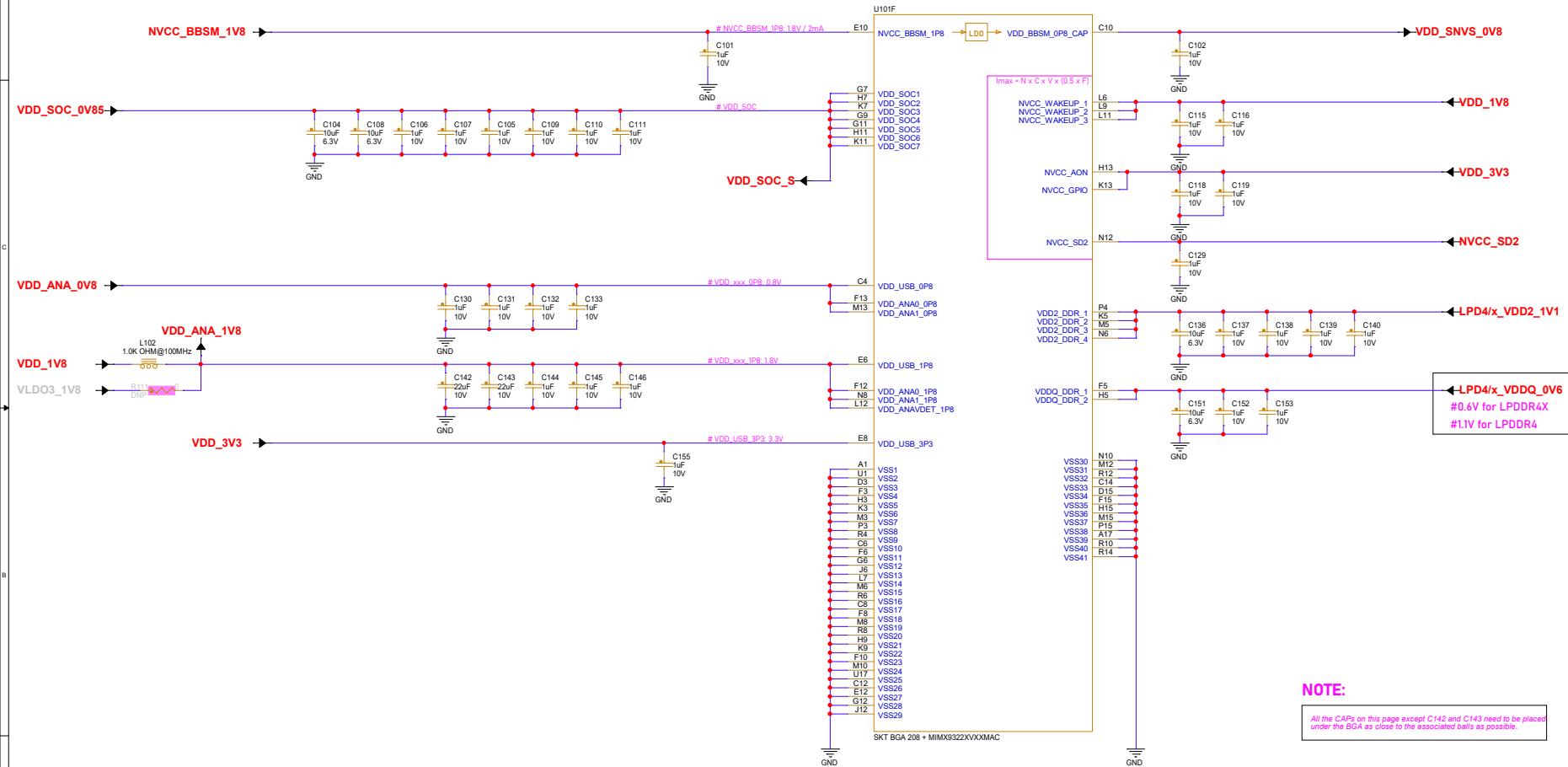
USB C DRP
VBUS <5V>

M.2 KEY-E
3.3V

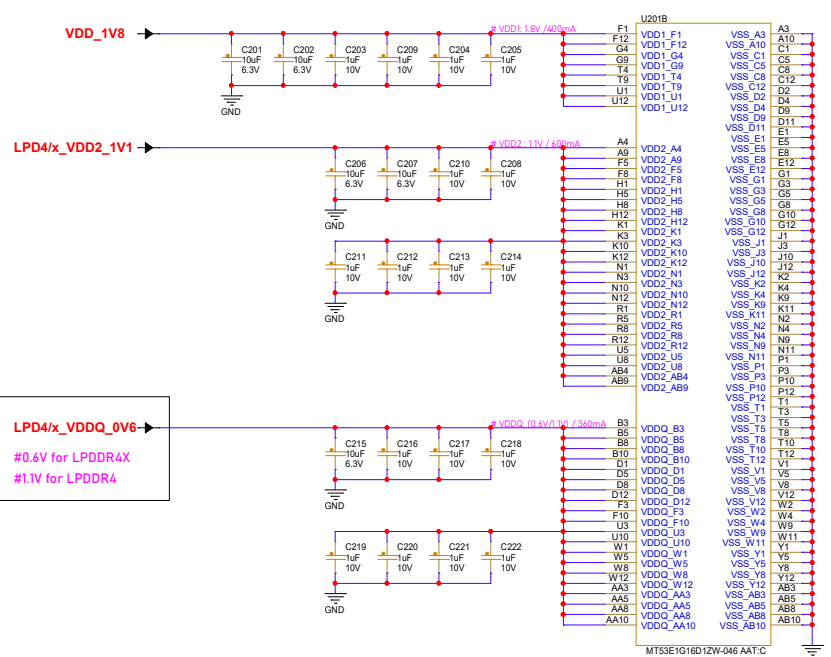
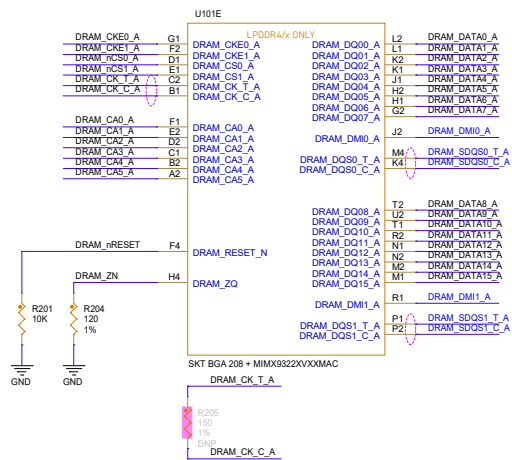
EXPI
3.3V
5V

PDM/CAN
3.3V
5V

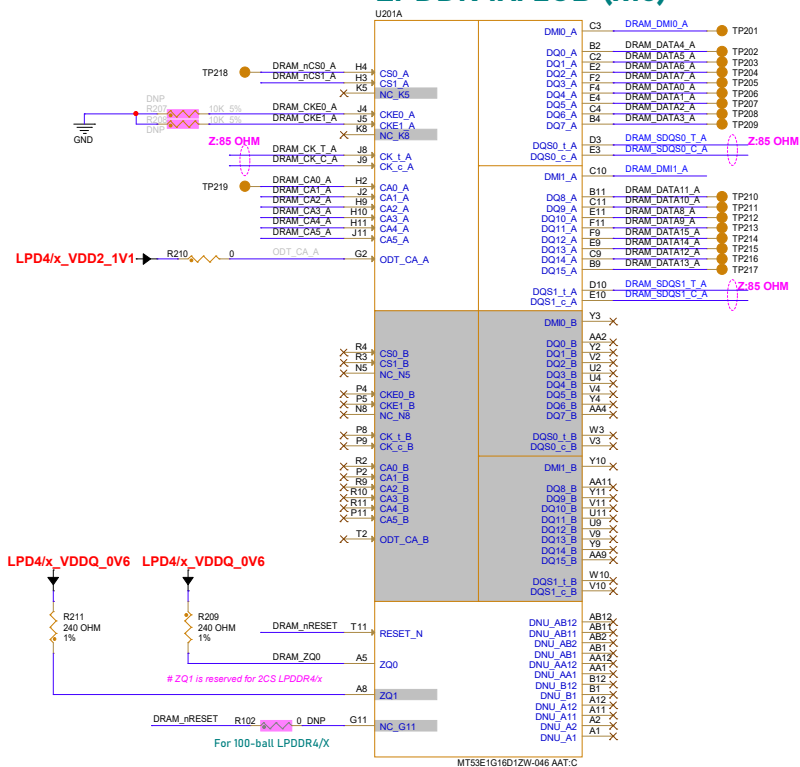
i.MX93 PWR



LPDDR4/X




LPDDR4X: 2GB (x16)



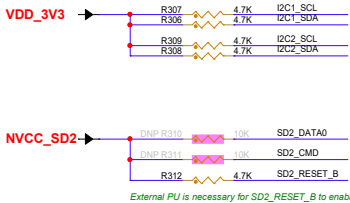
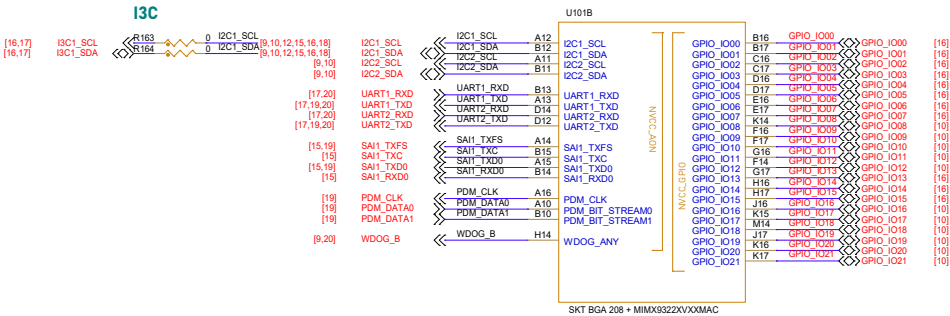
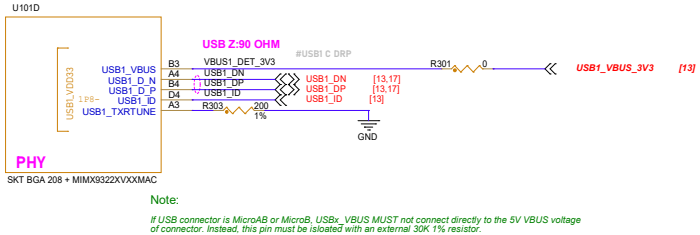
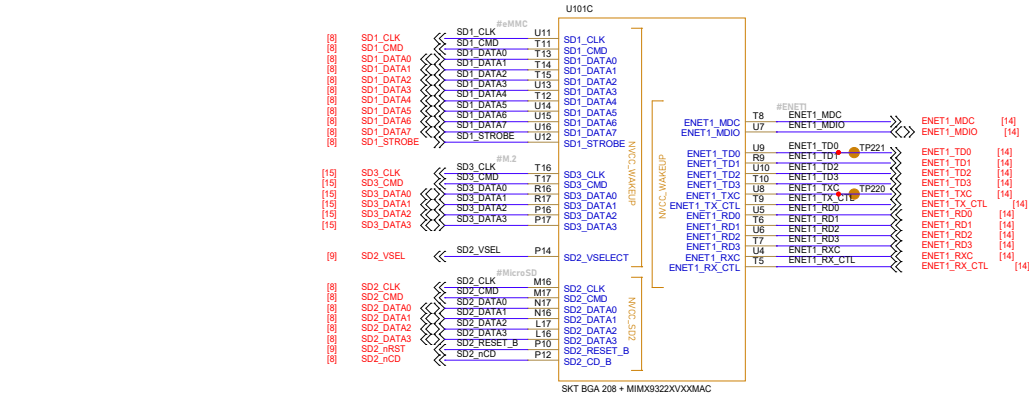
Power Supply Voltage Sequence:

RESET_n is held LOW.
VDD1 >= VDD2
VDD2 >= VDDQ-200mV

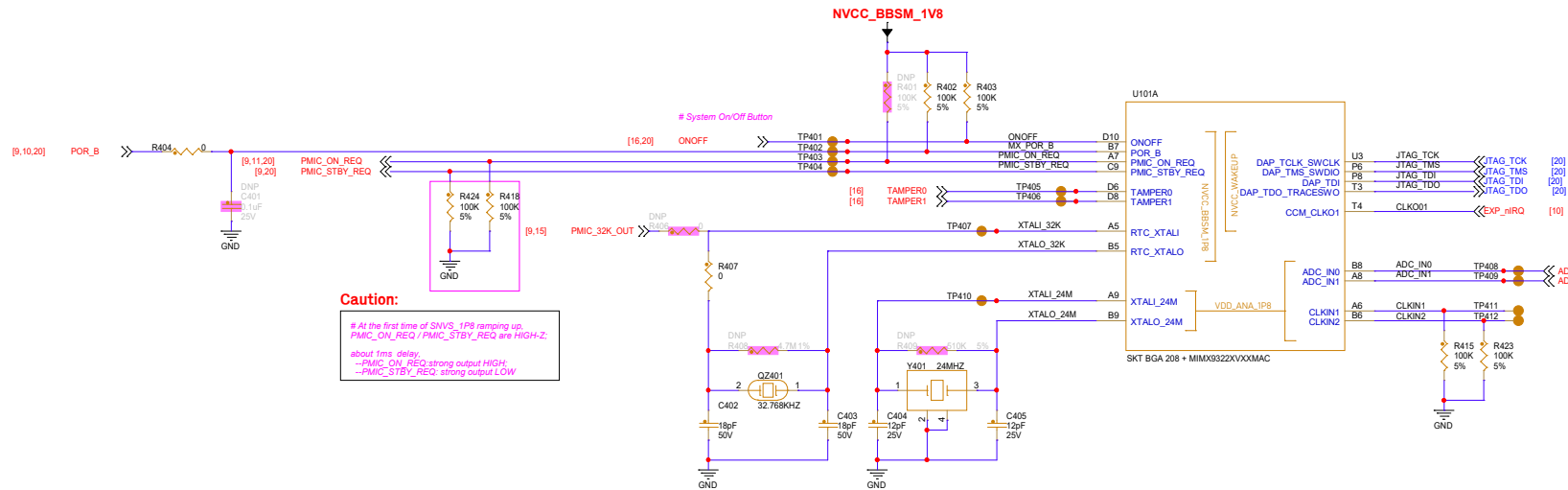
Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.

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Approved: NXP SE		Part C Document Number 5CH-54852 PDF: SPH-54558	
Date: Friday, June 13, 2008		Sheet 6 of 25	
		Rev A5	

i.MX93 IO/PHY

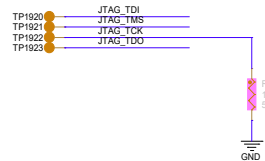


i.MX93 MISC

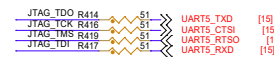


Caution:
At the first time of SNVS_1P8 ramping up,
PMIC_ON_REQ / PMIC_STBY_REQ are HIGH-Z,
about 1ms delay,
--PMIC_ON_REQ strong output HIGH,
--PMIC_STBY_REQ strong output LOW


JTAG/SWD



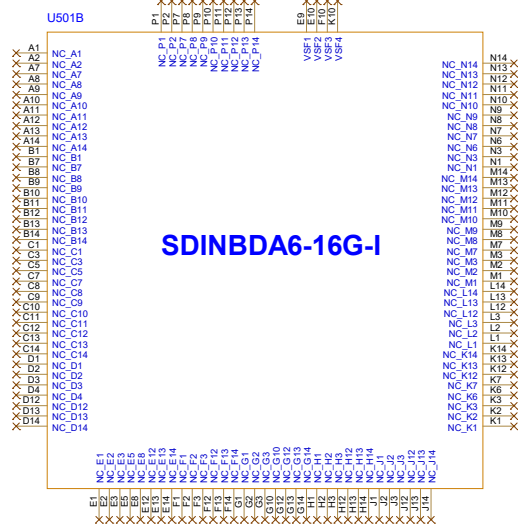
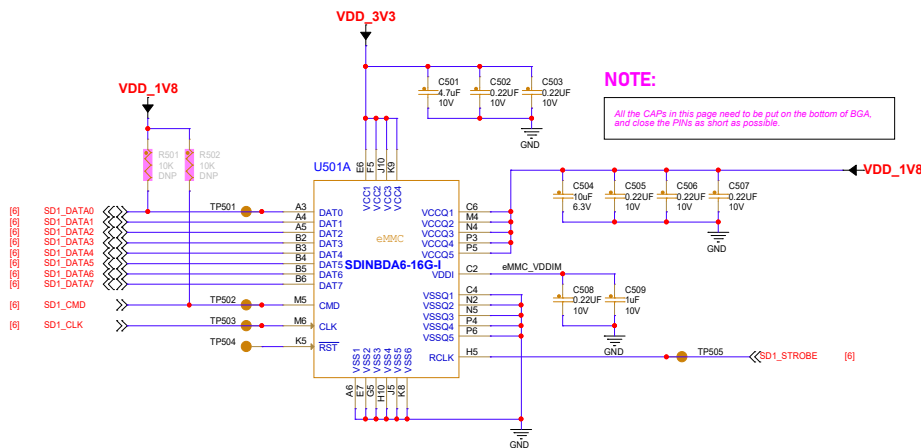
M.2 UART



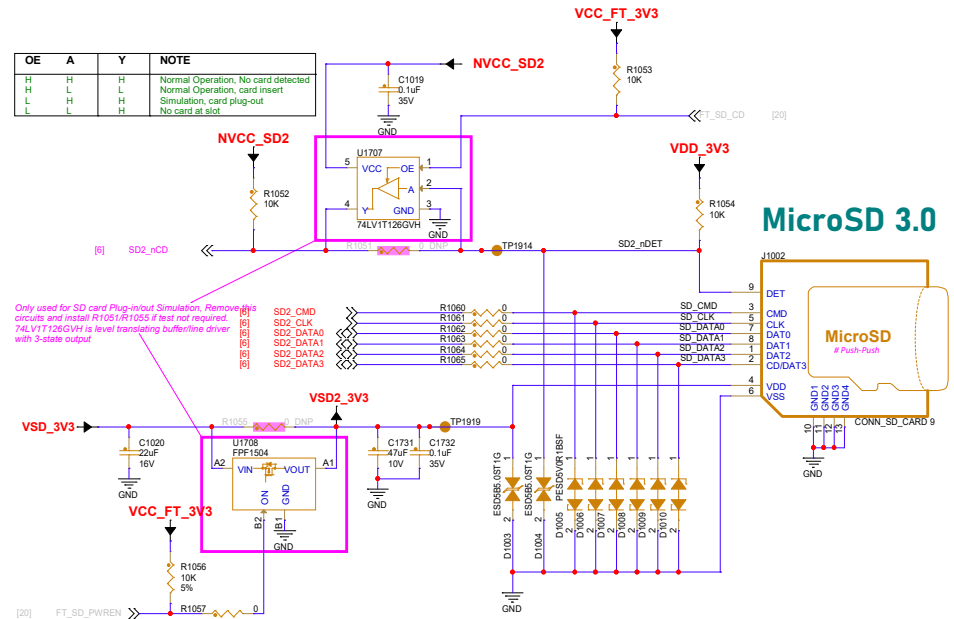
Debug through JTAG interface must remove card inserted in M.2 U1707

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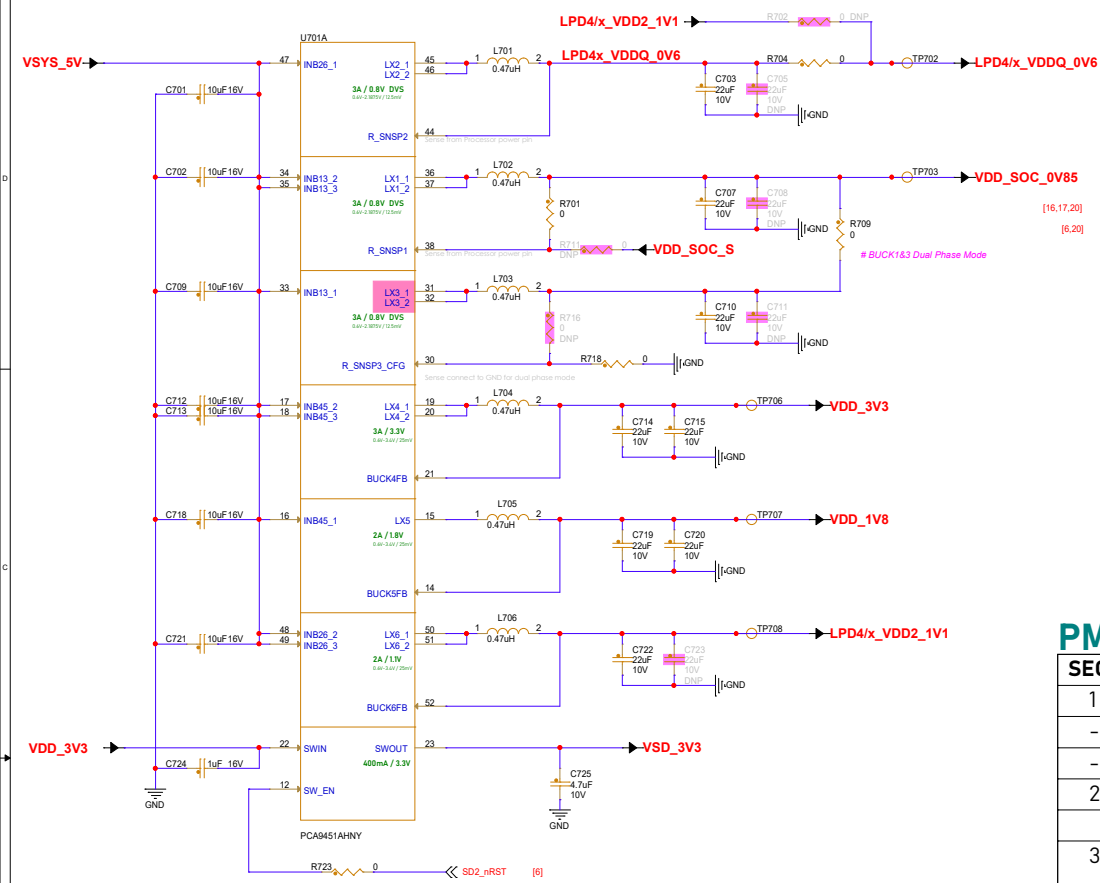
FLASH: eMMC <5.1> 16GB <2D MLC eMMC>



OE	A	Y	NOTE
H	H	L	Normal Operation, No card detected
H	L	L	Normal Operation, card insert
L	L	H	Simulation, card plug-out
L	L	L	No card at slot

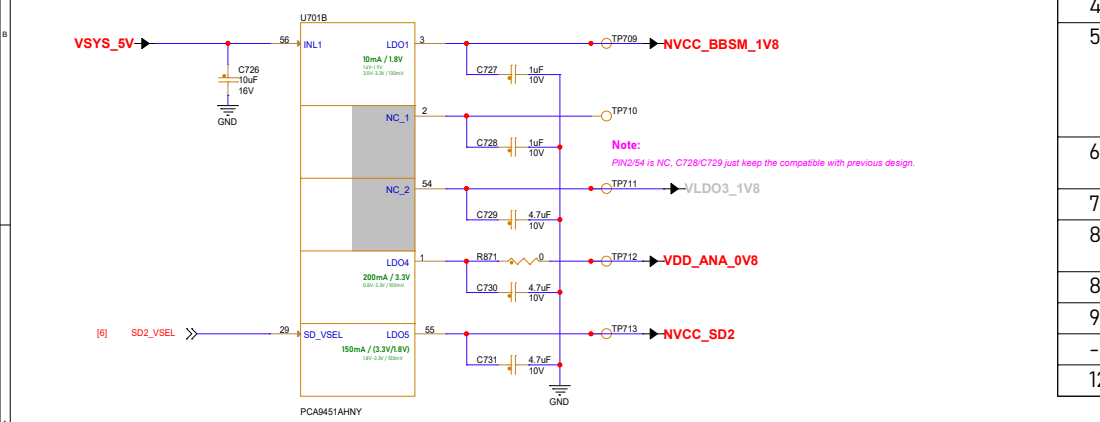


SYS PMIC



PMIC: PCA9451AHN CFG

SEQ	tstep/2ms	REGULATOR	VOL (V)	MAX I (mA)	PWR RAIL	TYP VOL(V)	REQ I (mA)
1		LDO1	1.8	10	NVCC_BB5M_1V8	1.8	2
-					PMIC_ON_REQ		
2	T1	BUCK1/3 DP	0.85	4000	VDD_SOC	DVS	Ref to DS
3	T2	LDO4	0.8	200	VDD_ANA_0P8 VDD_MIPI_0P8 VDD_USB_0P8	0.8	186
4							
5	T4	BUCK5	1.8	2000	VDD_ANAx_1P8 VDD_LVDS_1P8 VDD_MIPI_1P8 VDD_USB_1P8 NVCC_GPIO	1.8	1040 PERI INCLUDE
6	T5	BUCK6	1.1	1500	VDD2_DDR VDDQ_DDR (1.1V for LPD4)	1.1	676
7	T6	BUCK2	0.6	2000	VDDQ_DDR (0.6V for LPD4x)	0.6	360
8	T7	BUCK4	3.3	3000	NVCC_GPIO VDD_USB_3P3	3.3	2870 PERI INCLUDE
8	T7	Load Switch	-	400	SD_CARD (from BUCK4)	3.3	
9	T8	LDO5	1.8/3.3	150	NVCC_SD2	1.8/3.3	
-							
12		POR_B	--	--	POR_B		



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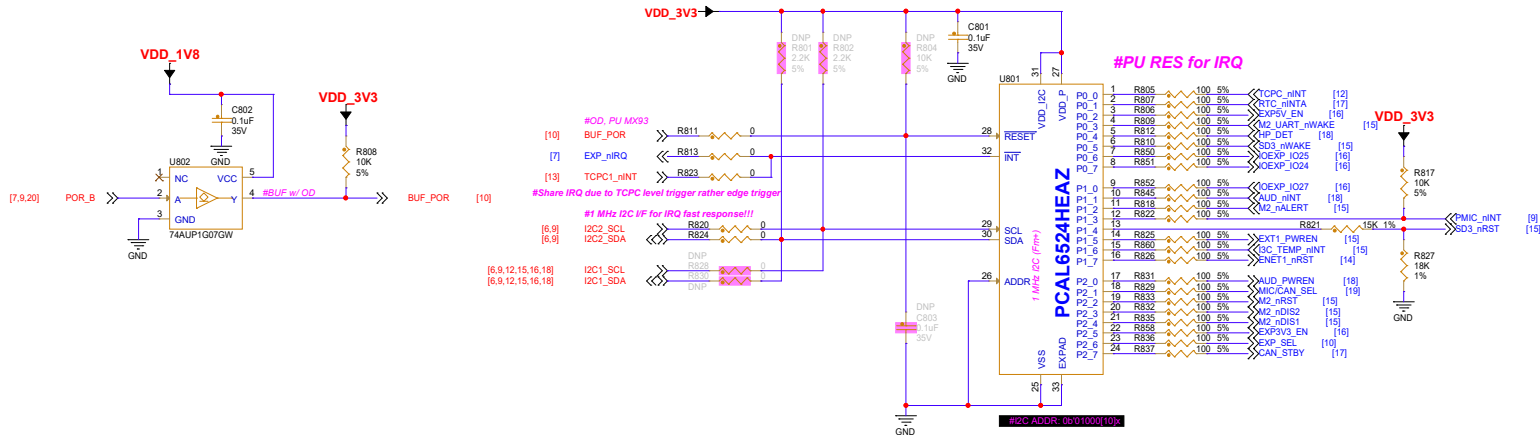
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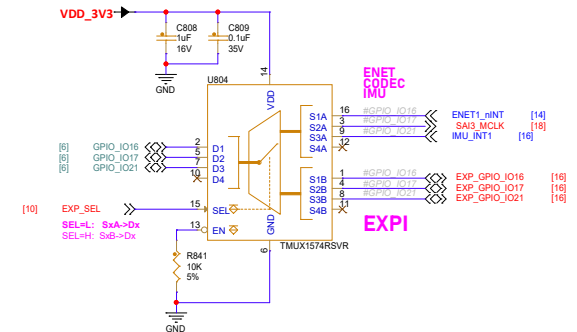
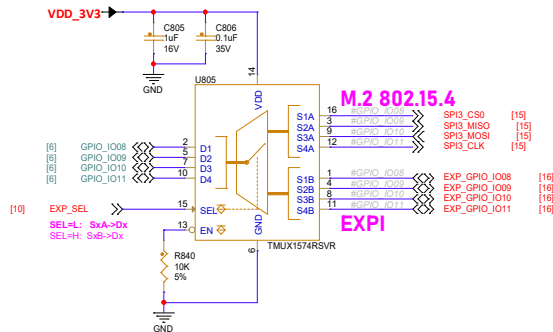
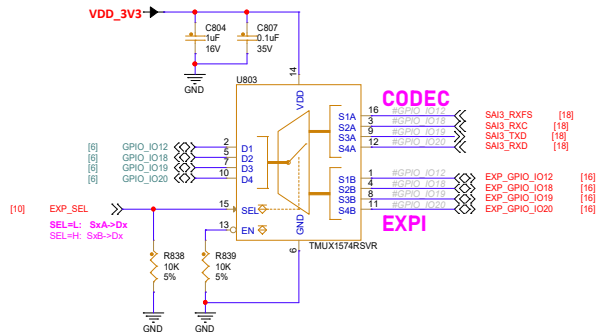
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IO MUX / EXP



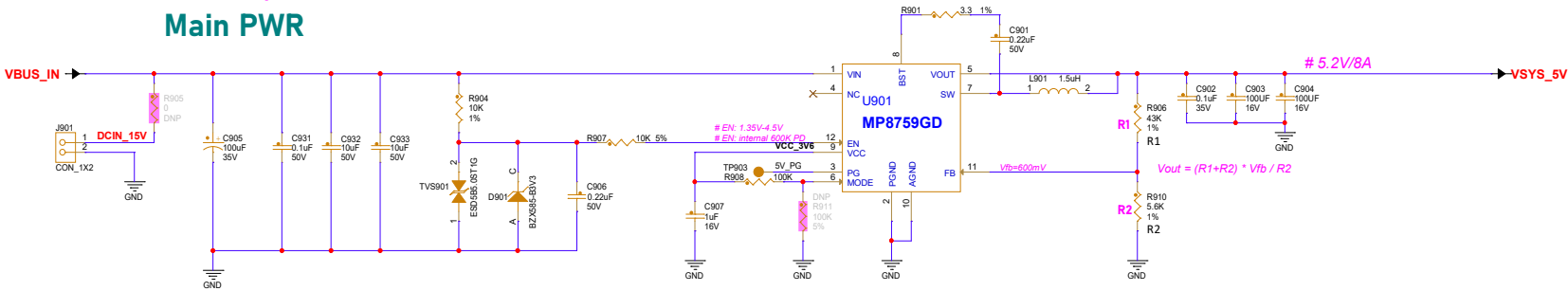
SHARED GPIO MUX



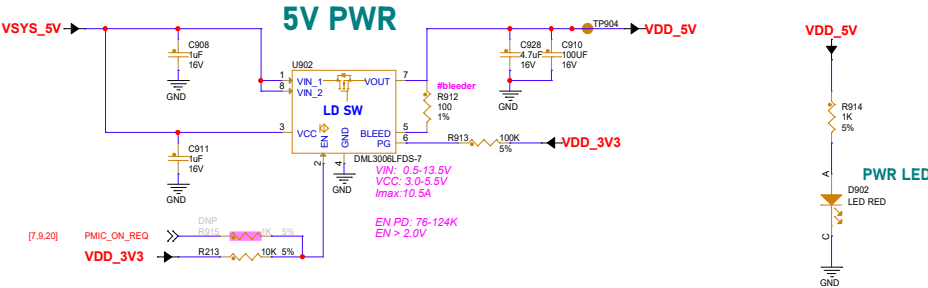
SYSTEM POWER

When PERI 12V is required, VBUS_IN must be at least 12V!!!

Main PWR

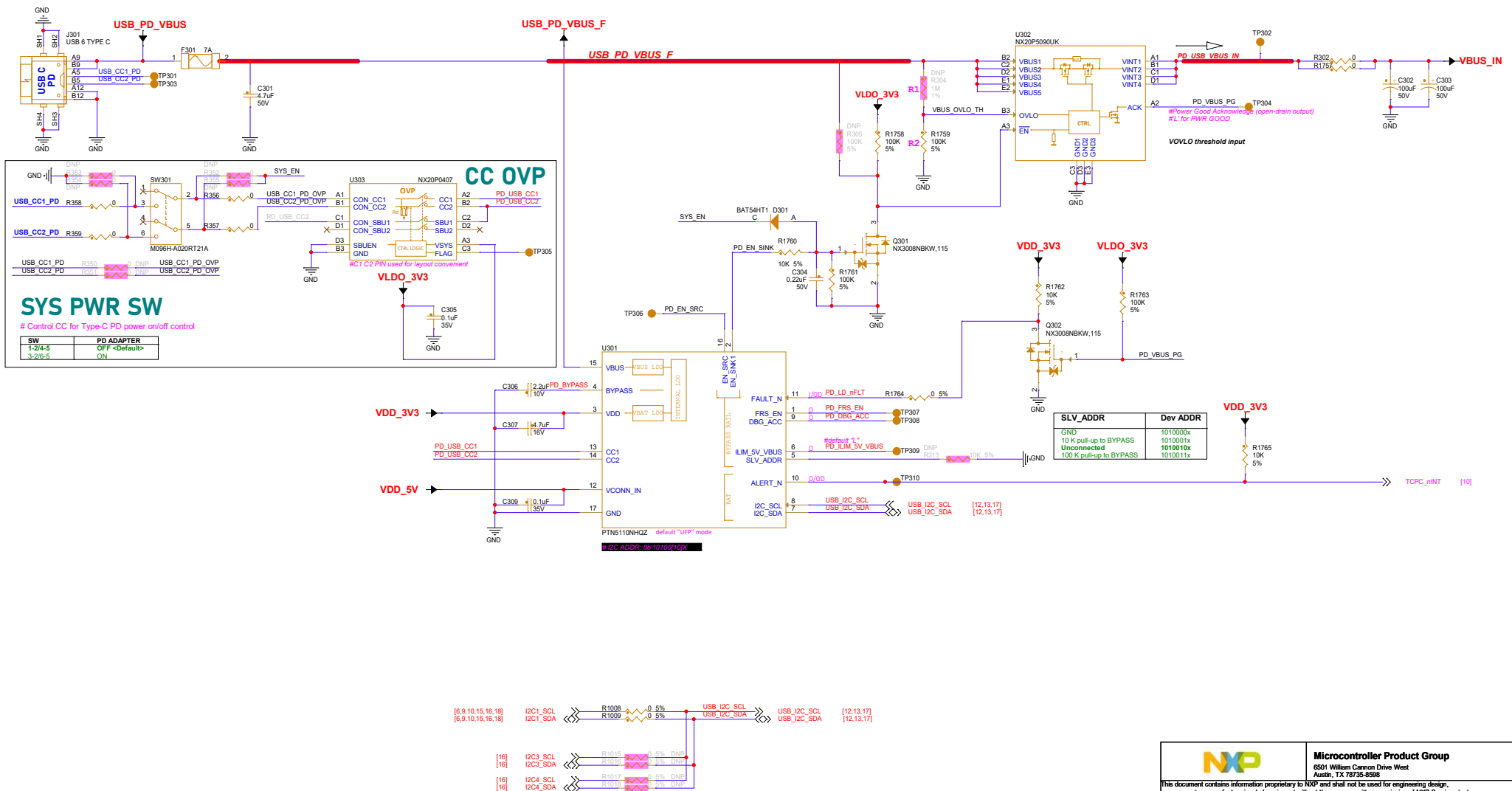


5V PWR

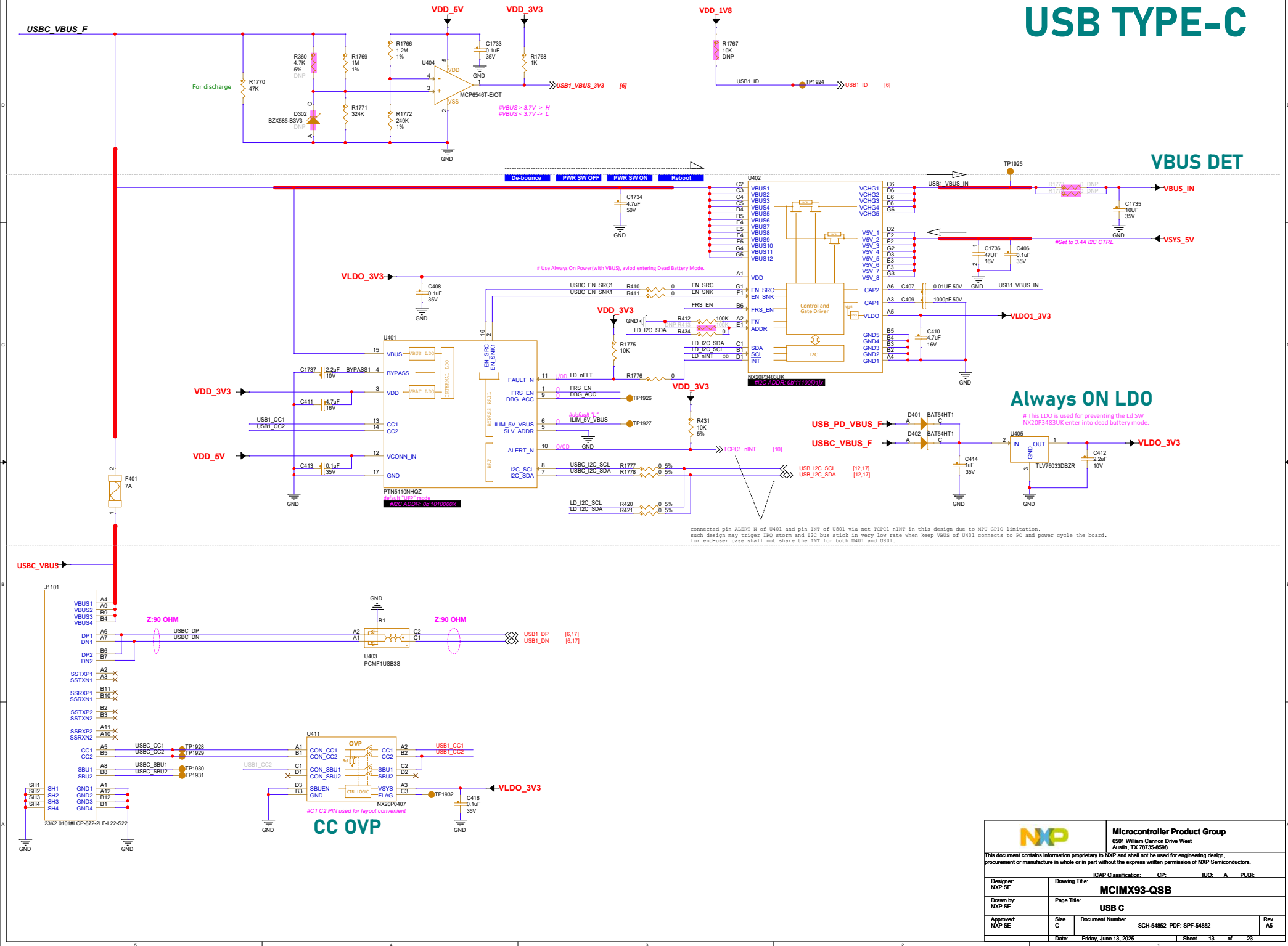


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					Rev A5

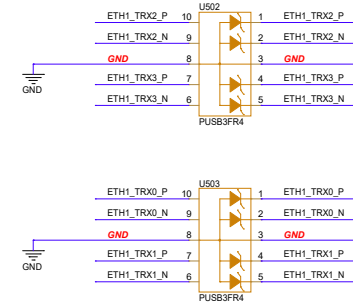
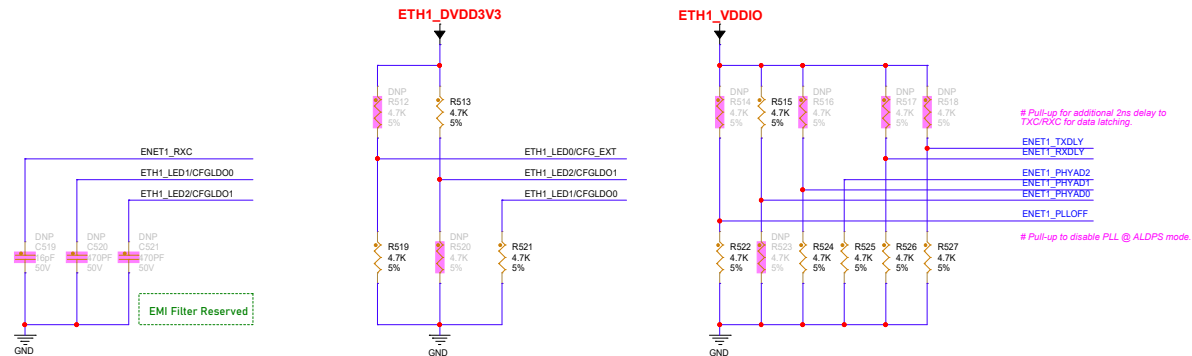
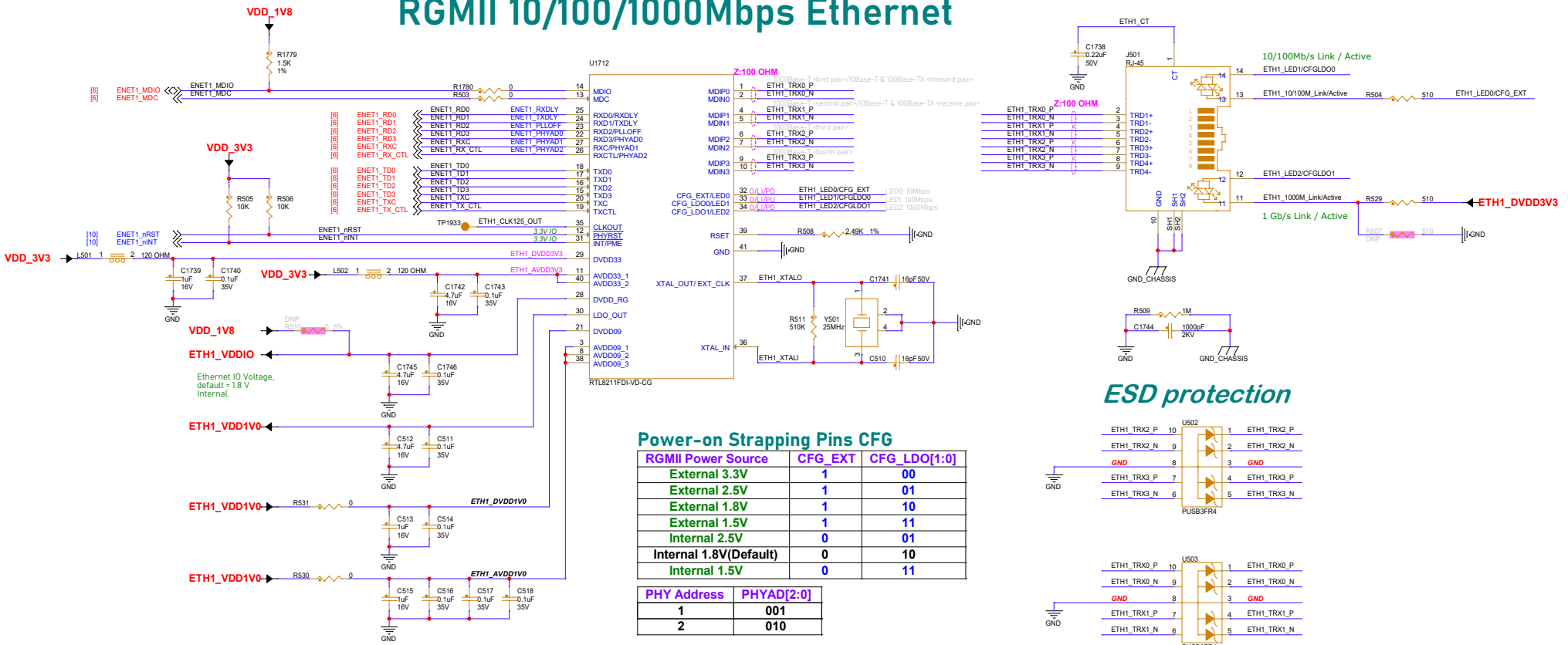
USB TYPE-C PD



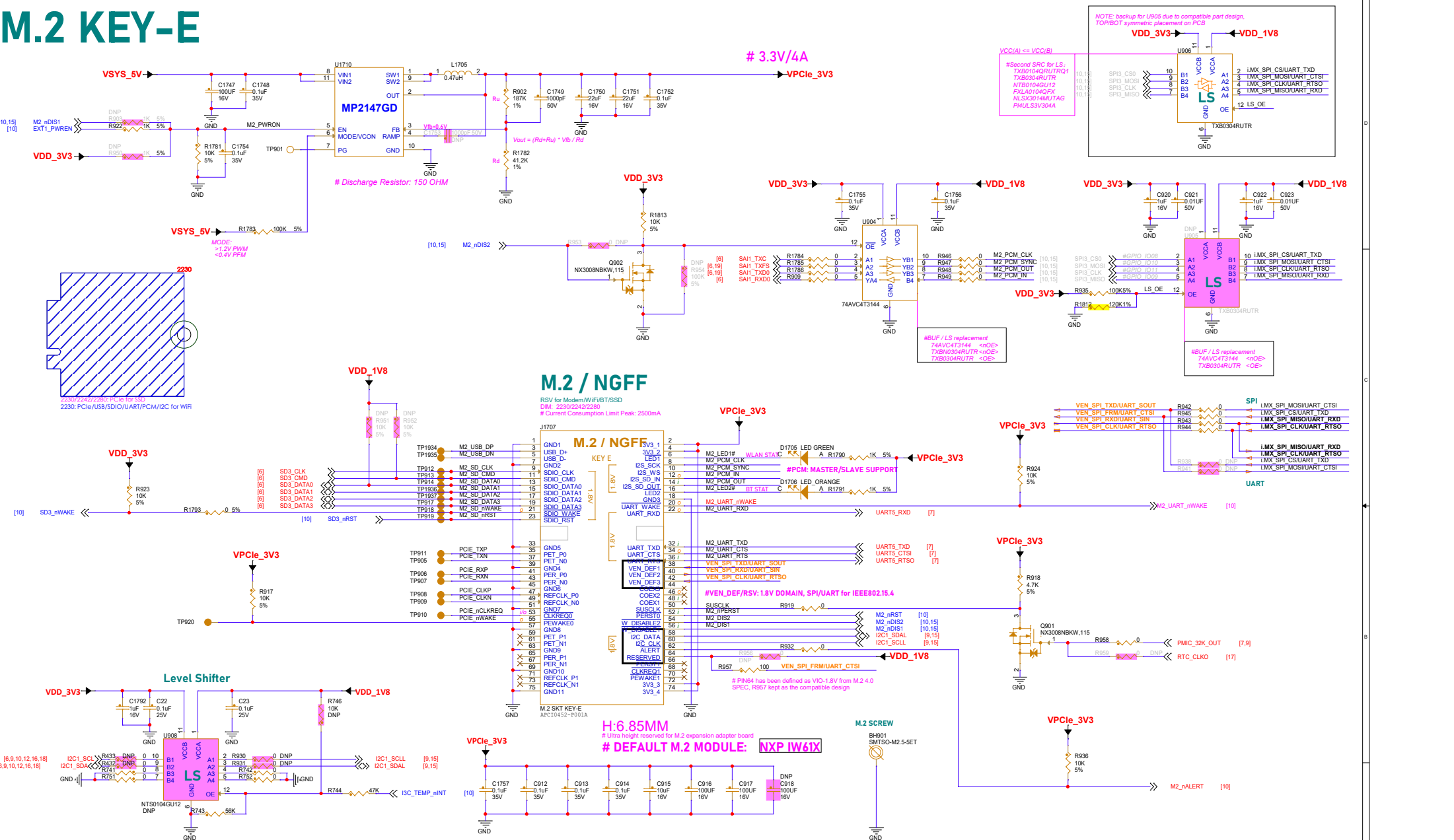
USB TYPE-C



RGMII 10/100/1000Mbps Ethernet



M.2 KEY-E



Key ID	Pin	Interface	Key Definition
A	8-15	2x PCIe x1 / USB 2.0 / I2C / DP x4	Display Port Based Connectivity
B	12-19	PCIe x2 / SATA / USB 2.0 / USB 3.1 Gen1 / HSIC / SSIC / Audio / UIM / I2C / SMBus	WWAN/SSD/Others Primary Key
C	16-23	PCIe/M-PCIe / USB 2.0 / USB 3.1 Gen1 / SSIC / I2C-SlimBUS / UIM / ANTCTL	WWAN Key
D	20-27	Reserved for Future Use (RFU)	RFU
E	24-31	2x PCIe x1 / USB 2.0 / I2C / SDIO / UART / PCM	SDIO Based Connectivity
F	28-35	Future Memory Interface (FMI)	Future Memory Interface
G	39-46	Not Used for M.2; for Custom/Non-Standard Apps	Generic (Not used for M.2)
H	43-50	Reserved for Future Use (RFU)	RFU
J	47-54	Reserved for Future Use (RFU)	RFU
K	51-58	Reserved for Future Use (RFU)	RFU
L	55-62	Reserved for Future Use (RFU)	RFU
M	59-66	PCIe x4 / SATA / SMBus	SSD 4 Lane PCIe

i.MX93 GPIO8-11

#GPIO_008 #SPI0_CS #UART2_TXD
#GPIO_009 #SPI0_MISO #UART2_RXD
#GPIO_010 #SPI0_MOSI #UART2_CTS<0>
#GPIO_011 #SPI0_CLK #UART2_RTS<0>

1W61X GPIO12-15

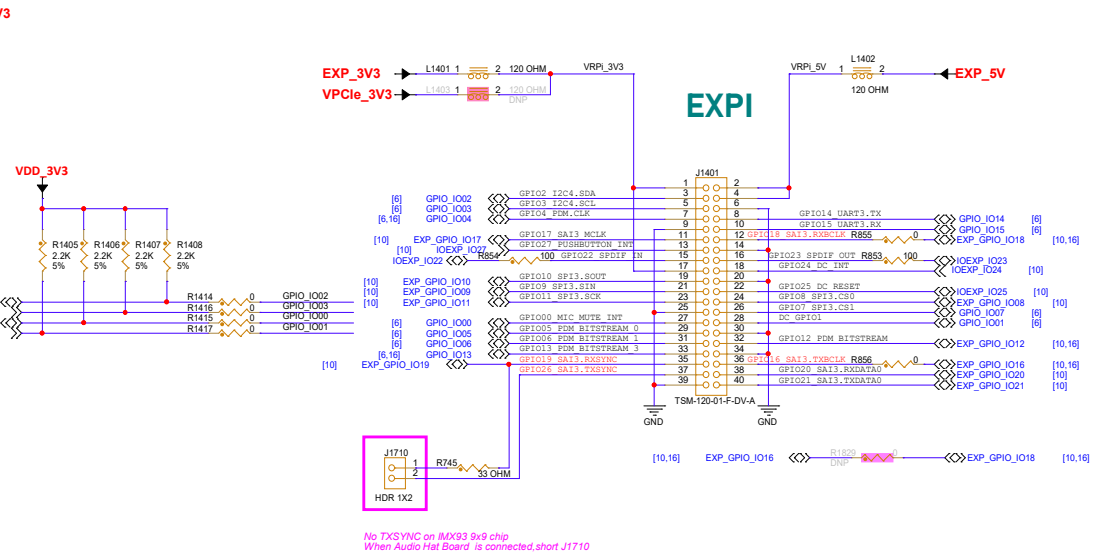
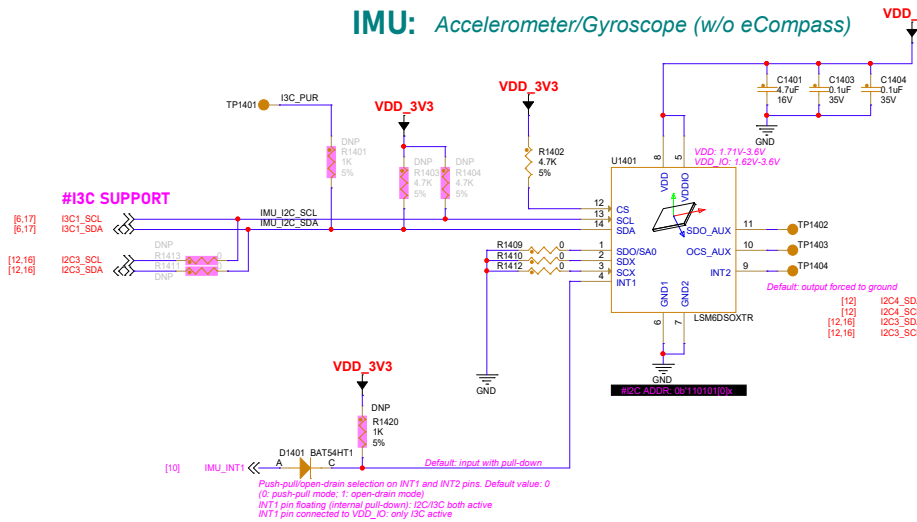
#GPIO_ID15 #SPI1_TXD #UART2_SOUT
#GPIO_ID14 #SPI1_RXD #UART2_SIN
#GPIO_ID13 #SPI1_FIRM #UART2_RTS<0>
#GPIO_ID12 #SPI1_CLK #UART2_CTS<0>

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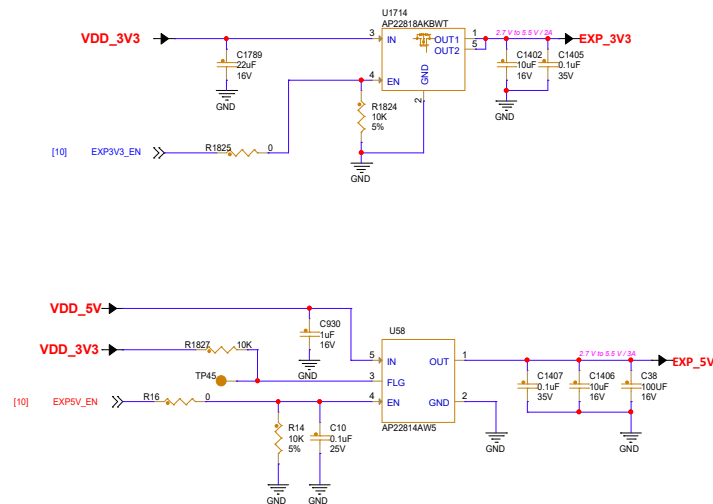
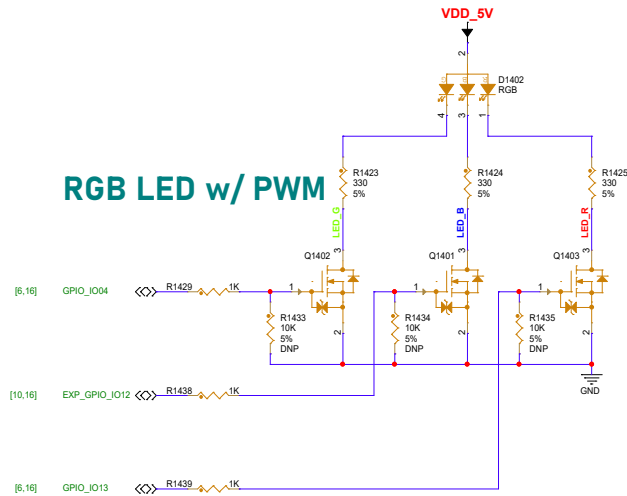
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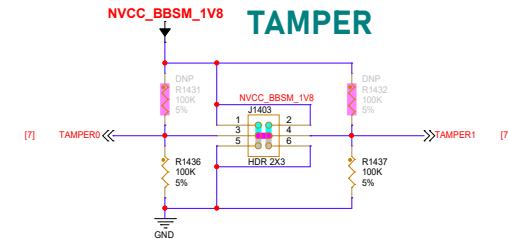
IMU: Accelerometer/Gyroscope (w/o eCompass)



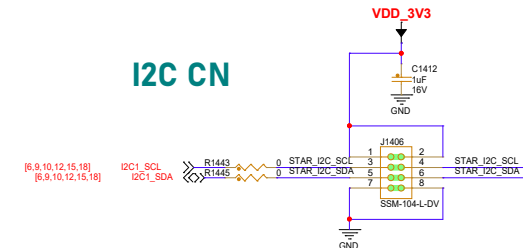
RGB LED w/ PWM



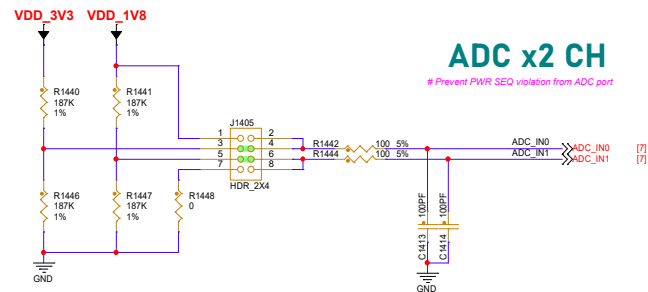
NVCC_BBSM_1V8 TAMPER



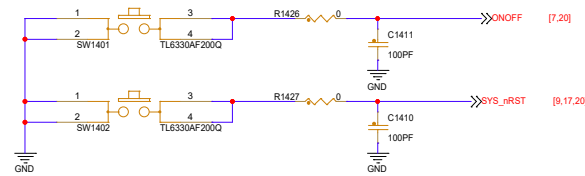
I2C CN




ADC x2 CH

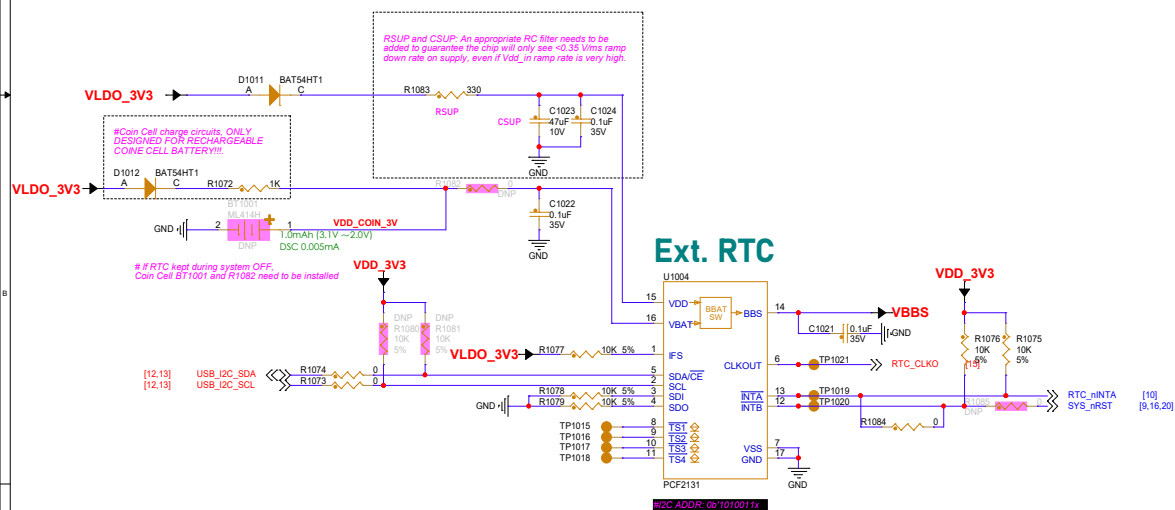
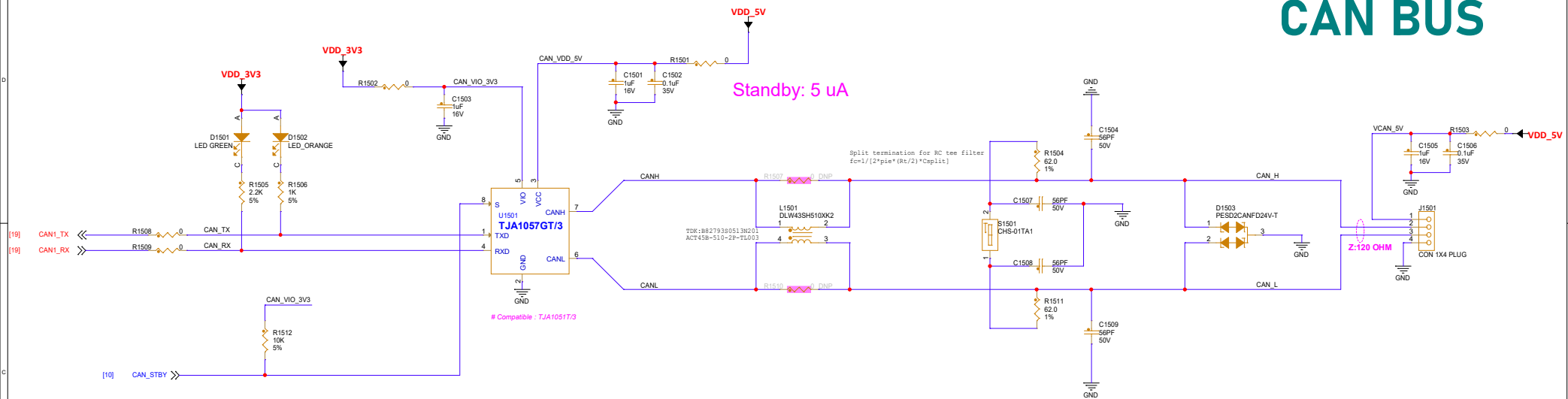


Buttons

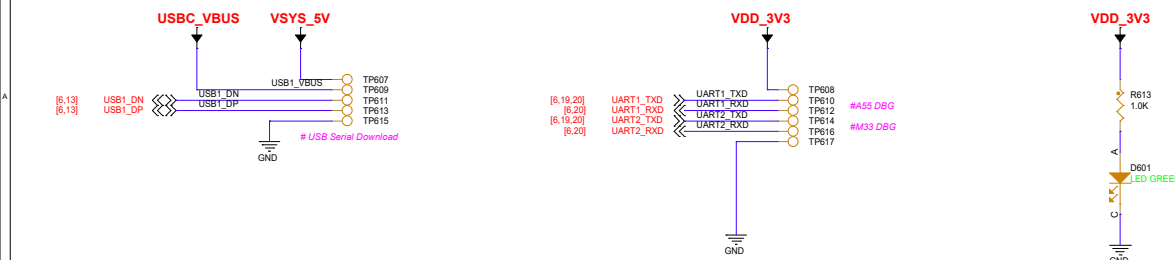
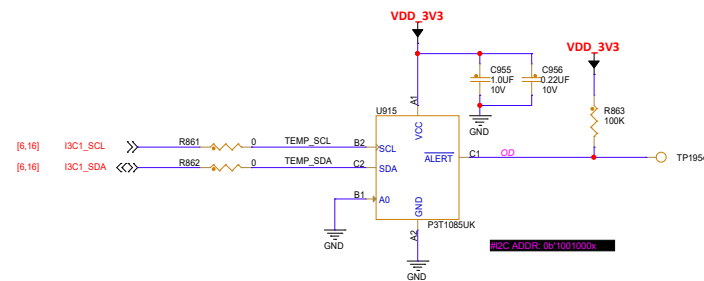



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Approved: NXP SE		Size C Document Number SC9-54852 PDF: SPF-54852	
Date: Friday, June 13 2008		Sheet 16 of 23	
Rev A5			

CAN BUS



I3C TEMP SENSOR

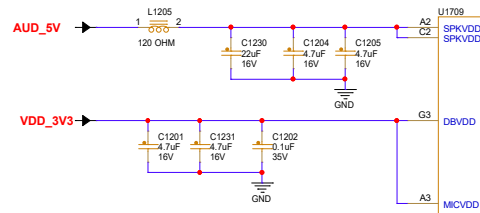


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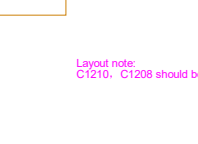
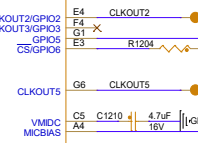
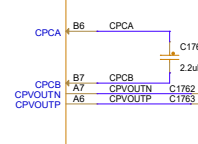
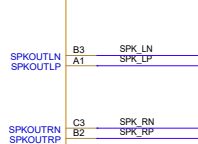
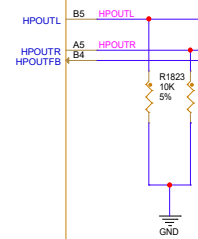
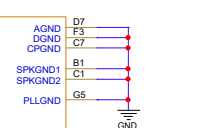
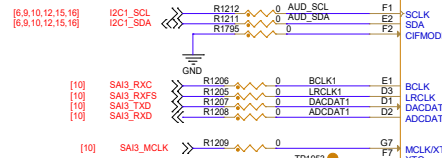
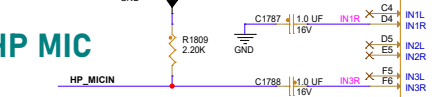
CODEC

DCVDD	1.62V - 2.0V
DBVDD	1.62V - 3.6V
MICVDD	1.70V - 3.6V
AVDD	1.70V - 2.0V
PLLVDD	1.70V - 2.0V
CPVDD	1.70V - 2.0V
SPKVDD	1.70V - 5.5V

Layout note:
Widen the trace SPKVDD
Max ~0.6A



HP MIC



Layout note:
C1210, C1208 should be as close to the WM8962B as possible.

HP_DET: REMOVE
LOW: PLUG
HIGH: PLUG

[10] HP_DET <<< R1822 0 HP_J_D

Layout note:
C1771 & C1772 close to HP Jack, for EMI purpose

Layout note:
Zobel Networks(C1769,C1770,R1798,R1801) close to WM8962B

Layout note:
C1761 should be as close to the WM8962B as possible.

VDD_3V3

R1203 100K R1221 100K

CLKOUT2/GPIO2 CLKOUT3/GPIO3 CS/GPIO6

CLKOUT5 TP1950

VMDC MICBIAS

C1219 4.7uF 16V

C1208 1.0 uF 16V

MICBIAS

TP1948

TP1949

TP1950

TP1951

TP1952

TP1953

TP1954

TP1955

TP1956

TP1957

TP1958

TP1959

TP1960

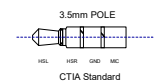
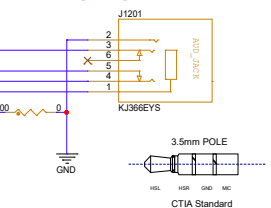
TP1961

TP1962

TP1963

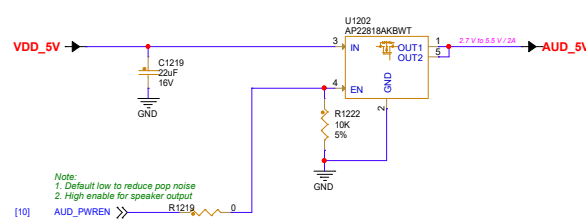
TP1964

HP JACK



Layout note:
R1800 close to J1201

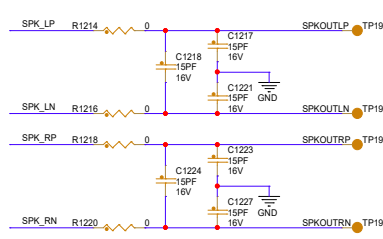
SPK PWR



Note:
1. Default low to reduce pop noise
2. High enable for speaker output

[10] AUD_PWREN >>> R1219 0

SPK CN



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PDM MIC

LDO 1.8V for DMIC

BOOT MODE CFG


i.MX93 BOOT MODE

BOOT_MODE[3:0]	BOOT CORE	BOOT DEVICE	COMMENT
0000	Cortex-A55	From internal fuses	
0001	Cortex-A55	Serial Downloader(USB1)	USB1
0010	Cortex-A55	USDHC1 8-bit eMMC 5.1	
0011	Cortex-A55	USDHC2 4-bit SD3.0	
0100	Cortex-A55	FlexSPI Serial NOR	with SFDP (JESD-216) discoverable parameters
0101	Cortex-A55	FlexSPI Serial NAND 2K	
0110	Cortex-A55	Infinite Loop	
0111	Cortex-A55	Test Mode (A55)	
1000	Cortex-M33	LPB: Boot From Fuses	
1001	Cortex-M33	LPB: Serial Downloader (USB1)	USB1
1010	Cortex-M33	LPB: USDHC1 8-bit 1.8V eMMC 5.1	
1011	Cortex-M33	LPB: USDHC2 4-bit SD 3.0	
1100	Cortex-M33	LPB: FlexSPI Serial NOR	with SFDP (JESD-216) discoverable parameters
1101	Cortex-M33	LPB: FlexSPI Serial NAND 2K	
1110	Cortex-M33	Infinite Loop	
1111	Cortex-M33	Test Mode (For DFT ATE Test)	

MIC/CAN

BOOT CFG

74LV1T34GWH:
Used for 1.8V/3.3V level translator;
Both 1.8V and 3.3V can be used for the DMIC array;
1.8V is designed due to high SNR;
If 3.3V used, part can be removed;



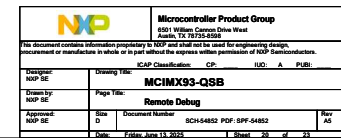
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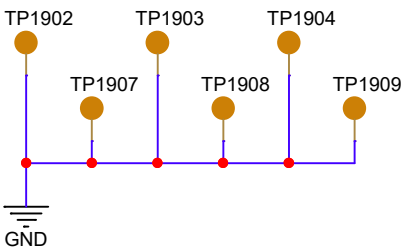
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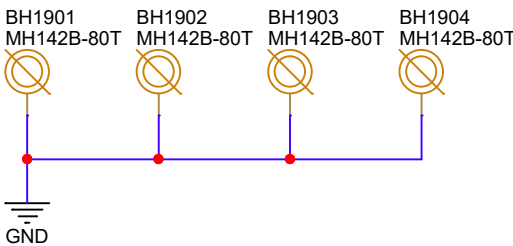
i.MX SoC RC I/F



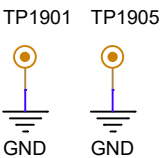
GND TP




SCREW HOLE



GND TESTLOOP



TOP Layer


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NOTE:

I2C DEV TABLE

PART	DEVICE	I2C ADDR	PORT	SPEED	VOL	DESCRIPTION
U801	PCAL6524HEAZ	0x22 (0b'01000[10]x)	MX-I2C2	1MHz Fm+	3.3V	IO EXP for IRQ/OUTPUT
U301	PTN5110NHQZ	0x52 (0b'10100[10]x)	MX-I2C1	400KHz	3.3V	USB C PD PHY
U401	PTN5110NHQZ	0x50 (0b'10100[00]x)	MX-I2C1	400KHz	3.3V	USB C PD PHY
U402	NX20P3483UK	0x71 (0b'11100[01]x)	MX-I2C1	400KHz	3.3V	USB Load Switch
U1401	LSM6DSOXTR	0x6A (0b'110101[0]x)	MX-I2C1/I2C3	I3C/I2C-400KHz	3.3V	IMU (I3C support)
U1709	WM8962B	0x1A (0b'0011010x)	MX-I2C1	526KHz	3.3V	Audio CODEC
U701	PCA9451AHN	0x25 (0b'0100101x)	MX-I2C2	1MHz Fm+	3.3V	PMIC
U1409	PCA9655EMTTXG	0x21 (0b'0100001)	FTDI-I2C	1MHz Fm+	3.3V	RDPM IO EXP
U915	P3T1085UK	0x48 (0b'1001000x)	MX-I2C1	I3C/I2C-400KHz	3.3V	Temp Sensor (I3C support)
U1004	PCF2131TF	0x53 (0b'1010011x)	MX-I2C1	400KHz	3.3V	Ext RTC

IOPAD	Alt0	Alt1	Alt2	Alt3	Alt4	Alt5	Alt6	Alt7	DEF MUX	Reset Status
RT0_XTALI RT0_XTALO PMIC_STBY_REQ PMIC_ON_REQ ONOFF POR_B TAMPER0 TAMPER1 GPIO_I000 GPIO_I001 GPIO_I002 GPIO_I003 GPIO_I004 GPIO_I005 GPIO_I006 GPIO_I007 GPIO_I008 GPIO_I009 GPIO_I010 GPIO_I011 GPIO_I012 GPIO_I013 GPIO_I014 GPIO_I015 GPIO_I016 GPIO_I017 GPIO_I018 GPIO_I019 GPIO_I020 GPIO_I021 GPIO_I022 GPIO_I023 GPIO_I024 GPIO_I025 GPIO_I026 GPIO_I027 GPIO_I028 GPIO_I029 COM_CLK01 COM_CLK02 COM_CLK03 COM_CLK04 DAP_TDI DAP_TMS_SWDIO DAP_TCLK_SWCLK DAP_TDO_TRACESWO ENET1_MDIO ENET1_MDIO ENET1_T0 ENET1_T1 ENET1_T2 ENET1_T3 ENET1_T4 ENET1_T5 ENET1_T6 ENET1_T7 ENET1_T8 ENET1_T9 ENET1_T10 ENET1_T11 ENET1_T12 ENET1_T13 ENET1_T14 ENET1_T15 ENET1_T16 ENET1_T17 ENET1_T18 ENET1_T19 ENET1_T20 ENET1_T21 ENET1_T22 ENET1_T23 ENET1_T24 ENET1_T25 ENET1_T26 ENET1_T27 ENET1_T28 ENET1_T29 ENET1_T30 ENET1_T31 ENET1_T32 ENET1_T33 ENET1_T34 ENET1_T35 ENET1_T36 ENET1_T37 ENET1_T38 ENET1_T39 ENET1_T40 ENET1_T41 ENET1_T42 ENET1_T43 ENET1_T44 ENET1_T45 ENET1_T46 ENET1_T47 ENET1_T48 ENET1_T49 ENET1_T50 ENET1_T51 ENET1_T52 ENET1_T53 ENET1_T54 ENET1_T55 ENET1_T56 ENET1_T57 ENET1_T58 ENET1_T59 ENET1_T60 ENET1_T61 ENET1_T62 ENET1_T63 ENET1_T64 ENET1_T65 ENET1_T66 ENET1_T67 ENET1_T68 ENET1_T69 ENET1_T70 ENET1_T71 ENET1_T72 ENET1_T73 ENET1_T74 ENET1_T75 ENET1_T76 ENET1_T77 ENET1_T78 ENET1_T79 ENET1_T80 ENET1_T81 ENET1_T82 ENET1_T83 ENET1_T84 ENET1_T85 ENET1_T86 ENET1_T87 ENET1_T88 ENET1_T89 ENET1_T90 ENET1_T91 ENET1_T92 ENET1_T93 ENET1_T94 ENET1_T95 ENET1_T96 ENET1_T97 ENET1_T98 ENET1_T99 ENET1_T100 ENET1_T101 ENET1_T102 ENET1_T103 ENET1_T104 ENET1_T105 ENET1_T106 ENET1_T107 ENET1_T108 ENET1_T109 ENET1_T110 ENET1_T111 ENET1_T112 ENET1_T113 ENET1_T114 ENET1_T115 ENET1_T116 ENET1_T117 ENET1_T118 ENET1_T119 ENET1_T120 ENET1_T121 ENET1_T122 ENET1_T123 ENET1_T124 ENET1_T125 ENET1_T126 ENET1_T127 ENET1_T128 ENET1_T129 ENET1_T130 ENET1_T131 ENET1_T132 ENET1_T133 ENET1_T134 ENET1_T135 ENET1_T136 ENET1_T137 ENET1_T138 ENET1_T139 ENET1_T140 ENET1_T141 ENET1_T142 ENET1_T143 ENET1_T144 ENET1_T145 ENET1_T146 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