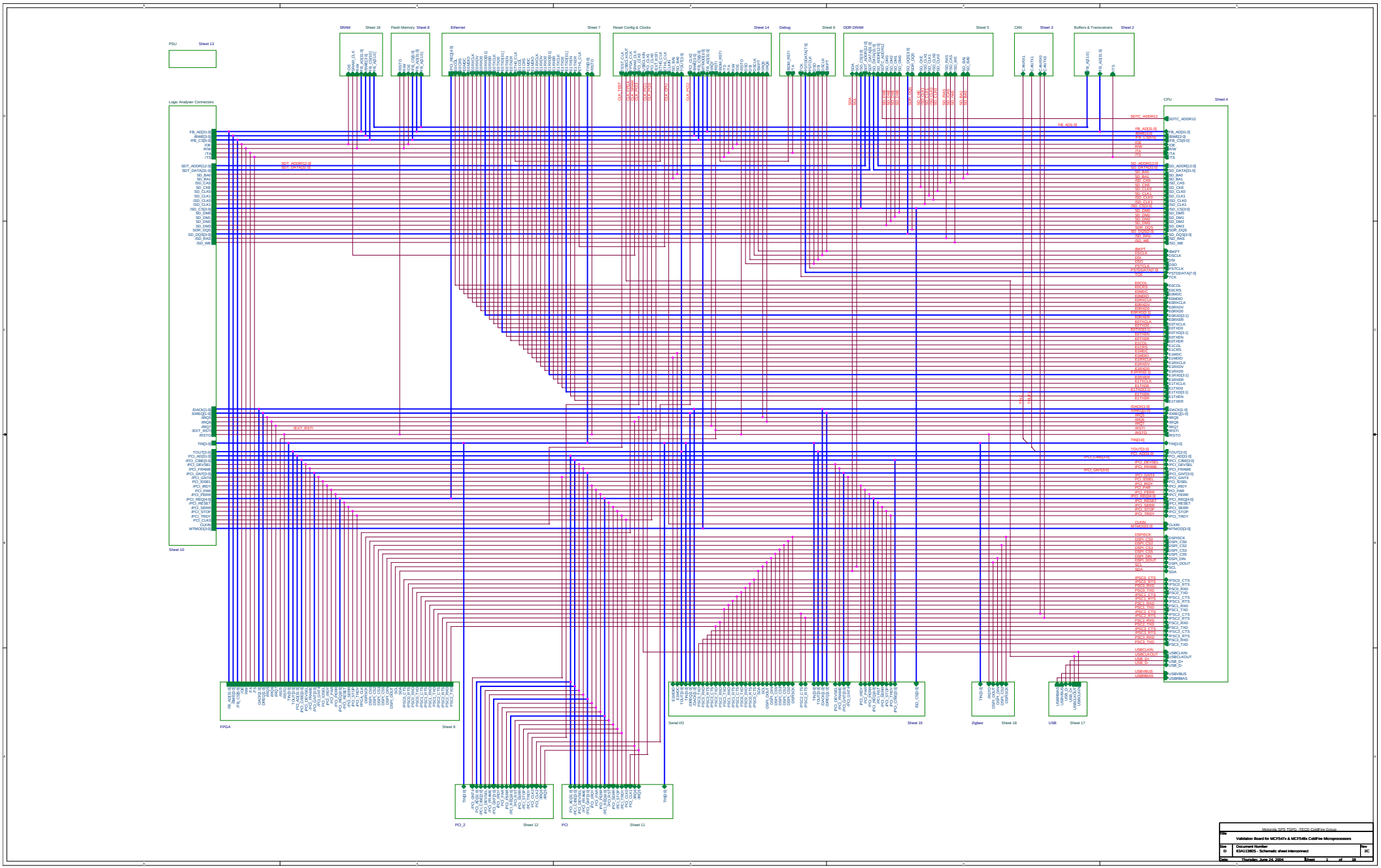

SRAM
Sheet 16
Flash Memory
Sheet 8
Ethernet
Sheet 7
Reset Config & Clocks
Sheet 14
Debug
Sheet 6
DDR DRAM
Sheet 5
CAN
Sheet 3
Buffers & Transceivers
Sheet 2
PSU
Sheet 13
Logic Analyser Connectors
Sheet 10
CPU
Sheet 4
FPGA
Sheet 9
Serial I/O
Sheet 15
Zigbee
Sheet 18
USB
Sheet 17
PCI_2
Sheet 12
PCI
Sheet 11
Motorola SPS TSPD - TSTR ColdFire Group
Validation Board for MCF547x & MCF548x ColdFire Microprocessors
Size
D
Document Number
63A113805 - Schematic sheet interconnect
Rev
2C
Date:
Thursday, June 24, 2004
Sheet
1
of
38

Address bus latches.

FB_A[31:0]

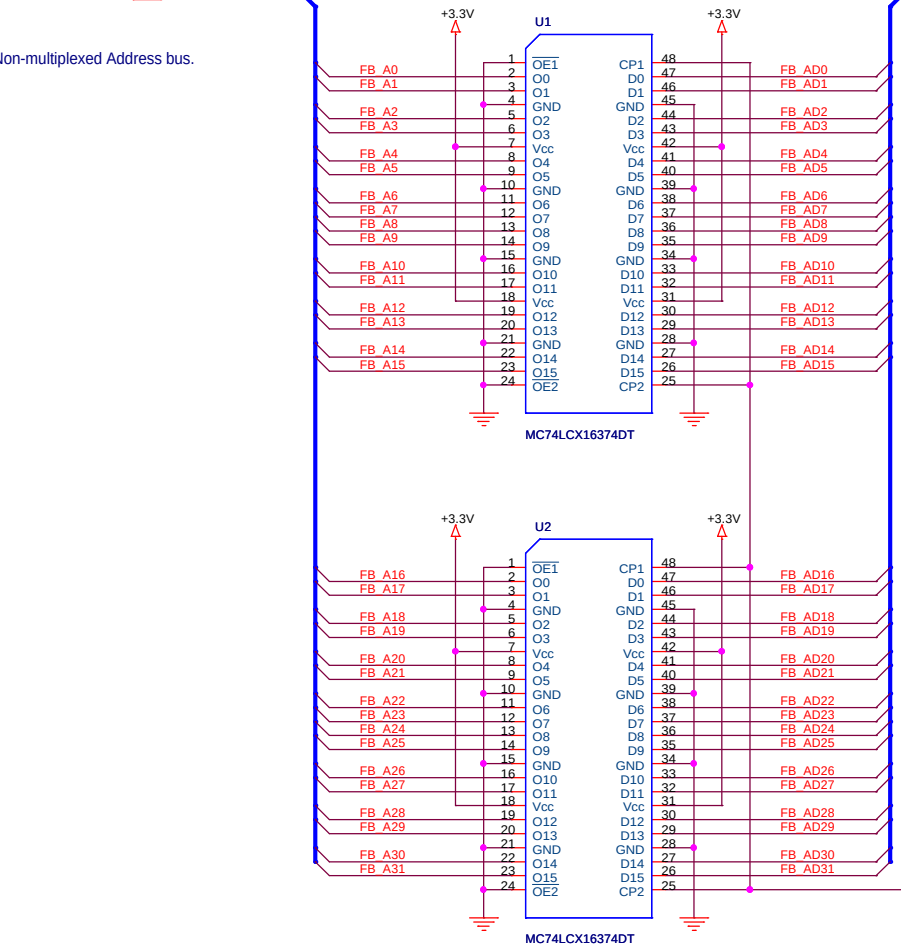
FB_A[31:0]

Non-multiplexed Address bus.

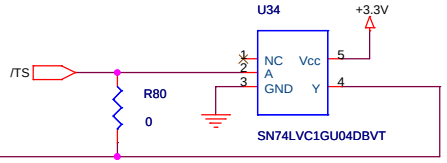
FB_AD[31:0]

FB_AD[31:0]

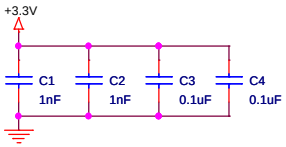
Multiplexed Address/Data bus from the CPU (sheet 4).



NOTE: For revision 1.0 of the MCF547x/8x, R80 is not populated, U34 is populated, and U1 and U2 should be '374 transparent latches. For revision 1.1 of the MCF547x/8x, the /TS signal will be inverted on-chip to generate an address latch enable (ALE) signal and the external inverter will not be needed. In this case R80 is populated, U34 is not, and U1 and U2 should be '373 transparent latches.



NOTE: please keep the track length from U34 pin 4 to U1 & U2 pins 25 & 48 to a minimum.



Motorola SPS TSPG -TECD ColdFire Group

Title: Validation Board for MCF547x & MCF548x Microprocessors

Size	Document Number	Rev
B	63A11380S - Flex bus address latches	2C

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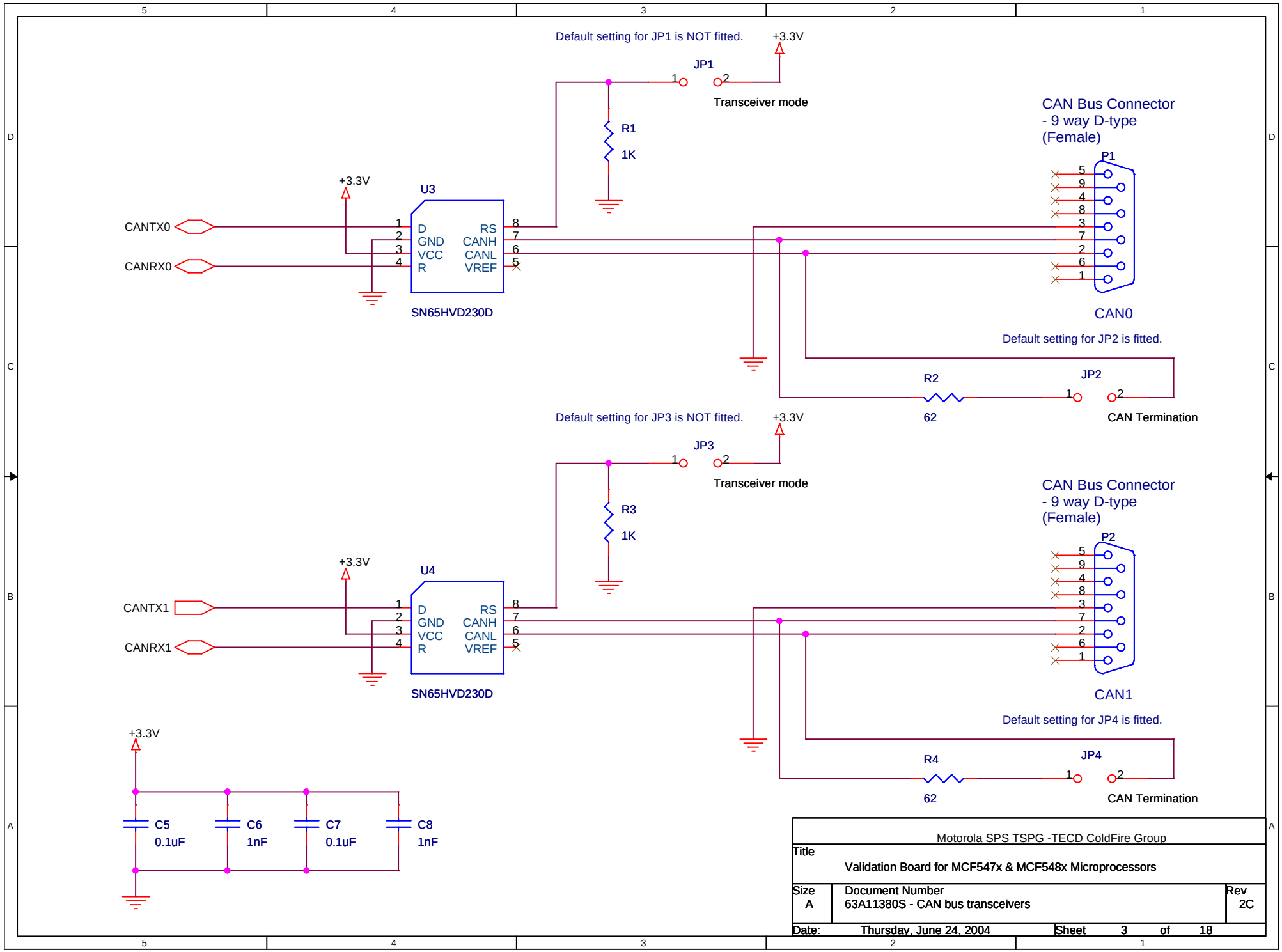
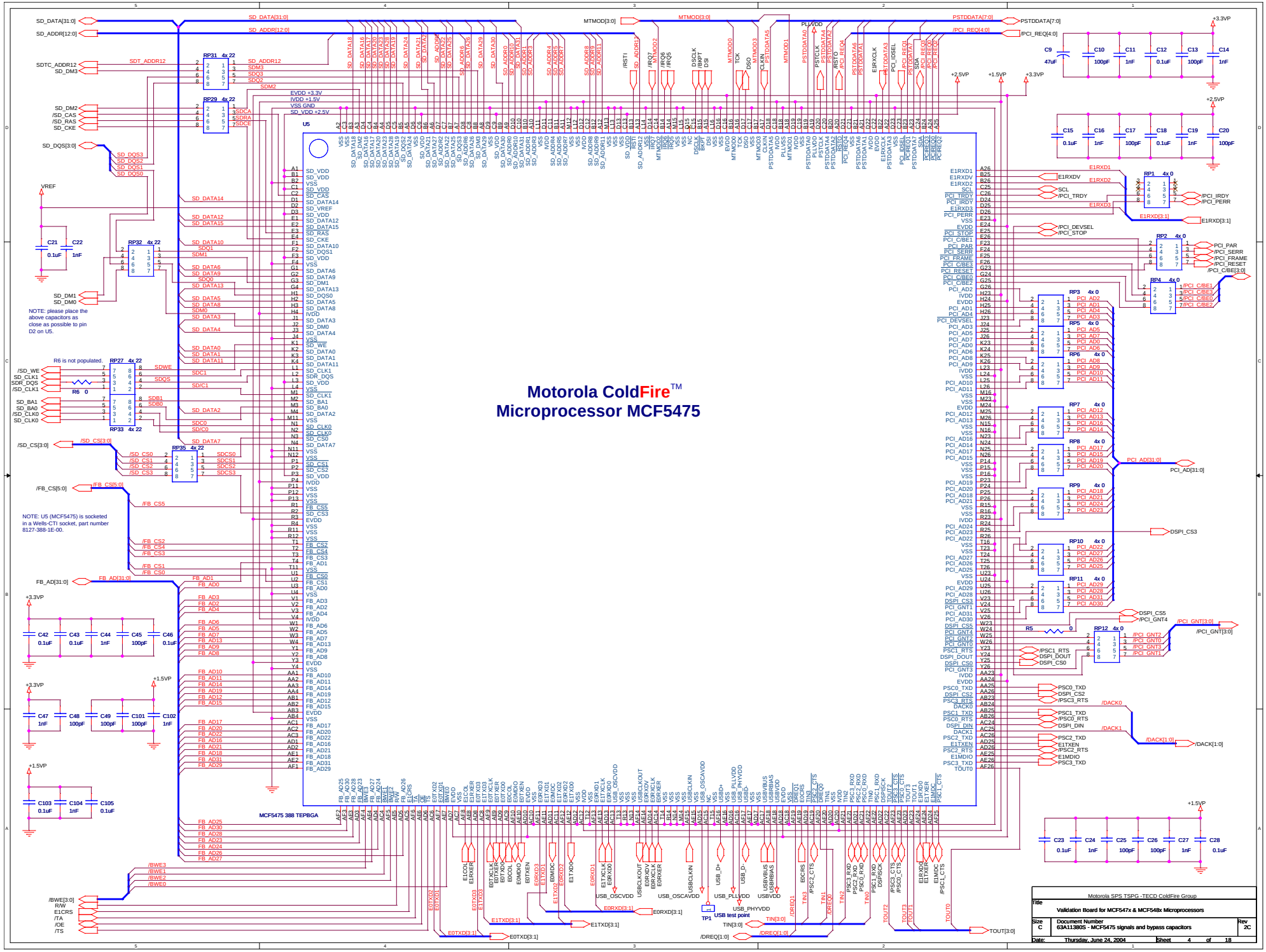


Motorola SPS TSPG -TECD ColdFire Group		
Title: Validation Board for MCF547x & MCF548x Microprocessors		
Size: A	Document Number: 63A11380S - CAN bus transceivers	Rev: 2C
Date: Thursday, June 24, 2004	Sheet 3 of 18	


Motorola ColdFire™
Microprocessor MCF5475
MCF5475 388 TEPBGA
U5
NOTE: please place the above capacitors as close as possible to pin D2 on U5.
NOTE: U5 (MCF5475) is socketed in a Wells-CTI socket, part number 8127-388-1E-00.
R6 is not populated.
USB test point
TP1
Motorola SPS TSPG -TECD ColdFire Group
Validation Board for MCF547x & MCF548x Microprocessors
Document Number 63A11380S - MCF5475 signals and bypass capacitors
Rev 2C
Thursday, June 24, 2004
Sheet 4 of 18

Place RP13 to RP20, RP38, RP46 as close to J1 as possible.

Place RP38 to RP46 as close to J1 as possible.

Micron MT2VDDT832UG-75 or SMT SM5320835D4F0CW/G/L DDR DIMM's
DDR DRAM DIMM 100pin socket part number - Molex 87630-0002.

NOTE: please place resistor packs RP34, RP36 & RP37 as close as possible to U5, the MCF5475, on sheet 4 of the schematics.

NOTE: please place resistor packs RP31, RP32 & RP35 as close as possible to U5, the MCF5475, on sheet 4 of the schematics.

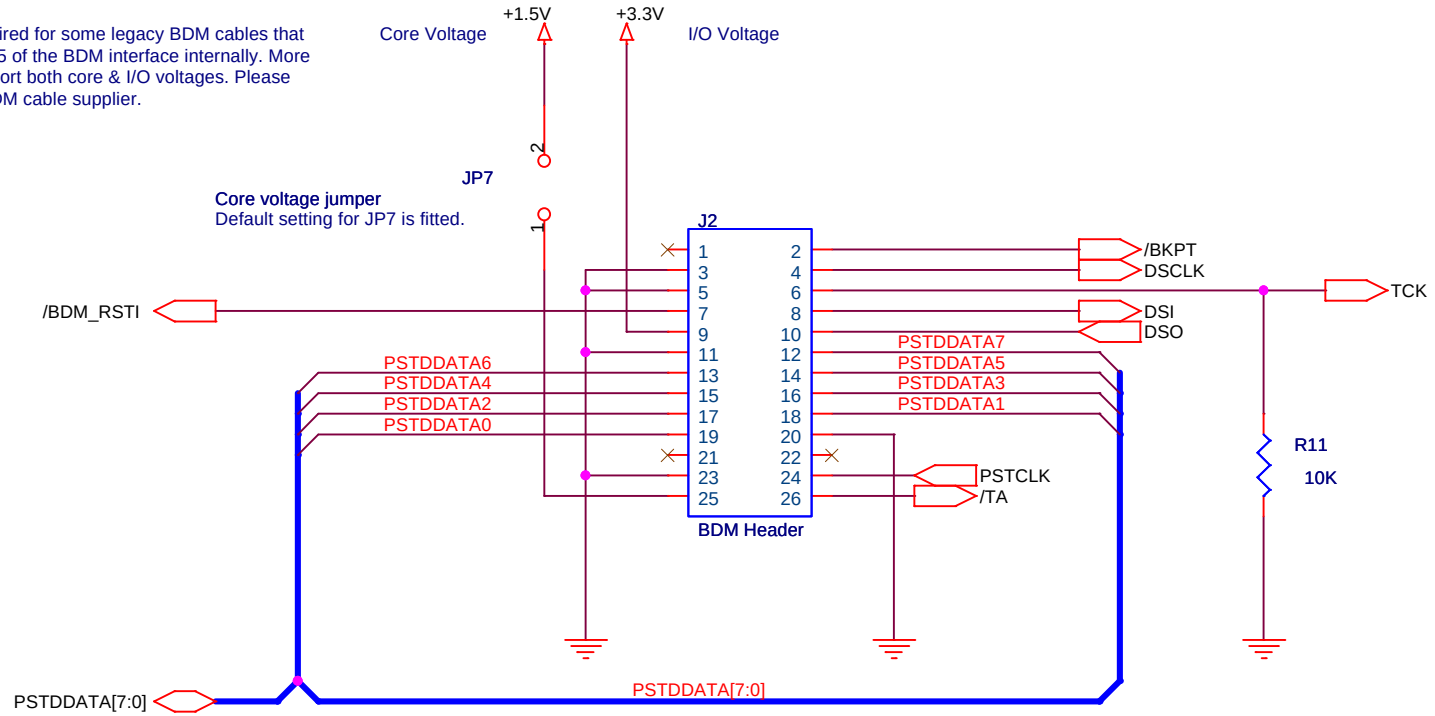
NOTE: please place the capacitors below close to pin 50 on the DDR DRAM DIMM.

NOTE: Please place VSense as close to the center of the VTT plane as possible.

RP45 is not populated.

Motorola SPS TSPG -TECD ColdFire Group		
Title: Validation Board for MCF547x & MCF548x Microprocessors		
Size: C	Document Number: 63A11380S - DDR DRAM DIMM	Rev: 2C
Date: Thursday, June 24, 2004	Sheet 5 of 18	

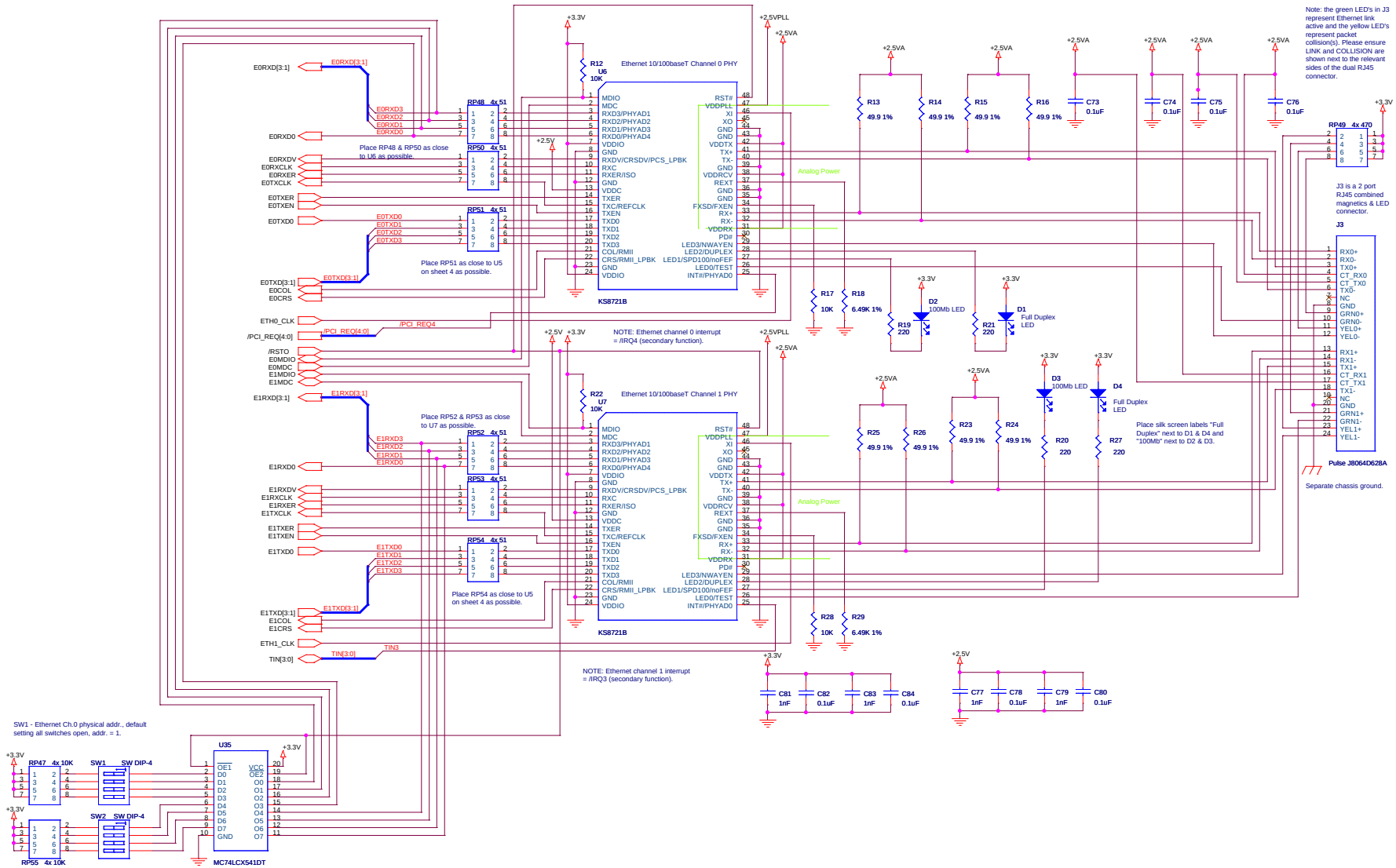
NOTE: JP7 is required for some legacy BDM cables that connect pins 9 & 25 of the BDM interface internally. More recent cables support both core & I/O voltages. Please check with your BDM cable supplier.



NOTE: 4.7K pull up resistors are used on signals /BKPT, DSCLK, DSI, DSO & /RSTI. A 1K pull up is used for -TA. See page 14 of the schematics.

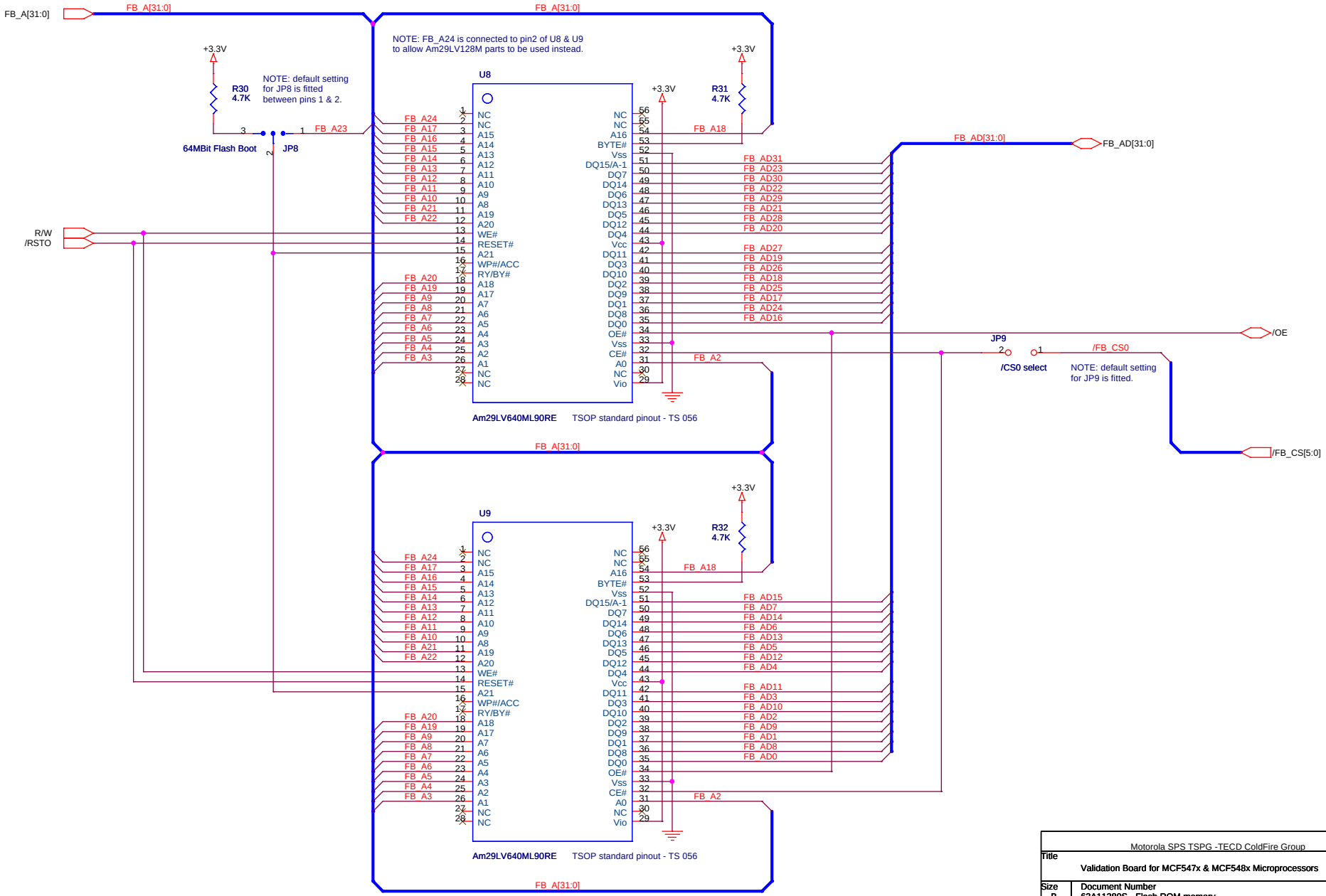
IMPORTANT NOTE: ONLY 3.3V BDM debugging cables can be used with MCF547x/8x processors.

Motorola SPS TSPG -TECD ColdFire Group		
Title: Validation Board for MCF547x & MCF548x Microprocessors		
Size: A	Document Number: 63A11380S - BDM/JTAG connector	Rev: 2C
Date: Thursday, June 24, 2004	Sheet 6 of 18	



Motorola SPS TSPG -TECD ColdFire Group

Title	Validation Board for MCF547x & MCF548x Microprocessors	
Size C	Document Number 63A11380S - Dual 10/100BaseT Ethernet transceivers	Rev 2C
Date: Thursday, June 24, 2004	Sheet 7 of 18	


FB_A[31:0]
FB_A[31:0]
NOTE: FB_A24 is connected to pin2 of U8 & U9
to allow Am29LV128M parts to be used instead.
+3.3V
R30
4.7K
NOTE: default setting
for JP8 is fitted
between pins 1 & 2.
64MBit Flash Boot
JP8
FB_A23
U8
R31
4.7K
FB_A18
FB_AD[31:0]
FB_AD[31:0]
R/W
/RSTO
Am29LV640ML90RE
TSOP standard pinout - TS 056
JP9
/CS0 select
/FB_CS0
NOTE: default setting
for JP9 is fitted.
/OE
/FB_CS[5:0]
U9
R32
4.7K
Motorola SPS TSPG -TECD ColdFire Group
Validation Board for MCF547x & MCF548x Microprocessors
Size B
Document Number
63A11380S - Flash ROM memory
Rev 2C
Date: Thursday, June 24, 2004
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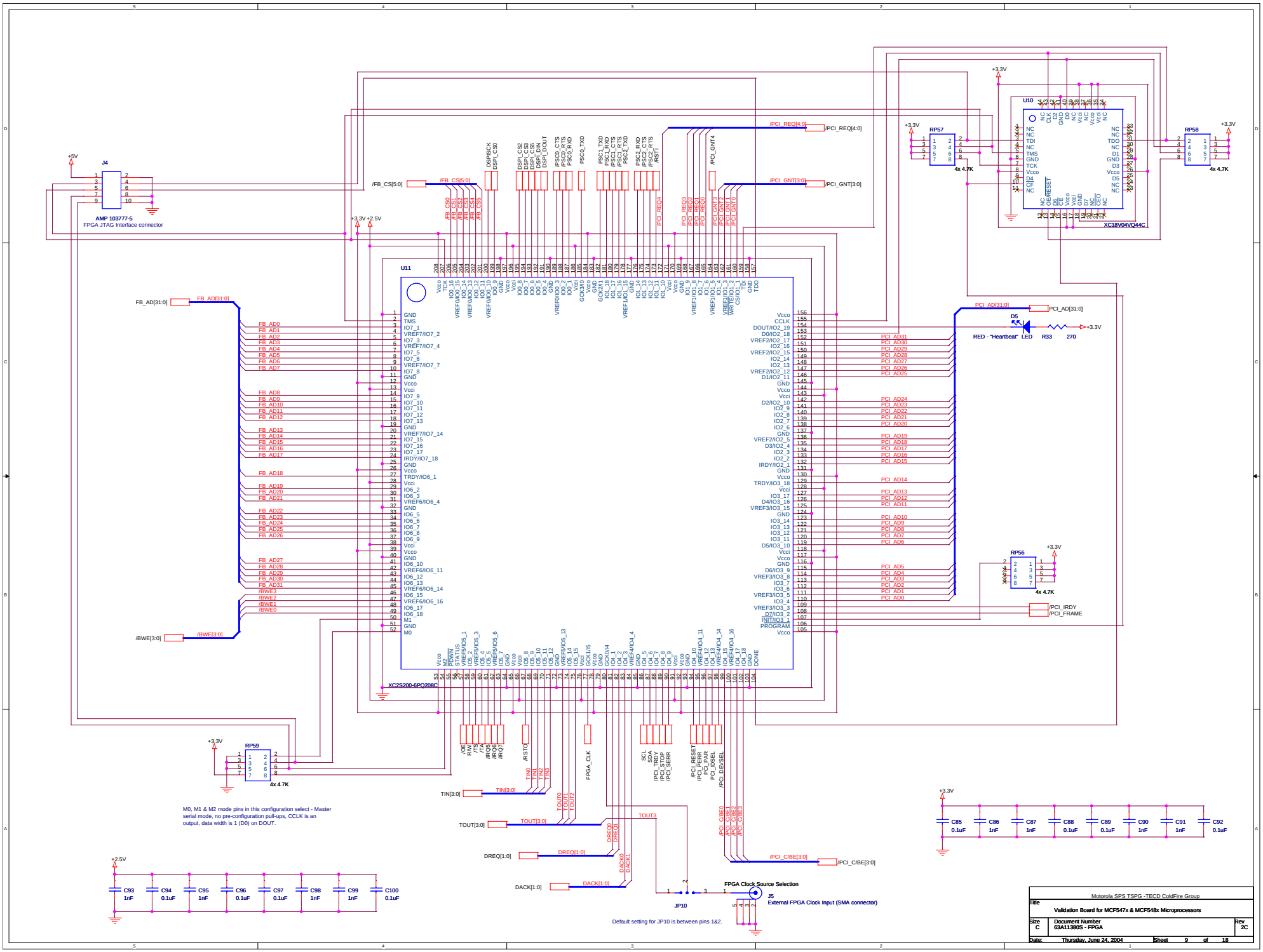
J4
AMP 103777-5
FPGA JTAG Interface connector
U11
XC2S200-6PQ208C
U10
XC18V04VQ44C
RP57
RP58
RP56
RP59
4x 4.7K
D5
RED - "Heartbeat" LED
R33
270
JP10
J5
External FPGA Clock Input (SMA connector)
FPGA Clock Source Selection
Default setting for JP10 is between pins 1&2.
M0, M1 & M2 mode pins in this configuration select - Master serial mode, no pre-configuration pull-ups, CCLK is an output, data width is 1 (D0) on DOUT.
C85 0.1uF
C86 1nF
C87 1nF
C88 0.1uF
C89 0.1uF
C90 1nF
C91 1nF
C92 0.1uF
C93 1nF
C94 0.1uF
C95 1nF
C96 0.1uF
C97 0.1uF
C98 1nF
C99 1nF
C100 0.1uF
Motorola SPS TSPG -TECD ColdFire Group
Validation Board for MCF547x & MCF548x Microprocessors
Document Number 63A11380S - FPGA
Rev 2C
Thursday, June 24, 2004
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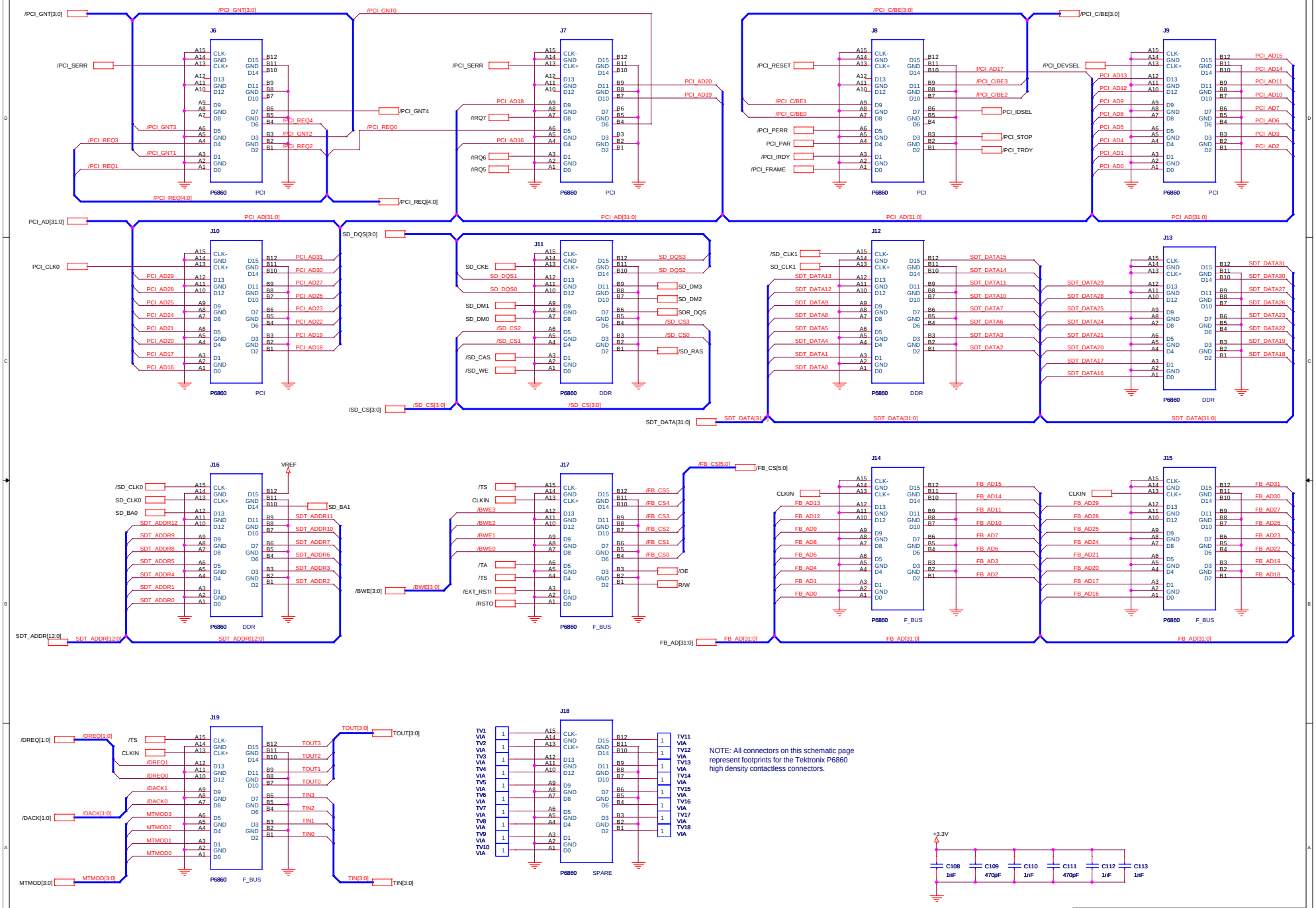


Motorola SPS TSPG -TECD ColdFire Group

Title	Validation Board for the MCF547x & MCF548x Microprocessors	
Size C	Document Number 63A11380S - Logic Analyser connectors	Rev 2C
Date: Thursday, June 24, 2004	Sheet 10 of 18	

NOTE: PCI slot 1 uses /PCI_REQ1 & /PCI_GNT1 signals and PCI slot 2 uses /PCI_REQ2 & /PCI_GNT2 signals. PCI slot 1 has IDSEL connected to PCI_AD17 and PCI slot 2 has IDSEL connected to PCI_AD18. Both PCI connectors are setup for 3.3V operation and +/-12V is supplied via P3 to each PCI connector. Finally, JTAG is unusable on both PCI connectors.

2-way Bare Wire Power Connector

P3

Augat 25V-02

Universal 32-bit PCI Connector

PCI Slot 1

PCI socket part number - AMP 145167-4

J20

Universal 32-bit PCI Connector

PCI Slot 2

PCI socket part number - AMP 145167-4

J21

RP60 4x 10K

RP61 4x 10K

R36 5.1K

R34 5.1K

R37 5.1K

R35 5.1K

R38 75

R39 75

C117 0.1uF

C119 0.1uF

C118 0.1uF

C120 0.1uF

C121 C122 C123 C124 C125 C126 C127 C128 C129 C130 C131 C132 0.1uF / 1nF

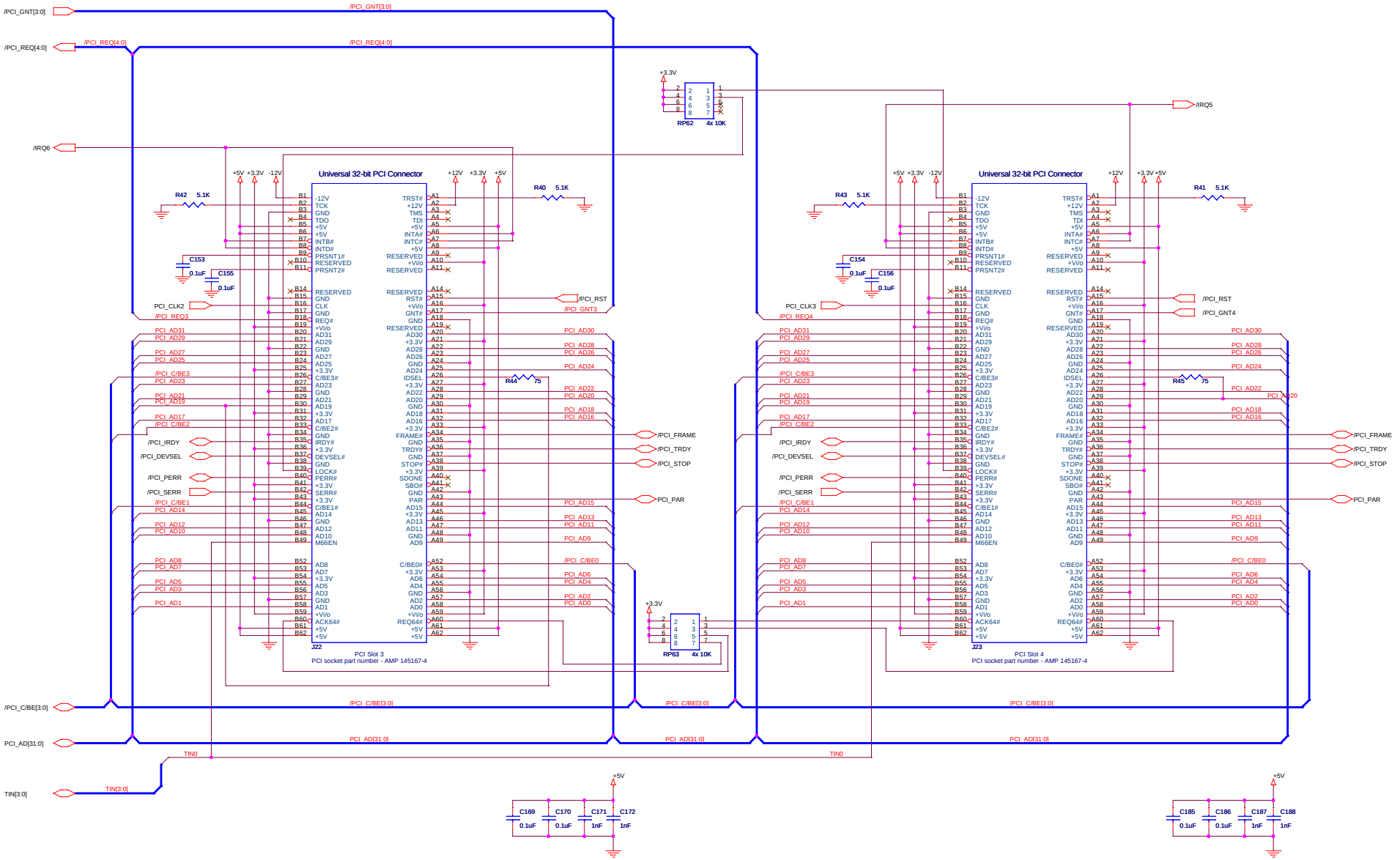
C133 C134 C135 C136 0.1uF / 1nF

C137 C138 C139 C140 C141 C142 C143 C144 C145 C146 C147 C148 0.1uF / 1nF

C149 C150 C151 C152 0.1uF / 1nF

Motorola SPS TSPG -TECD ColdFire Group	
Title	Validation Board for MCF547x & MCF548x Microprocessors
Size C	Document Number 63A11380S - 2x PCI bus connectors
Rev	2C
Date:	Thursday, June 24, 2004
Sheet	11 of 18

NOTE: PCI slot 3 uses /PCI_REQ3 & /PCI_GNT3 signals and PCI slot 4 uses /PCI_REQ4 & /PCI_GNT4 signals. PCI slot 3 has IDSEL connected to PCI_AD19 and PCI slot 4 has IDSEL connected to PCI_AD20. Both PCI connectors are setup for 3.3V operation and +/-12V is supplied via P3 (sheet 11) to each PCI connector. Finally, JTAG is unusable on both PCI connectors.



Motorola SPS TSPG -TECD ColdFire Group		
Title: Validation Board for MCF547x & MCF548x Microprocessors		
Size: C	Document Number: 63A11380S - Second 2x PCI bus connectors	Rev: 2C
Date: Thursday, June 24, 2004	Sheet 12 of 18	

NOTE: place the circuit bounded by the dotted line as close as possible to pin A19 on the CPU - sheet 4 U5. Forming a filter for the PLL of U5.

+1.5VP
R46 10
NOTE: R46 is 1206 size.
PLLVDD
C189 10uF
C190 100pF
PLL filtering.

DC voltage input range +7 to +14V & 1.5A min.

P4 Power Jack Connector - 2.1mm diameter
Switchcraft RAPC722
POWER SW SLIDE-SPST(Board Edge)
SW3
2-way Bare Wire Power Connector
P5
Augat 25V-02
J24
+12V
GND
GND
+5V
PC disk drive power connector

NOTE: the positive terminal of each power connector must be shown on the silkscreen of the PCB

F1 5A Fast blow.
C193 0.1uF
C194 1nF
C195 1000uF 35V

3.3V Regulator
U12 LM2596S-3.3
VIN VOUT ~ON/OFF GND TAB FB
L1 25uH
D8 MBRS340T3
C191 330uF
C192 0.1uF
R47 270
D9
+3.3V GREEN POWER LED

JP11 SHOULD BE INSTALLED DURING ASSEMBLY
JP11
2 PIN JUMPER
+3.3VP
+3.3V

5.0V Regulator
U13 LM2596S-5
L2 25uH
D14 MBRS340T3
C196 330uF
C197 0.1uF
R48 560
D15
+5V GREEN POWER LED
D13 MBRS340T3

NOTE: Diodes prevent excessive difference between 3.3V & 2.5V rails, at power up
D7 MRA4003T3
D6 MBRS340T3

NOTE: Schottky Diode prevents excessive difference between 3.3V & 2.5V rails, at power down
D10 MBRS340T3

NOTE: Diodes prevent excessive difference between 2.5V & 1.5V rails, at power up
D11 MRA4003T3
D12 MRA4003T3

NOTE: Schottky Diode prevents excessive difference between 2.5V & 1.5V rails, at power down
D16 MBRS340T3

NOTE: VREF = 1.25V or 1,65V (Half of selected supply)
VSense = VTT = termination resistor supply
(Place VSense in the centre of the VTT plane)

JP5 +2.5V/+3.3V
Default setting for JP5 DIMM socket voltage selection is between pins 1&2 DDR DRAM setting.

U14 LP2995M
VREF VSense NC GND VSENSE VREF VTT PVIN AVIN VDDQ RAMVdd
C199 0.1uF
C200 330uF
C198 330uF
C201 47uF

1.5V Regulator
U15 LT1086CM
VIN ADJ VOUT
C202 47uF
R50 120
R51 22
C203 330uF
C204 0.1uF
D17
+1.5V GREEN POWER LED

JP12 SHOULD BE INSTALLED DURING ASSEMBLY
JP12
2 PIN JUMPER
+1.5VP
+1.5V

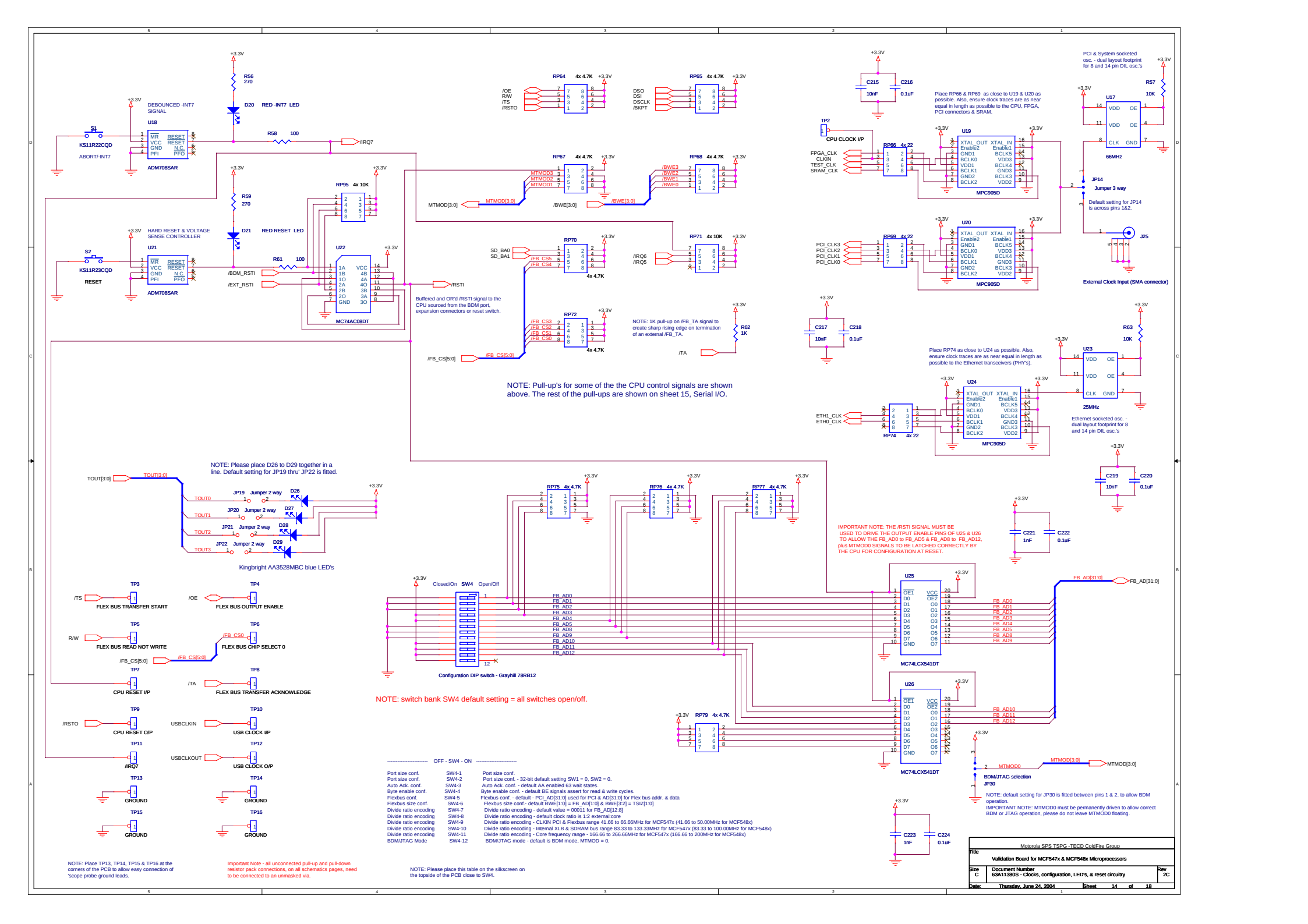
JP13 SHOULD BE INSTALLED DURING ASSEMBLY
JP13
2 PIN JUMPER
+2.5VP

2.5V Regulator
U16 LM2596S-ADJ
R52 470 1%
R53 15 1%
L3 25uH
R55 470 1%
D18 MBRS340T3
C205 0.1uF
C206 330uF
C207 0.1uF
R54 220
D19
+2.5V GREEN POWER LED
C209 0.1uF
C210 47uF
C211 0.1uF
C212 0.1uF
C213 1nF
C214 47uF

STEWARD HI1206T500R-00
FB1
FB2
FB3
Ethernet Ground
System Ground

All resistors are 0805 body size.
All caps less than 1uF are 0805 body size and COG/NPO dielectric material.

Motorola SPS TSPG -TECD ColdFire Group		
Title: Validation Board for MCF547x & MCF548x Microprocessors		
Size: B	Document Number: 63A11380S - DC to DC power supply	Rev: 2C
Date: Thursday, June 24, 2004	Sheet 13 of 18	


DEBOUNCED -INT7 SIGNAL
D20 RED -INT7 LED
R56 270
R58 100
/IRQ7
S1
KS11R22CQD
ABORT/-INT7
U18
ADM708SAR
HARD RESET & VOLTAGE SENSE CONTROLLER
R59 270
D21 RED RESET LED
R61 100
S2
KS11R23CQD
RESET
U21
ADM708SAR
RP95 4x 10K
U22
MC74AC08DT
/BDM_RSTI
/EXT_RSTI
/RSTI
Buffered and OR'd /RSTI signal to the CPU sourced from the BDM port, expansion connectors or reset switch.
RP64 4x 4.7K
/OE
R/W
/TS
/RSTO
RP65 4x 4.7K
DSO
DSI
DSCLK
/BKPT
RP67 4x 4.7K
MTMOD3
MTMOD2
MTMOD1
MTMOD[3:0]
RP68 4x 4.7K
/BWE3
/BWE2
/BWE1
/BWE0
/BWE[3:0]
RP70 4x 4.7K
SD_BA0
SD_BA1
/FB_CS5
/FB_CS4
RP71 4x 10K
/IRQ6
/IRQ5
RP72 4x 4.7K
/FB_CS3
/FB_CS2
/FB_CS1
/FB_CS0
/FB_CS[5:0]
NOTE: 1K pull-up on /FB_TA signal to create sharp rising edge on termination of an external /FB_TA.
R62 1K
/TA
NOTE: Pull-up's for some of the the CPU control signals are shown above. The rest of the pull-ups are shown on sheet 15, Serial I/O.
C215 10nF
C216 0.1uF
Place RP66 & RP69 as close to U19 & U20 as possible. Also, ensure clock traces are as near equal in length as possible to the CPU, FPGA, PCI connectors & SRAM.
TP2
CPU CLOCK I/P
FPGA_CLK
CLKIN
TEST_CLK
SRAM_CLK
RP66 4x 22
U19
MPC905D
PCI_CLK3
PCI_CLK2
PCI_CLK1
PCI_CLK0
RP69 4x 22
U20
MPC905D
PCI & System socketed osc. - dual layout footprint for 8 and 14 pin DIL osc.'s
R57 10K
U17
66MHz
JP14
Jumper 3 way
Default setting for JP14 is across pins 1&2.
J25
External Clock Input (SMA connector)
C217 10nF
C218 0.1uF
Place RP74 as close to U24 as possible. Also, ensure clock traces are as near equal in length as possible to the Ethernet transceivers (PHY's).
R63 10K
U23
25MHz
U24
MPC905D
ETH1_CLK
ETH0_CLK
RP74 4x 22
Ethernet socketed osc. - dual layout footprint for 8 and 14 pin DIL osc.'s
C219 10nF
C220 0.1uF
C221 1nF
C222 0.1uF
IMPORTANT NOTE: THE /RSTI SIGNAL MUST BE USED TO DRIVE THE OUTPUT ENABLE PINS OF U25 & U26 TO ALLOW THE FB_AD0 to FB_AD5 & FB_AD8 to FB_AD12, plus MTMOD0 SIGNALS TO BE LATCHED CORRECTLY BY THE CPU FOR CONFIGURATION AT RESET.
NOTE: Please place D26 to D29 together in a line. Default setting for JP19 thru' JP22 is fitted.
TOUT[3:0]
JP19 Jumper 2 way D26
JP20 Jumper 2 way D27
JP21 Jumper 2 way D28
JP22 Jumper 2 way D29
Kingbright AA3528MBC blue LED's
RP75 4x 4.7K
RP76 4x 4.7K
RP77 4x 4.7K
Closed/On SW4 Open/Off
FB_AD0
FB_AD1
FB_AD2
FB_AD3
FB_AD4
FB_AD5
FB_AD8
FB_AD9
FB_AD10
FB_AD11
FB_AD12
Configuration DIP switch - Grayhill 78RB12
NOTE: switch bank SW4 default setting = all switches open/off.
U25
MC74LCX541DT
U26
MC74LCX541DT
FB_AD[31:0]
RP79 4x 4.7K
TP3 /TS FLEX BUS TRANSFER START
TP4 /OE FLEX BUS OUTPUT ENABLE
TP5 R/W FLEX BUS READ NOT WRITE
TP6 /FB_CS0 FLEX BUS CHIP SELECT 0
TP7 CPU RESET I/P
TP8 /TA FLEX BUS TRANSFER ACKNOWLEDGE
TP9 /RSTO CPU RESET O/P
TP10 USBCLKIN USB CLOCK I/P
TP11 /IRQ7
TP12 USBCLKOUT USB CLOCK O/P
TP13 GROUND
TP14 GROUND
TP15 GROUND
TP16 GROUND
NOTE: Place TP13, TP14, TP15 & TP16 at the corners of the PCB to allow easy connection of 'scope probe ground leads.
Important Note - all unconnected pull-up and pull-down resistor pack connections, on all schematics pages, need to be connected to an unmasked via.
NOTE: Please place this table on the silkscreen on the topside of the PCB close to SW4.
OFF - SW4 - ON
Port size conf. SW4-1 Port size conf.
Port size conf. SW4-2 Port size conf. - 32-bit default setting SW1 = 0, SW2 = 0.
Auto Ack. conf. SW4-3 Auto Ack. conf. - default AA enabled 63 wait states.
Byte enable conf. SW4-4 Byte enable conf. - default BE signals assert for read & write cycles.
Flexbus conf. SW4-5 Flexbus conf. - default - PCI_AD[31:0] used for PCI & AD[31:0] for Flex bus addr. & data
Flexbus size conf. SW4-6 Flexbus size conf.- default BWE[1:0] = FB_AD[1:0] & BWE[3:2] = TSIZ[1:0]
Divide ratio encoding SW4-7 Divide ratio encoding - default value = 00011 for FB_AD[12:8]
Divide ratio encoding SW4-8 Divide ratio encoding - default clock ratio is 1:2 external:core
Divide ratio encoding SW4-9 Divide ratio encoding - CLKIN PCI & Flexbus range 41.66 to 66.66MHz for MCF547x (41.66 to 50.00MHz for MCF548x)
Divide ratio encoding SW4-10 Divide ratio encoding - Internal XLB & SDRAM bus range 83.33 to 133.33MHz for MCF547x (83.33 to 100.00MHz for MCF548x)
Divide ratio encoding SW4-11 Divide ratio encoding - Core frequency range - 166.66 to 266.66MHz for MCF547x (166.66 to 200MHz for MCF548x)
BDM/JTAG Mode SW4-12 BDM/JTAG mode - default is BDM mode, MTMOD = 0.
C223 1nF
C224 0.1uF
BDM/JTAG selection
JP30
MTMOD0
MTMOD[3:0]
NOTE: default setting for JP30 is fitted between pins 1 & 2. to allow BDM operation.
IMPORTANT NOTE: MTMOD0 must be permanently driven to allow correct BDM or JTAG operation, please do not leave MTMOD0 floating.
Motorola SPS TSPG -TECD ColdFire Group
Title
Validation Board for MCF547x & MCF548x Microprocessors
Size C
Document Number 63A11380S - Clocks, configuration, LED's, & reset circuitry
Rev 2C
Date: Thursday, June 24, 2004
Sheet 14 of 18

NOTE: place U28 (IRDA transceiver) on the edge of the EVB.

Default setting for JP23 & 24 is fitted.

PSC2_TXD Isolation JP23

PSC2_TXD
PSC2_RXD

JP24

PSC2_RXD Isolation JP25

IRDA mode select

U28 TFDU6102
Vcc2 IRED Anode
IRED Cathode
Txd
Rxd
SD
Vcc1
Mode
GND

Default setting for JP25 is between pins 1&2.

C228 1nF
C229 0.1uF

U27 MAX3225CAP or ICL3225CA
READY
C1+
V+
C1-
C2+
C2-
V-
T2OUT
R2IN
R2OUT
FORCEOFF
VCC
GND
T1OUT
R1IN
R1OUT
FORCEON
T1IN
T2IN
INVALID

C227 0.1uF
C230 0.1uF
C231 0.1uF
C232 0.1uF
C225 1nF
C226 0.1uF

RS232 Transceiver.

P6 TERMINAL PORT 9-WAY D-TYPE (Female)

PSC0_RXD
PSC0_TXD
/PSC0_RTS
/PSC0_CTS

JP26 /PSC0_RTS Isolation
JP27 /PSC0_CTS Isolation

Default setting for JP26 & JP27 is fitted.

U29 MAX3225CAP or ICL3225CA

C233 0.1uF
C234 0.1uF
C235 0.1uF
C236 0.1uF
C237 1nF
C238 0.1uF

RS232 Transceiver.

P7 AUXILIARY PORT 9-WAY D-TYPE (Female)

PSC1_RXD
PSC1_TXD
/PSC1_RTS
/PSC1_CTS

JP28 /PSC1_RTS Isolation
JP29 /PSC1_CTS Isolation

Default setting for JP28 & JP29 is fitted.

TIN[3:0]
TOUT[3:0]
/DREQ[1:0]
E1MDC
TIN0
TIN1
TIN2
TIN3
TOUT0
TOUT1
/DREQ0
/DREQ1
TOUT2
TOUT3

J26 SAMTEC MTMM-126-04-G-D-148
E1MDIO
PSC3_TXD
/PSC3_CTS
DSPI_CS2
DSPI_CS5
/DACK0
/DACK1
PSC3_RXD
/PSC3_RTS
DSPI_CS3
/DACK[1:0]

NOTE: the I2C bus on the MCF547x/8x processor is 3.3V tolerant only. If connection to a 5V system is required high frequency voltage level shifters will be required between the peripheral and processor.

RP81 4x 4.7K
SCL
SDA
J28 0.1" pitch BERG connector
NOT POPULATED AT ASSEMBLY.

U30 AT24C02AN-10TI-2.7 2Kb Serial EEPROM
A0
A1
A2
GND
VCC
WP
SCL
SDA

Serial EEPROM address =2 on I2C bus.

J27 QSPI connector 0.1 pitch
DSPI_CS0
DSPI_CS2
DSPI_CS3
DSPI_CS5
DSPISCK
DSPI_DIN
DSPI_DOUT
DSPI_CS0
DSPI_CS2
DSPI_CS3
DSPI_CS5

RP80 4x 4.7K

NOT POPULATED AT ASSEMBLY.

NOTE: Pull-up's for some of the the CPU control signals. The rest of the pull-ups are shown on sheet 14, Reset, Configuration & Clocks.

RP82 4x 4.7K
TIN3
TIN2
TIN1
TIN0
TIN[3:0]
/SD_CS[3:0]

RP83 4x 4.7K +2.5V
/SD_CS3
/SD_CS2

RP84 4x 4.7K
/PSC3_CTS
/PSC3_RTS

RP85 4x 4.7K
/PCI_REQ4
/PSC2_RTS
/PSC2_CTS

RP86 4x 4.7K
/PSC1_RTS
/PSC1_CTS
/PSC0_RTS
/PSC0_CTS

RP87 4x 4.7K
/DACK1
/DACK0
/DREQ1
/DREQ0
/DACK[1:0]
/DREQ[1:0]

/PCI_REQ[4:0]

RP88 4x 4.7K
/PCI_REQ3
/PCI_REQ2
/PCI_REQ1
/PCI_REQ0
/PCI_REQ[4:0]

RP89 4x 4.7K
/PCI_TRDY
/PCI_RST
/PCI_GNT[3:0]

RP90 4x 4.7K
/PCI_GNT3
/PCI_GNT2
/PCI_GNT1
/PCI_GNT0

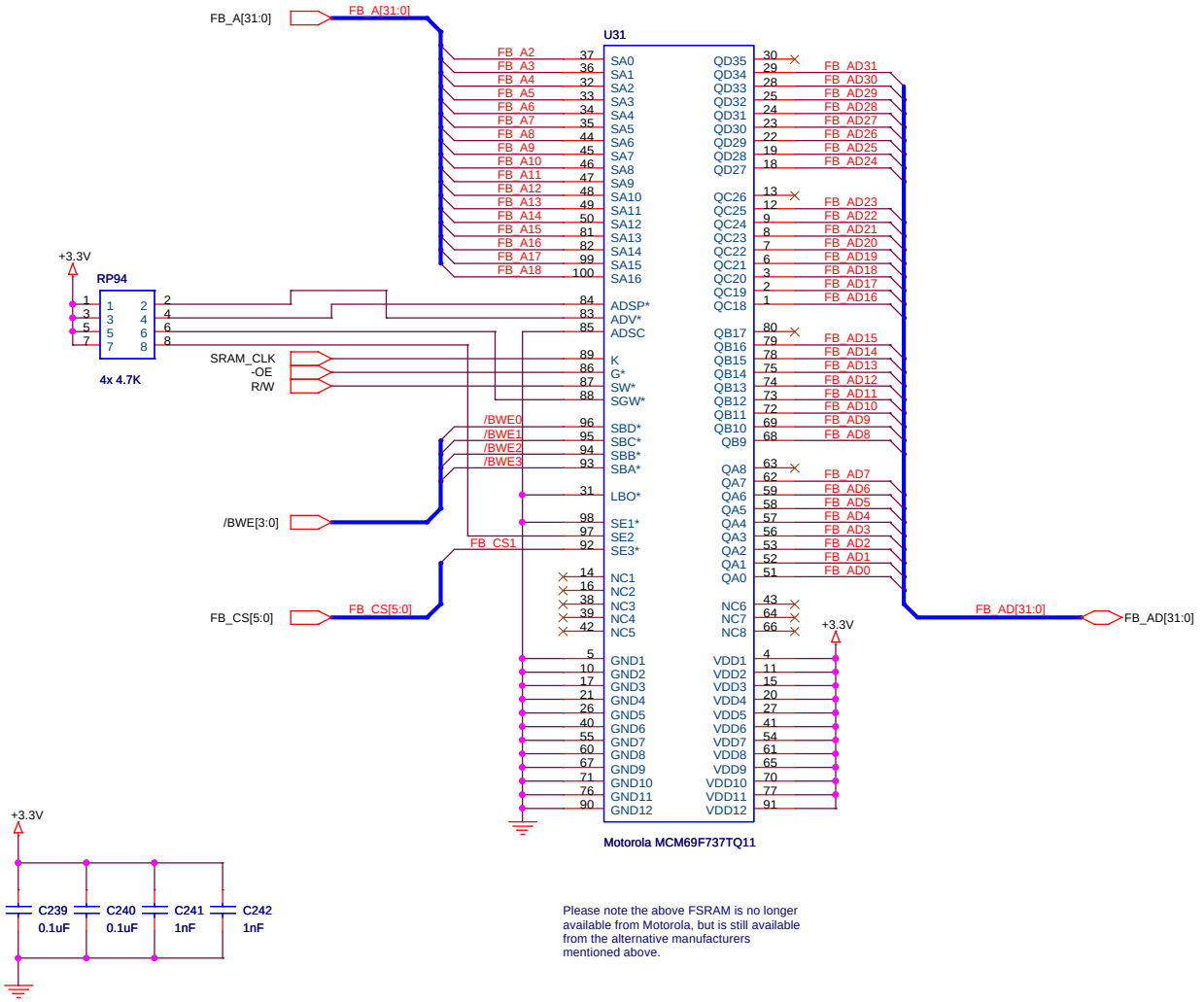
RP91 4x 4.7K
/PCI_STOP
/PCI_PERR
/PCI_SERR
PCI_PAR

RP92 4x 4.7K
/PCI_GNT4
/PCI_FRAME
/PCI_IRDY
/PCI_DEVSEL

RP93 4x 4.7K
/PCI_C/BE3
/PCI_C/BE2
/PCI_C/BE1
/PCI_C/BE0
/PCI_C/BE[3:0]

Motorola SPS TSPG -TECD ColdFire Group	
Title: Validation Board for MCF547x & MCF548x Microprocessors	
Size: C	Document Number: 63A11380S - RS232 & IRDA transceivers + I2C & QSPI connectors
Rev: 2C	
Date: Thursday, June 24, 2004	Sheet 15 of 18

NOTE: Alternative FSRAM's with the same PCB footprint and functionality are :- Samsung K7B403625M, Cypress CY7C1345B, IDT 71V3577 & Micron MT58L128L36F1.



Please note the above FSRAM is no longer available from Motorola, but is still available from the alternative manufacturers mentioned above.

Motorola SPS TSPG -TECD ColdFire Group		
Title: Validation Board for MCF547x & MCF548x Microprocessors		
Size: B	Document Number: 63A11380S - FSRAM	Rev: 2C
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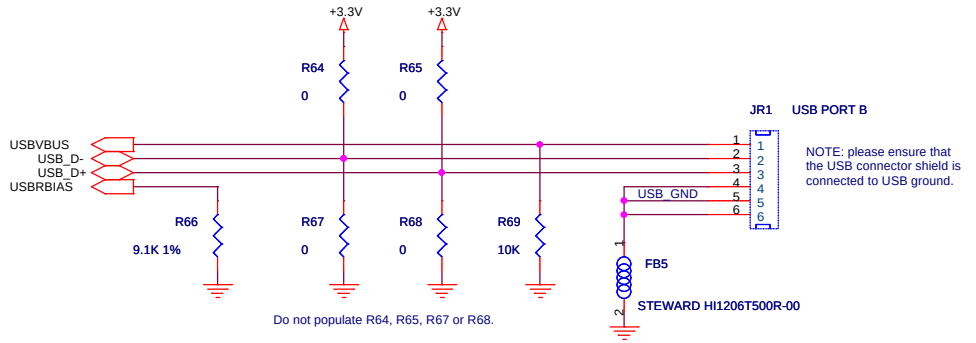
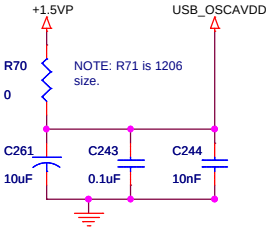
NOTE: there must be a 90ohm differential phase impedance between signals USB_D- & USB_D+. Please couple these traces as soon as they leave U5 (sheet4) through to JR1.

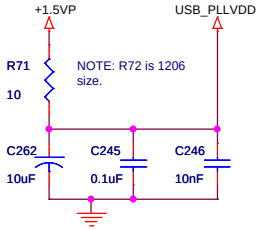


NOTE: please ensure that the USB connector shield is connected to USB ground.

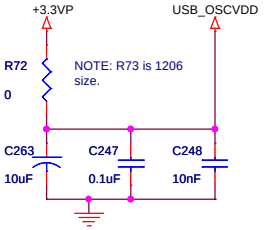
Do not populate R64, R65, R67 or R68.



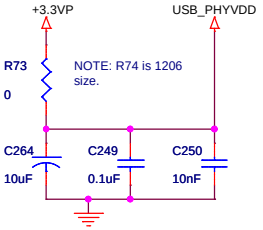
NOTE: place the circuit above as close as possible to pin AD15 on the MCF5475, CPU - U5, sheet 4. As this is the filter for USB_OSCAVDD.



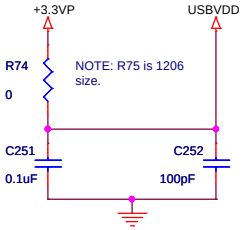
NOTE: place the circuit above as close as possible to pin AD16 on the MCF5475, CPU - U5, sheet 4. As this is the filter for USB_PLLVDD.



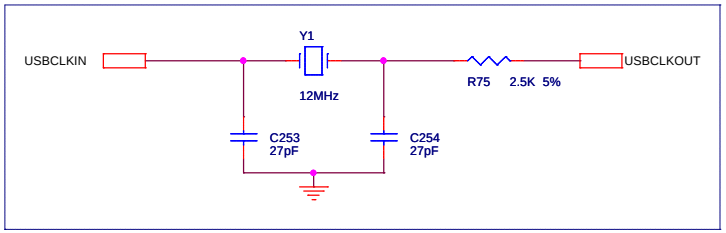
NOTE: place the circuit above as close as possible to pin AC13 on the MCF5475, CPU - U5, sheet 4. As this is the filter for USB_OSCVDD.



NOTE: place the circuit above as close as possible to pin AC16 on the MCF5475, CPU - U5, sheet 4. As this is the filter for USB_PHYVDD.



NOTE: place the circuit above as close as possible to pins AE18 on the MCF5475, CPU - U5, sheet 4. As this is the filter for USBVDD.



NOTE: place the circuit bounded by the dotted line as close as possible to pins AF14 & AF15 on the MCF5475, CPU - U5, sheet 4.

Motorola SPS TSPG -TECD ColdFire Group

Title: Validation Board for MCF547x & MCF548x Microprocessors

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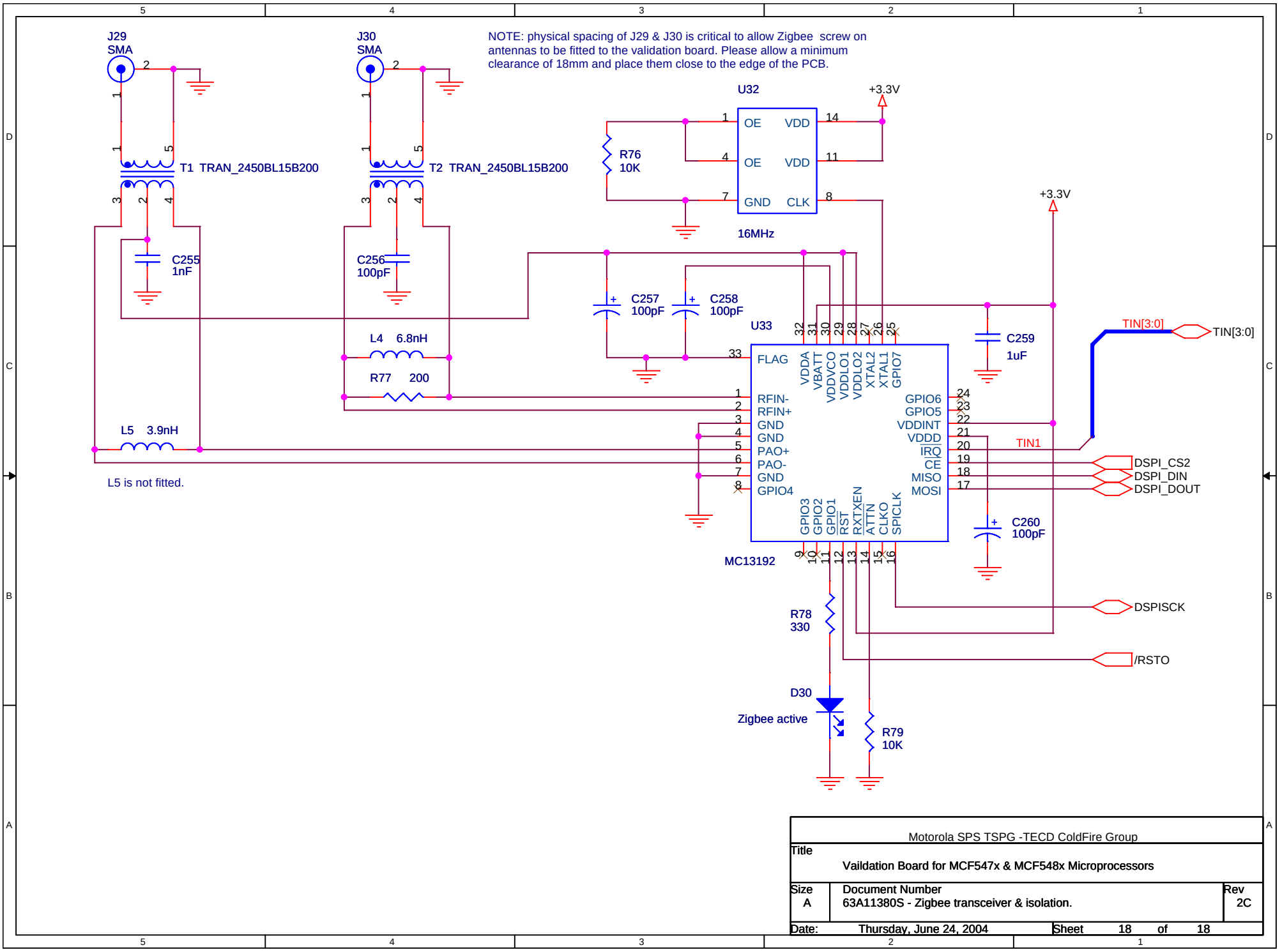
J29
SMA
J30
SMA
NOTE: physical spacing of J29 & J30 is critical to allow Zigbee screw on antennas to be fitted to the validation board. Please allow a minimum clearance of 18mm and place them close to the edge of the PCB.
T1 TRAN_2450BL15B200
T2 TRAN_2450BL15B200
C255
1nF
C256
100pF
U32
+3.3V
R76
10K
OE
VDD
OE
VDD
GND
CLK
16MHz
C257
100pF
C258
100pF
U33
L4 6.8nH
R77 200
L5 3.9nH
L5 is not fitted.
FLAG
RFIN-
RFIN+
GND
GND
PAO+
PAO-
GND
GPIO4
VDDA
VBATT
VDDVCO
VDDLO1
VDDLO2
XTAL2
XTAL1
GPIO7
GPIO6
GPIO5
VDDINT
VDDD
IRQ
CE
MISO
MOSI
GPIO3
GPIO2
GPIO1
RST
RXTXEN
ATTN
CLKO
SPICLK
MC13192
C259
1uF
C260
100pF
TIN[3:0]
TIN1
DSPI_CS2
DSPI_DIN
DSPI_DOUT
DSPISCK
/RSTO
R78
330
D30
Zigbee active
R79
10K
Motorola SPS TSPG -TECD ColdFire Group
Title
Vaildation Board for MCF547x & MCF548x Microprocessors
Size
A
Document Number
63A11380S - Zigbee transceiver & isolation.
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