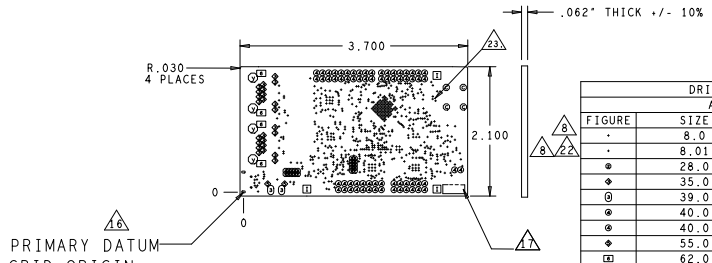
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	ORIGINAL RELEASE	04-25-16	K.T.
	B	AS PER ECO65041	05-17-16	K.T.
	C	AS PER ECO67700	09-29-16	K.T.

NOTES (UNLESS OTHERWISE SPECIFIED)

1. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-6012 CLASS 2 (LATEST REVISION).
2. THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.
3. BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101B-26, 83 or 98
   Tg - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
   Td - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.
4. COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A'
5. CHARACTERISTIC IMPEDANCE - REFER TO DETAIL B
6. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .003"/.0035"
7. PLATING FINISH - BOTH SIDES ENIG (ELECTROLESS NICKEL IMMERSION GOLD):
   .05080-.232 MICRON (2-8 MICROINCH) OF GOLD OVER
   2.540-6.350 MICRON (100-250 MICROINCH) OF NICKEL.
8. ALL THROUGH HOLE VIAS MAY BE PLATED SHUT.
9. SOLDERMASK - GREEN COLOR (TAIYO OR EQUIVALENT), BOTH SIDES.
   MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM NXP.
10. SILKSCREEN - WHITE EPOXY INK, BOTH SIDES. NO SILKSCREEN ON ANY EXPOSED COPPER FEATURE.
11. ELECTRICAL TEST - 100% IPCD356.
12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.
13. DRC'S MUST BE RUN ON THE GERBER BEFORE BUILDING BOARDS, UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY NXP.
14. TEARDROPS MAYBE ADDED AT THE FAB HOUSE TO ALL SIGNAL LAYERS.
15. 2 SOLDER SAMPLES TO BE PROVIDED.
16. BASIC GRID INCREMENT AT 1:1 IS .0001.
17. SUPPLIER MARKINGS - ON SOLDER SIDE ONLY, WHERE SHOWN.
    - MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0
18. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (PB)
19. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)
20. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP. ALL HOLE LOCATION TOLERANCES ARE TO BE +/-.002 IN REFERENCE TO THE PRIMARY DATUM.
21. FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURERS REQUIREMENTS. THE ADDITION OF RAILS AND .125" NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF CONTRACT MANUFACTURER.PANELIZATION MUST BE APPROVED BY CONTRACT MANUFACTURER.
22. THIS BOARD USES VIA-IN-PAD.
    A. VIA IN PAD TO BE FILLED WITH NON-CONDUCTIVE VIA FILL.
       LACKWERKE-PETERS PP2795 ARE EQUIVALENT AND MADE PLANNER TO THE PADS.
    B.OVERPLATE THE FILED VIA AND APPLY FINISH METAL TREATMENT.
23. INTENTIONAL SHORTS AT:
    SH1 GND & AGND (PASTE SHORT NOT A COPPER SHORT)
24. THE MANUFACTURE HAS THE OPTION TO ADD COPPER THIEVING ON OUTER AND INNER LAYERS, KEEP A MINIMUM DISTANCE OF .100" FROM ANY BOARD FEATURES.



DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
•	8.0	+0.0/-8.0	PLATED	649
•	8.01	+0.0/-8.0	PLATED	58
⊕	28.0	+2.0/-2.0	PLATED	20
◆	35.0	+2.0/-2.0	PLATED	24
0	39.0	+3.0/-3.0	PLATED	2
⊕	40.0	+2.0/-2.0	PLATED	2
⊕	40.0	+3.0/-3.0	PLATED	64
◆	55.0	+3.0/-3.0	PLATED	2
⊠	62.0	+3.0/-3.0	PLATED	4
⊕	48.0	+2.0/-2.0	NON-PLATED	4
1	125.0	+3.0/-3.0	NON-PLATED	3
9	128.0	+2.0/-2.0	NON-PLATED	4
•	34.0x26.0	+3.0/-3.0	PLATED	2
▭	59.0x33.0	+3.0/-3.0	PLATED	2

DETAIL B
IMPEDANCE REQUIREMENTS
IMPEDANCE TOLERANCE IS 10%

Layers	Single Ended		Differential					
	Trace Width (Mils)	Impedance (Ohms)	Trace Width (Mils)	Trace Spacing "Airgap" (Mils)	Impedance (Ohms)	Trace Width (Mils)	Trace Spacing "Airgap" (Mils)	Impedance (Ohms)
L1_PS	4	50	4	6.80	90	3.20	6.80	100
L4_SS	4	50	4	6.80	90	3.20	6.80	100

FINISHED Cu WEIGHT

LAYER 1	L1_PS	1/2 oz.
LAYER 2	L2_GND	1 oz.
LAYER 3	L3_PWR	1 oz.
LAYER 4	L4_SS	1/2 oz.

DETAIL A
LAYER STACKUP
SCALE: NONE

___ PUBI (PUBLIC INFORMATION)
X FIUO (NXP INTERNAL USE ONLY)
___ NCP (NXP CONFIDENTIAL PROPRIETARY)

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS ANGLES
.XX ±.01 ±0-30'
.XXX ±.005
✓ RMS ALL MACHINED SURFACES
BREAK ALL SHARP EDGES AND CORNERS.
REMOVE BURRS.
UNDERLINED DIM. NOT TO SCALE.
THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.

PART NO. 170-29217

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO NXP AND SHALL NOT BE USED FOR ENGINEERING DESIGN PROCUREMENT OR MANUFACTURE IN WHOLE OR IN PART WITHOUT THE CONSENT OF NXP.

APPROVALS	DATE
DRAWN MANIKANDAN M	09-29-16
CHECKED WANG BRIAN	09-29-16
DESIGN ENGINEER KINJALK	09-29-16

NXP
6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA

TITLE: PRINTED WIRING BOARD X-LS1012AFRDM

SIZE	CAD FILE NAME	DWG. NO.	REV
D	LAY-29217	FAB-29217	C

SCALE 1/1 DO NOT SCALE DRAWING SHEET 1 OF 1