

This figure displays a technical drawing of a Printed Wiring Board (PWB) design, specifically a layer stackup and drill chart. The drawing includes various dimensions, tolerances, and material specifications.

NOTES (UNLESS OTHERWISE SPECIFIED):

- THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-A-600 CLASS 2 (LATEST REVISION).
- THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.
- BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101B-26, 83 or 98.
Tg - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
Td - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.
- COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A'
- CHARACTERISTIC IMPEDANCE - NONE
- MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .005"/.005"
- PLATING FINISH - BOTH SIDES ENIG (ELECTROLESS NICKEL IMMERSION GOLD):
.05080-.232 MICRON (2-8 MICROINCH) OF GOLD OVER
2.540-6.350 MICRON (100-250 MICROINCH) OF NICKEL.
- ALL THROUGH HOLE VIAS MAY BE PLATED SHUT.
- SOLDERMASK - BLACK COLOR, BOTH SIDES.
MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM FREESCALE.
- SILKSCREEN - WHITE EPOXY INK, BOTH SIDES. NO SILK ON PADS.
- ELECTRICAL TEST - 100% IPCD356.
- PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.
- DRC'S MUST BE RUN ON THE GERBER BEFORE BUILDING BOARDS,
UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY FREESCALE.
- TEARDROPS MAYBE ADDED AT THE FAB HOUSE TO ALL SIGNAL LAYERS.
- 2 SOLDER SAMPLES TO BE PROVIDED.
- BASIC GRID INCREMENT AT 1:1 IS .0001.
- SUPPLIER MARKINGS - ON SOLDER SIDE ONLY, WHERE SHOWN.
MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0
- THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP **Pb**
- THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP **260°C**
- ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP.
ALL HOLE LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM.
- FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURERS REQUIREMENTS.
THE ADDITION OF RAILS AND .125" NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF CONTRACT MANUFACTURER. PANELIZATION MUST BE APPROVED BY CONTRACT MANUFACTURER.
- INTENTIONAL SHORT IN J11 BETWEEN NETS KL25_SWO_CLK AND SWO_CLK_TGTMCU.
INTENTIONAL SHORT ON J20 BETWEEN NETS P3V3_VREG AND P3V3
INTENTIONAL SHORT ON J14 BETWEEN NETS RST_TGTMCU AND RST_TGTMCU
5 INTENTIONAL DANGLING VIAS IN U7 AREA.
- COPPER SHAVING IS ALLOWED IN FRONT OF PADS OF CONNECTORS J5 AND J7
IN ORDER TO KEEP A 0.010" CLEARANCE FROM THE EDGE OF THE BOARDS.

DRILL CHART: TOP to BOTTOM
ALL UNITS ARE IN MILS

FIGURE	SIZE	TOLERANCE	PLATED	QTY
Ø	10.0	+0.0/-10.0	PLATED	455
⊘	18.0	+2.0/-2.0	PLATED	3
⊙	28.0	+2.0/-2.0	PLATED	20
⓪	40.0	+3.0/-3.0	PLATED	16
Ⓔ	41.0	+3.0/-3.0	PLATED	32
Ⓕ	47.0	+3.0/-3.0	PLATED	32
△	73.0	+3.0/-3.0	PLATED	2
⬢	35.0	+2.0/-2.0	NON-PLATED	4
□	125.0	+3.0/-3.0	NON-PLATED	4

DETAIL A
LAYER STACKUP
SCALE: NONE

FINISHED Cu WEIGHT

LAYER	THICKNESS	WEIGHT
LAYER 1 COMPONENT SIDE	1 oz.	1 oz.
LAYER 2 SOLDER SIDE	1 oz.	1 oz.

The drawing also includes a top view of the board showing dimensions (e.g., 3.20, 2.20, 1.10, 2.10) and a cross-section view labeled "PRIMARY DATUM GRID ORIGIN".