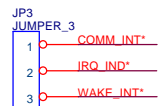
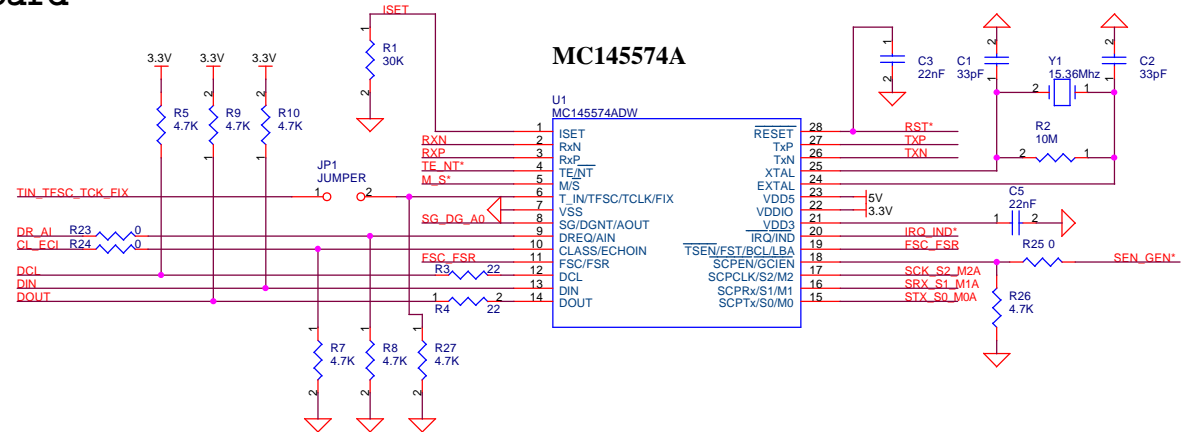
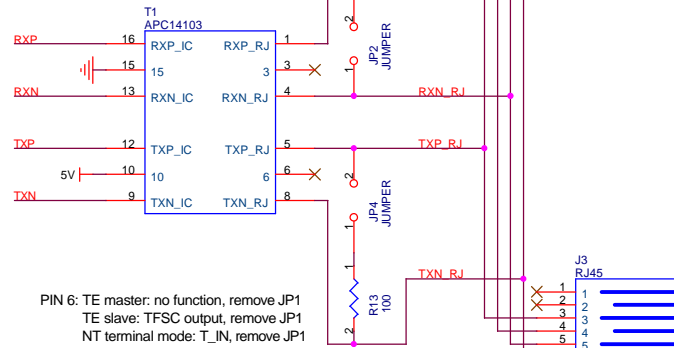


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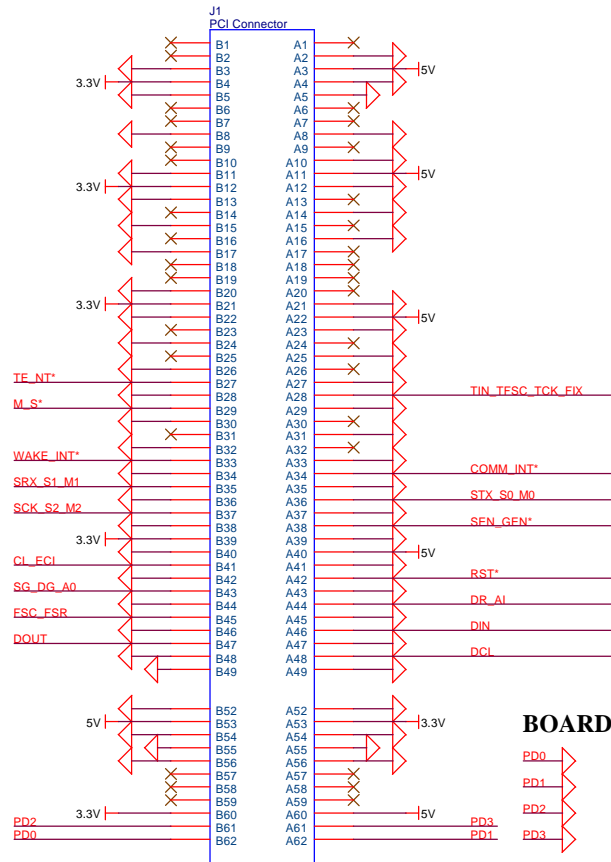
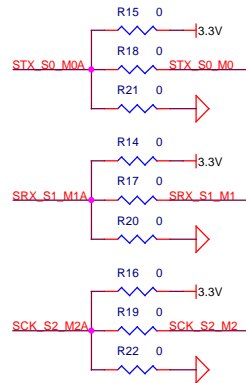
## S0 INTERFACE



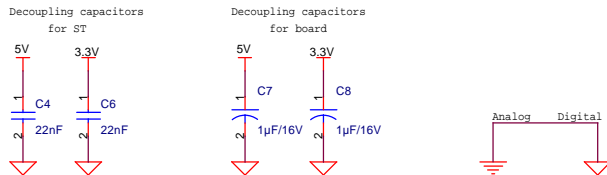
PIN 6: TE master: no function, remove JP1  
TE slave: TFSC output, remove JP1  
NT terminal mode: T\_IN, remove JP1  
other NT modes: FIX input, set JP1

PIN 10: TE master: CLASS input  
other modes: no  
function, tied to VSS  
PIN 9: TE master, NT terminal mode: DREQUEST input  
other modes: no function, tied to VSS

## S0, S1, S2 CONFIG



**BOARD\_ID = 0**



Rev 1.00 : Initial Version			
MOTOROLA Semiconductors		Av. Eisenhower B.P. 1029	
NCSG / CTASD / ISDN		31023 TOULOUSE Cedex	
Title HSEVB - MC145574A Daughter Board			
Designed by : E. Cheyron			Rev 1.00
Size B	Document Number		
Date:	Thursday, August 17, 2000	Sheet	1 of 1