SECTION 1
M5407TEKC3 DAUGHTERBOARD SPECIFICATION

Revision 1.d, 09/08/00: Edited by John Kelley
Revision 1.c, 09/01/00: Edited by John Kelley
Revision 1.b, 08/21/00: Edited by John Kelley
Revision 1.a, 08/15/00: Created by John Kelley

1.1 OVERVIEW

This M5407TEKC3 Daughterboard specification document describes the Tektronix Logic Analyzer connector daughterboard being developed for use with the M5407C3 Evaluation board's two expansion connectors. This includes available component information and specification.

The intent of this document is to outline the requirements of the M5407TEKC3 Daughterboard. Suggestions are encouraged and should be sent to the author (j.kelley@Motorola.com).

1.2 BRIEF SUMMARY

Below is a brief summary of the M5407TEKC3 Daughterboard board specification. More detailed information can be found in following sections.

M5407TEKC3 Daughterboard Configuration:

- Two, 120 pin Surface-Mount Connectors that mate with the M5407C3 expansion connectors
- Five, 38 pin Mictor Connectors that allow connectivity to the Tektronix Logic Analyzer
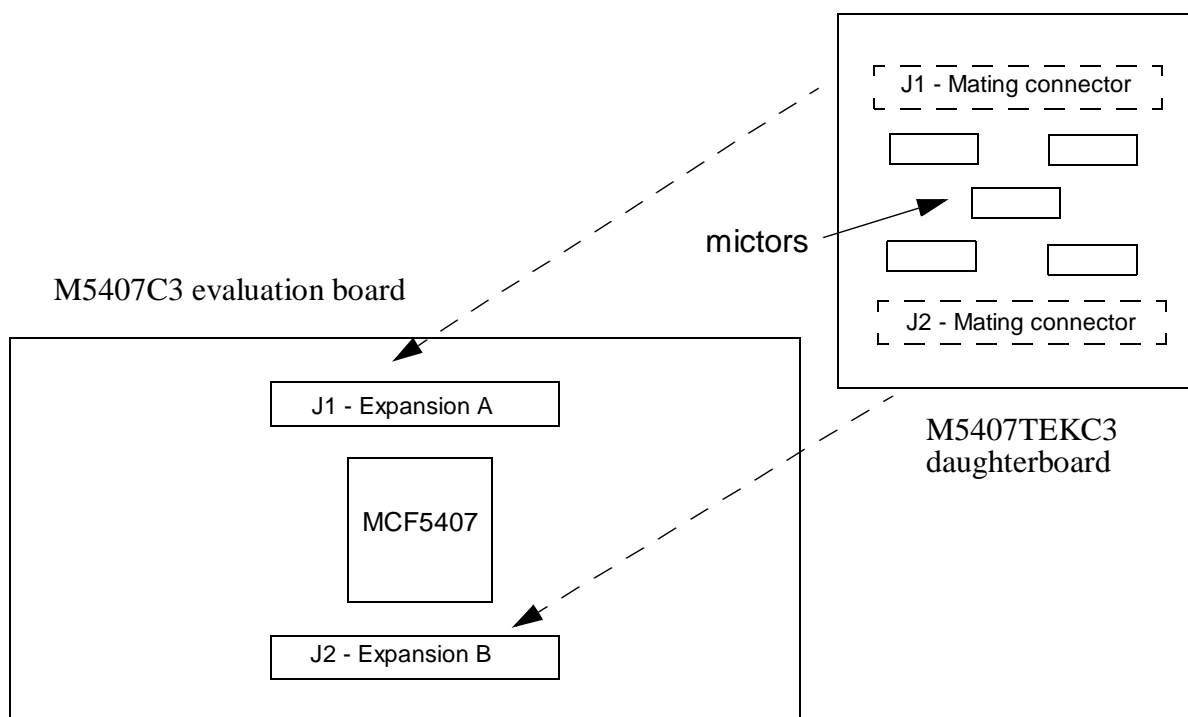

Figure 1. Block diagram view of M5407C3 and daughterboard M5407TEKC3.

Motorola General Business Use

Figure 1 shows a conceptual view of how the M5407TEKC3 daughterboard will be laid out and how it will connect with the M5407C3 board. The M5407C3 board has two 120 pin expansion connectors located on either side of the MCF5407 Processor as shown. The M5407TEKC3 will have two mating 120 pin connectors on its bottom side. Through these connectors, the M5407TEKC3 daughterboard will connect with the M5407C3 board signals and route them to the five mictors on the top side. These mictor connectors will allow the user to easily access the signals from the M5407C3 board with a logic analyzer.

1.3 HARDWARE/PHYSICAL SPECIFICATION

1. All major components should be thoroughly labeled on silkscreen.

    — A "dot" next to every 5th pin on a package (except mictors)
    — Pin 1(one) of every device will be labeled
    — All labels will be aligned to 0° or -90° for easy reading

2. The board name, "Motorola ColdFire M5407TEKC3", will also be easily visible on the board.

3. Special care should be made to allow all cables, while debugging the board, to be plugged in at the same time without interfering with nearby cables.

1.3.1 Headers/Connectors

In general, the headers/connectors on the M5407TEKC3 Daughter Board should be unique to minimize the potential of the user connecting to an incorrect expansion connection. Where possible, the connectors should be keyed and labeled. Signal loading and transmission effects must be taken in consideration.

1.3.1.1 MICTOR CONNECTORS

Five, 38-pin connectors (Matched Impedance Connectors AMP767054-1) will allow easy access to the 5407 board signals by the logic analyzer. It is recommended that the signal placement on the connectors match those on the 5307 board as much as possible to minimize changes to the Logic Analyzer system files. Those pinouts may be found in the 5307 evaluation board documentation located at "www.motorola.com/coldfire/".

1.3.1.2 EXPANSION CONNECTORS

Two, 120-pin expansion connectors (120-way SMT Receptacle expansion connector, AMP179031-5) will provide access to all pins of the microprocessor by connecting with the 5407 board's mating 120-pin expansion connectors (AMP 177983-5). The signals are determined by the existing mating connector on the 5407 board.

(IMPORTANT: Do not ground or otherwise use those pins listed as empty in the below tables because the pin may be connected to a signal or power from the 5407 board)

Table 1-1. Expansion Port A Pin Assignment

PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME
1	IVCC	2	IVCC	61	D20	62	A15
3	IVCC	4	GND	63	D21	64	A16
5	D0	6	$\overline{\text{HIZ}}$	65	D22	66	GND
7	D1	8	$\overline{\text{BKPT\_TMS}}$	67	GND	68	A17
9	GND	10	DSDI_TDI	69	D23	70	A18
11	D2	12	IVCC	71	D24	72	A19
13	D3	14	DSD0_TD0	73	D25	74	+3.3
15	+3.3	16	TCK	75	+3.3	76	A20
17	D4	18	DSCLK_TRST	77	D26	78	A21
19	D5	20	GND	79	D27	80	A22
21	GND	22	A0	81	D28	82	GND
23	D6	24	A1	83	GND	84	A23
25	D7	26	+3.3	85	D29	86	A24
27	+3.3	28	A2	87	D30	88	A25
29	D8	30	A3	89	D31	90	+3.3
31	D9	32	A4	91	+3.3	92	A26
33	D10	34	GND	93	SIZ0	94	A27
35	GND	36	A5	95	SIZ1	96	A28
37	D11	38	A6	97	GND	98	GND
39	D12	40	A7	99	$\overline{\text{OE}}$	100	A29
41	D13	42	+3.3	101	$\overline{\text{CS0}}$	102	A30
43	+3.3	44	A8	103	$\overline{\text{CS1}}$	104	A31
45	D14	46	A9	105	+3.3	106	IVCC
47	D15	48	A10	107	GND	108	GND
49	D16	50	GND	109	GND	110	GND
51	GND	52	A11	111	IVCC	112	IVCC
53	D17	54	A12	113		114	
55	D18	56	A13	115		116	
57	D19	58	+3.3	117	GND	118	GND
59	+3.3	60	A14	119	GND	120	GND

Table 1-2. Expansion Port B Pin Assignment

PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME
1	IVCC	2	IVCC	61	TIN1	62	GND
3	GND	4	GND	63	-R_RAS0/SO0	64	GND
5	$\overline{CS2}$	6	PP0	65	-R_RAS1/SO2	66	MTMOD1
7	$\overline{CS3}$	8	PP1	67	GND	68	MTMOD0
9	$\overline{CS4}$	10	+3.3	69	-R_CAS0/$\overline{DQM0}$	70	IVCC
11	IVCC	12	PP2	71	-R_CAS1/$\overline{DQM1}$	72	CLKIN
13	$\overline{CS5}$	14	PP3	73	-R_CAS2/$\overline{DQM2}$	74	GND
15	$\overline{CS6}$	16	PP4	75	+3.3	76	$\overline{RSTO}$
17	$\overline{CS7}$	18	GND	77	-R_CAS3/$\overline{DQM3}$	78	IVCC
19	GND	20	PP5	79	$\overline{R\_DRAMW}$	80	BCLKO
21	$\overline{AS}$	22	PP6	81	$\overline{R\_SRAS}$	82	GND
23	R/$\overline{W}$	24	PP7	83	GND	84	EDGESEL
25	$\overline{TA}$	26	IVCC	85	$\overline{R\_SCAS}$	86	+3.3
27	+3.3	28	PSTDDATA7	87	R_SCKE	88	TXD0
29	$\overline{TS}$	30	PSTDDATA6	89	$\overline{BWE0}$	90	RXD0
31	$\overline{CF\_RSTI}$	32	GND	91	+3.3	92	$\overline{RTS0}$
33	$\overline{IRQ7}$	34	PSTDDATA5	93	$\overline{BWE1}$	94	$\overline{CTS0}$
35	GND	36	PSTDDATA4	95	$\overline{BWE2}$	96	GND
37	$\overline{IRQ5}$	38	+3.3	97	$\overline{BWE3}$	98	TXD1
39	$\overline{IRQ3}$	40	PSTDDATA3	99	GND	100	RXD1
41	$\overline{IRQ1}$	42	PSTDDATA2	101	SCL	102	$\overline{RTS1}$
43	IVCC	44	GND	103	SDA	104	$\overline{CTS1}$
45	$\overline{BR}$	46	PSTDDATA1	105	GND	106	IVCC
47	$\overline{BD}$	48	PSTDDATA0	107	IVCC	108	IVCC
49	$\overline{BG}$	50	IVCC	109	+3.3	110	+3.3
51	GND	52	PSTCLK	111		112	$\overline{CS\_FPCIBD}$
53	TOUT1	54	GND	113		114	
55	TOUT0	56	MTMOD3	115		116	
57	TIN0	58	MTMOD2	117	GND	118	GND
59	+3.3	60	IVCC	119	GND	120	GND

1.3.2 Test Points

Test points should be installed for GND, +3.3, and IVCC.

1.3.3 Signal Noise Interference

Signal noise should be minimized to meet requirement for this application, by implementing best layout design methodologies.

1.4 SPECIFICATION FEEDBACK

Once again, we are looking for suggestions and improvements to this board. Please send feedback to John Kelley at j.kelley@Motorola.com.