T1024RDB

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Version Control

Version	Date	Modifications
V0.1	2014/08	First release of Schematics
V1.0	2014/08	Released to Manufacturing
V2.0	2014/09	1. Change AQ2104 to AQR105, add another AQR105 for 2.5G SGMII 2. Add serdes mux for PCIe and 2.5G SGMII 3. Add VCORE power measurement
V3.0	2014/11	1. Add 2 clock mux for SD1/2_REFCLK selection 2. Change T1040 debug version resistors "V40" to "DNP"

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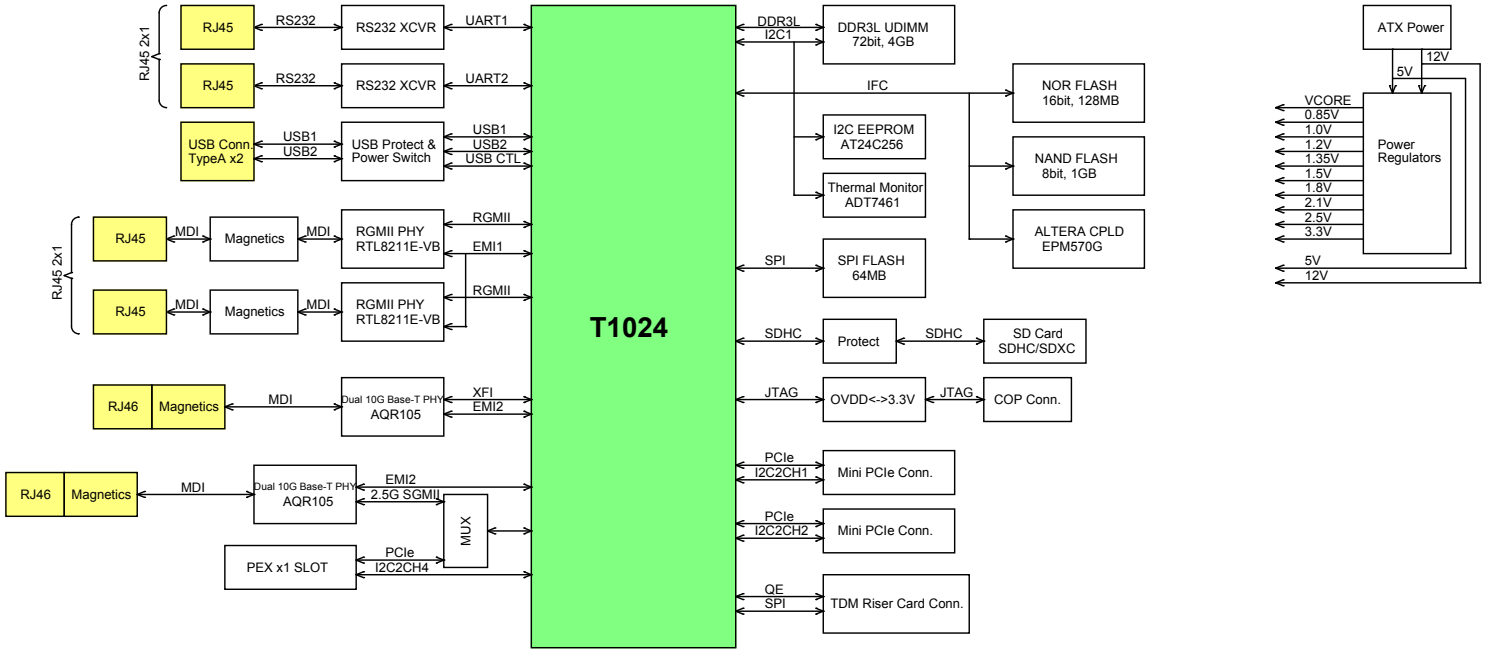
SYSTEM BLOCK DIAGRAM



Title: T1024RDB			
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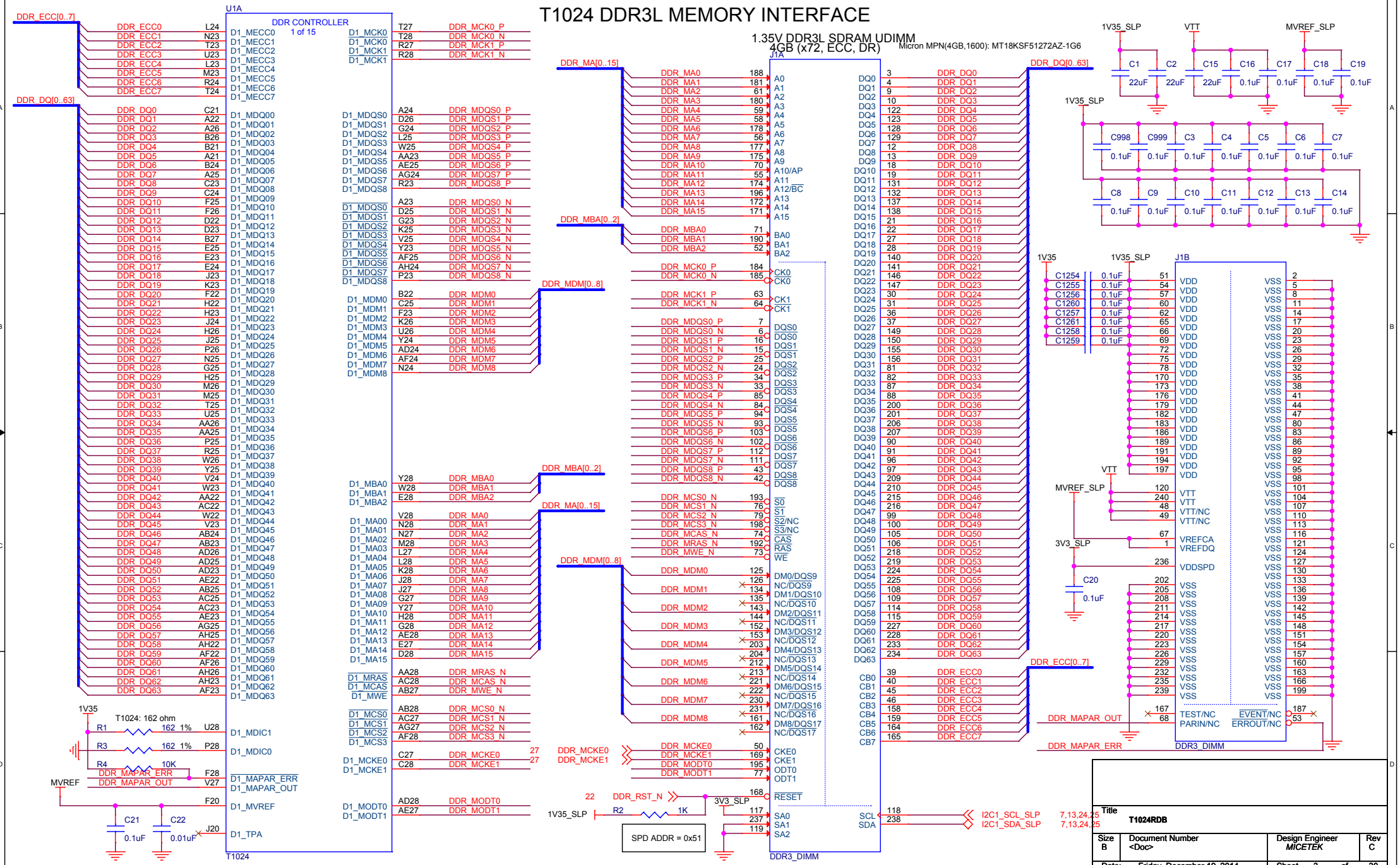
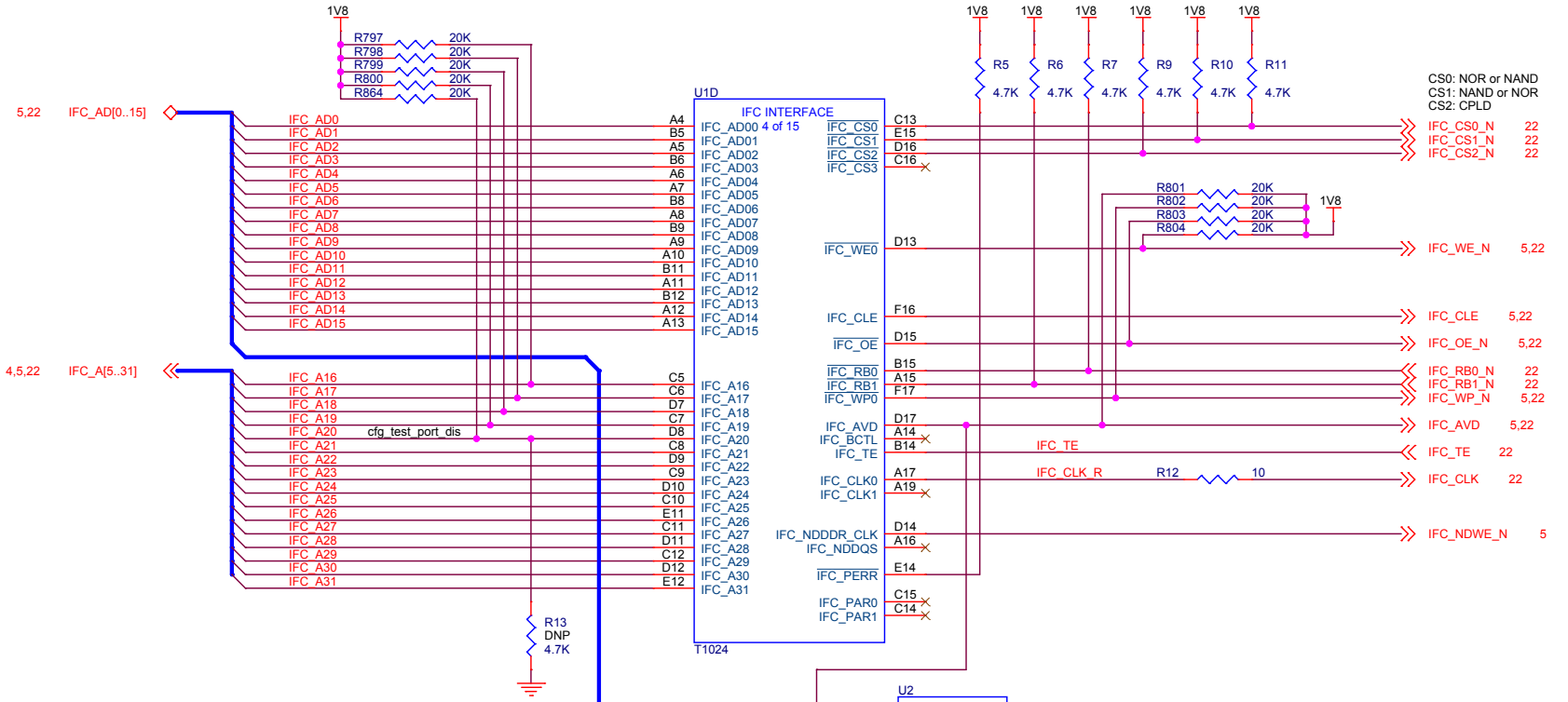
T1024 DDR3L MEMORY INTERFACE

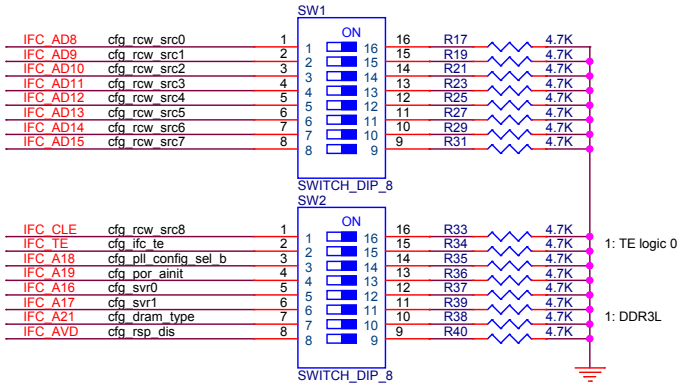


T1024 IFC INTERFACE



T1024 RESET CONFIGURATION

cfg_rcw_src[0:8]
0_0010_0111: NOR FLASH BOOT
0_0100_0000: SD CARD BOOT
0_0100_0101: SPI BOOT
1_0001_1001: NAND FLASH BOOT



Title: T1024RDB			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: A
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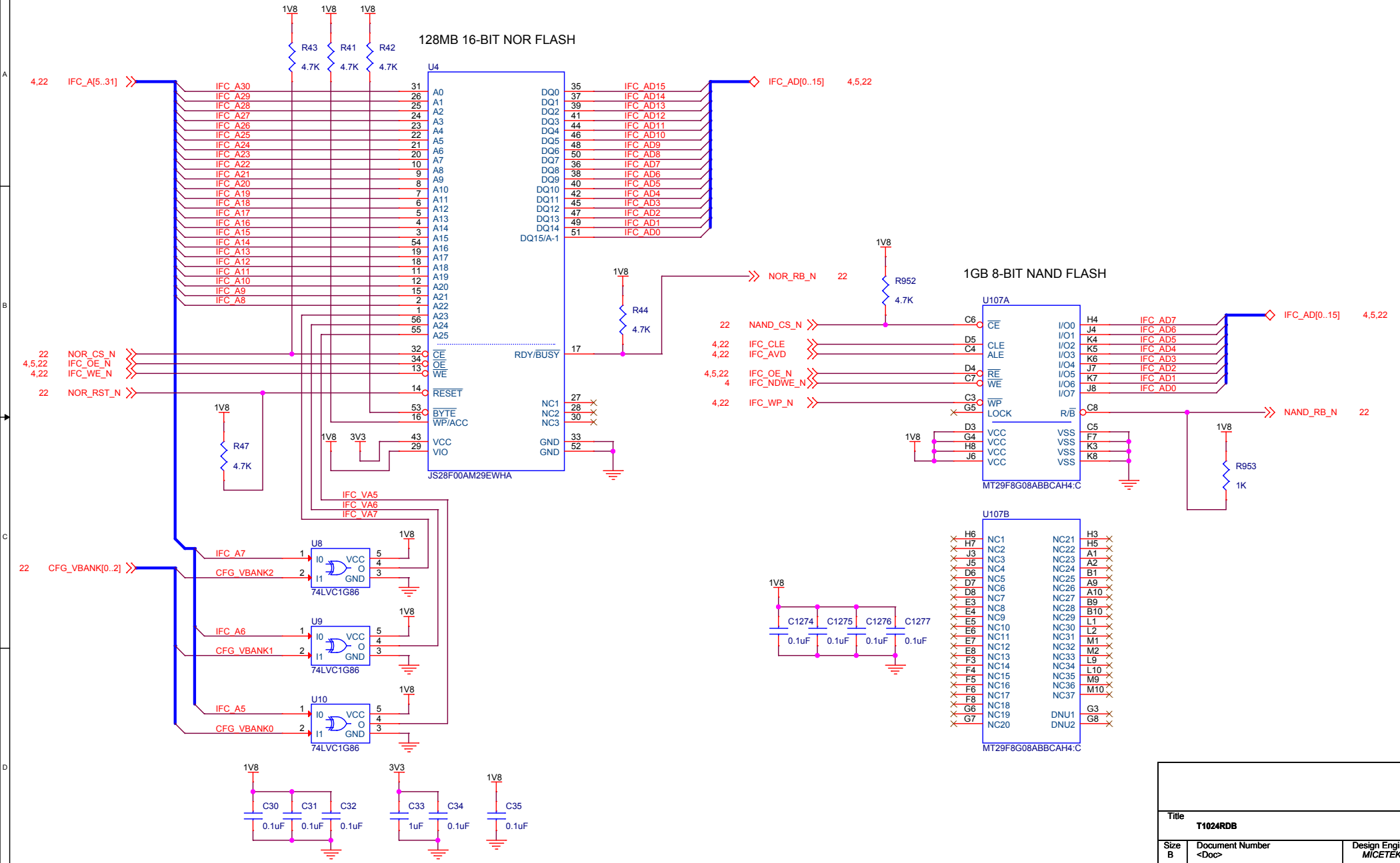
T1024 NOR and NAND FLASH INTERFACE



Title: T1024RDB			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: C
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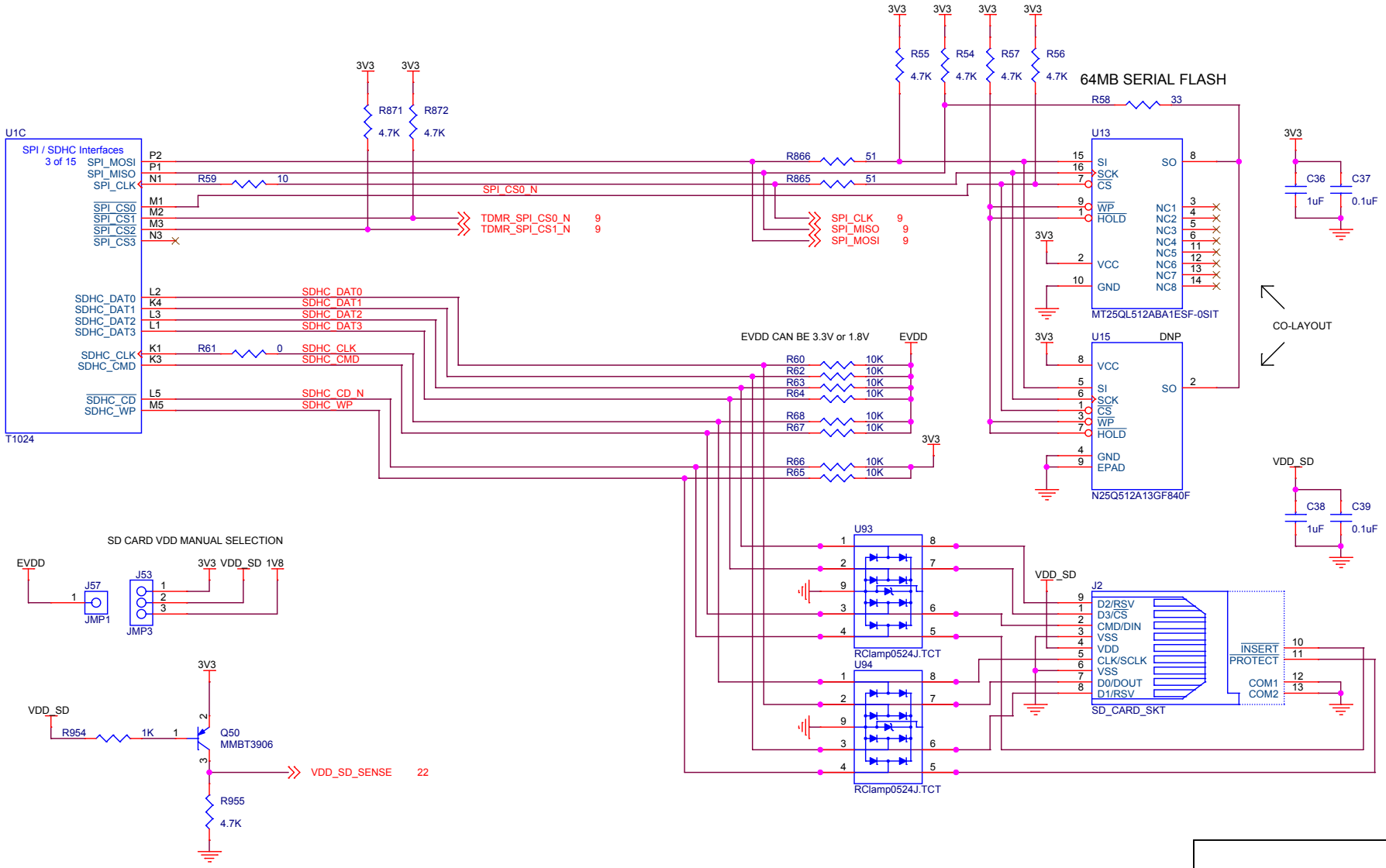
T1024 SPI FLASH and SDHC INTERFACE



Title: T1024RDB			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: C
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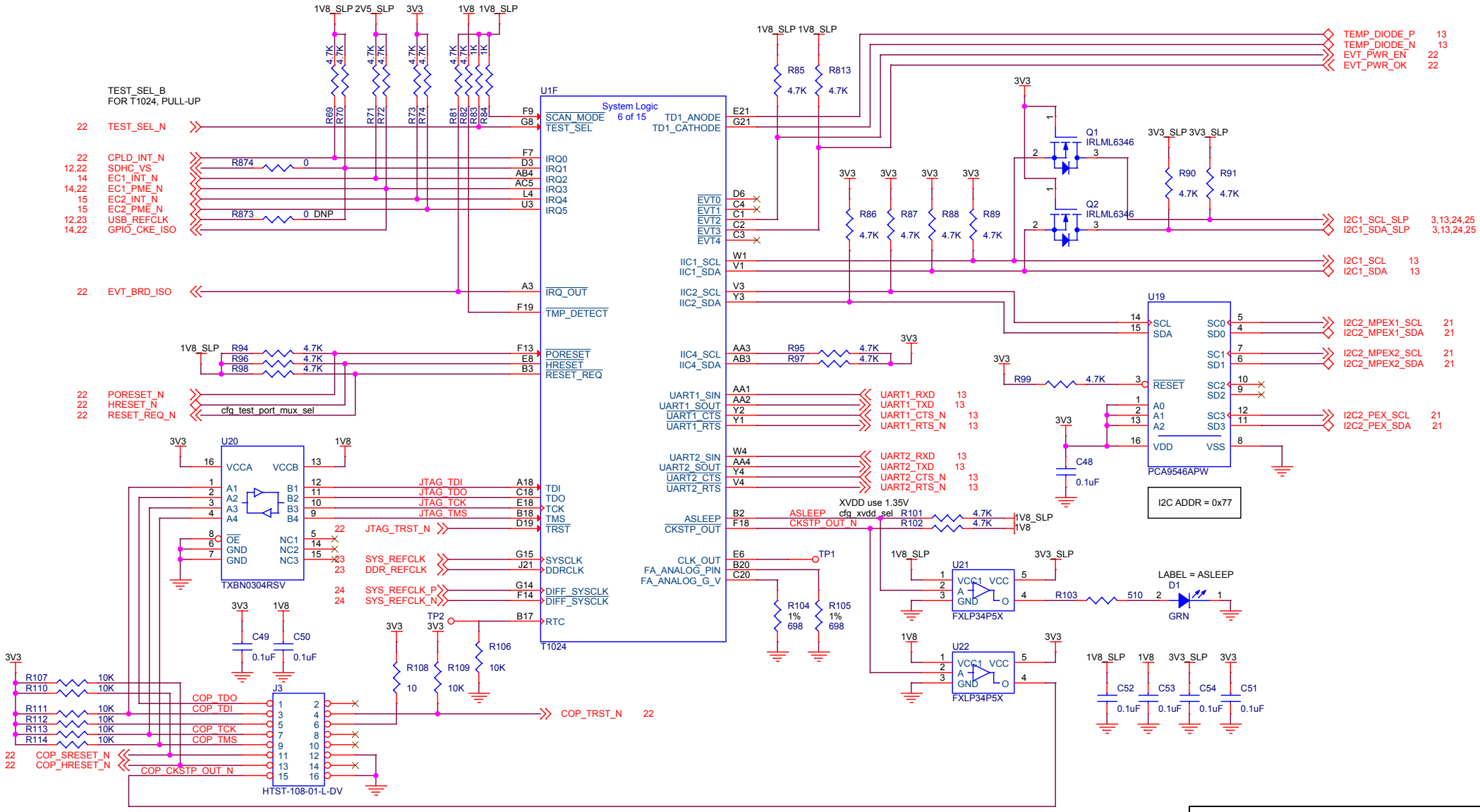
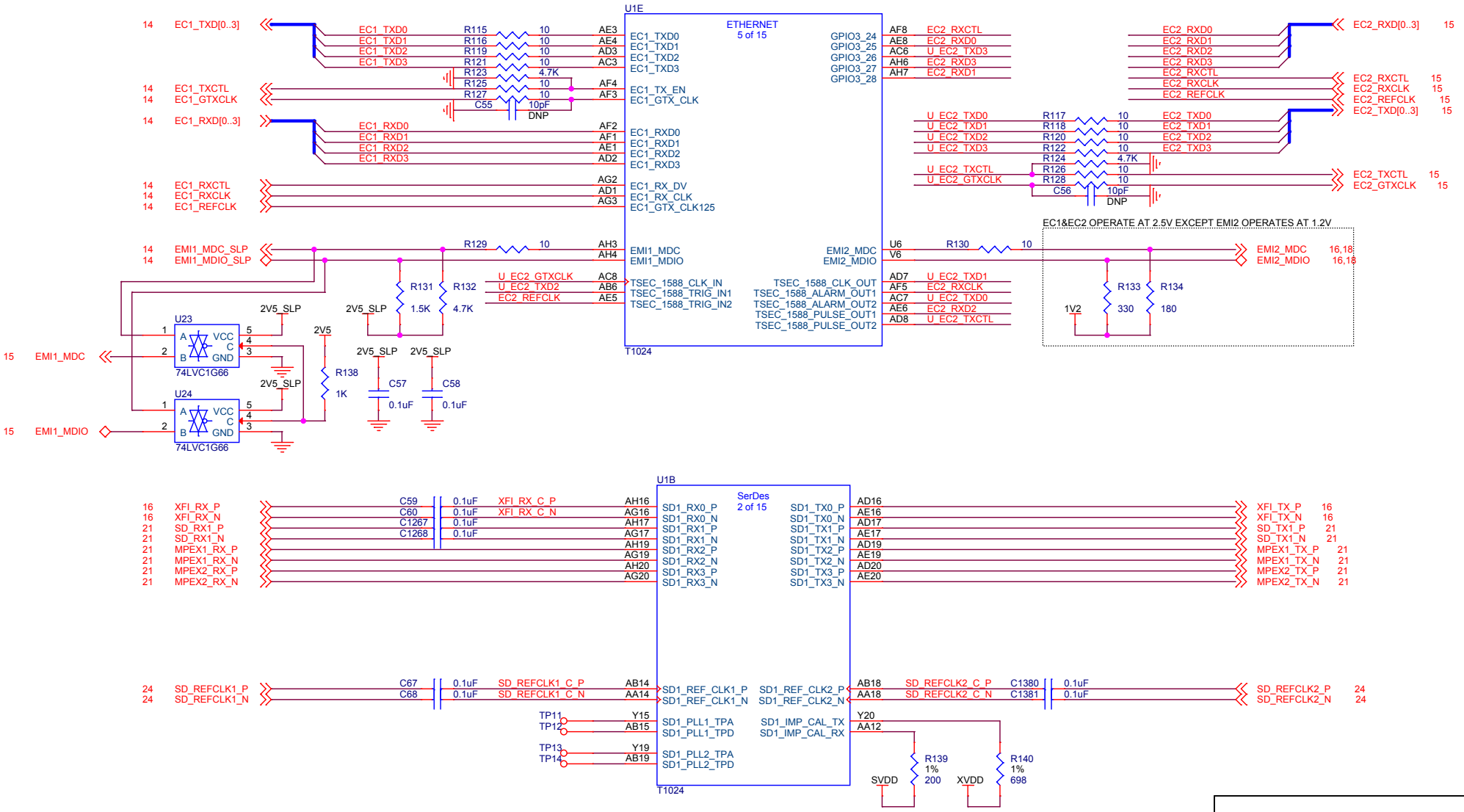
T1024 SYSTEM LOGIC INTERFACE



T1024 ETHERNET and SERDES INTERFACE



Title: T1024RDB			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: C
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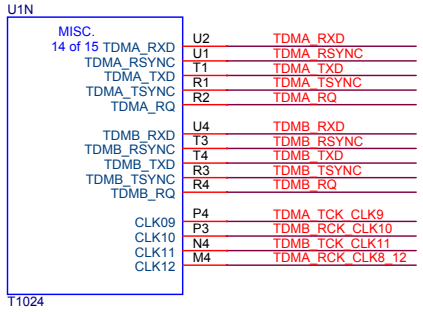
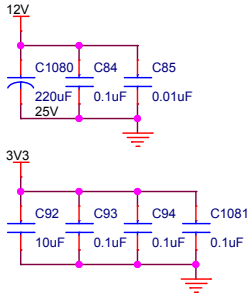
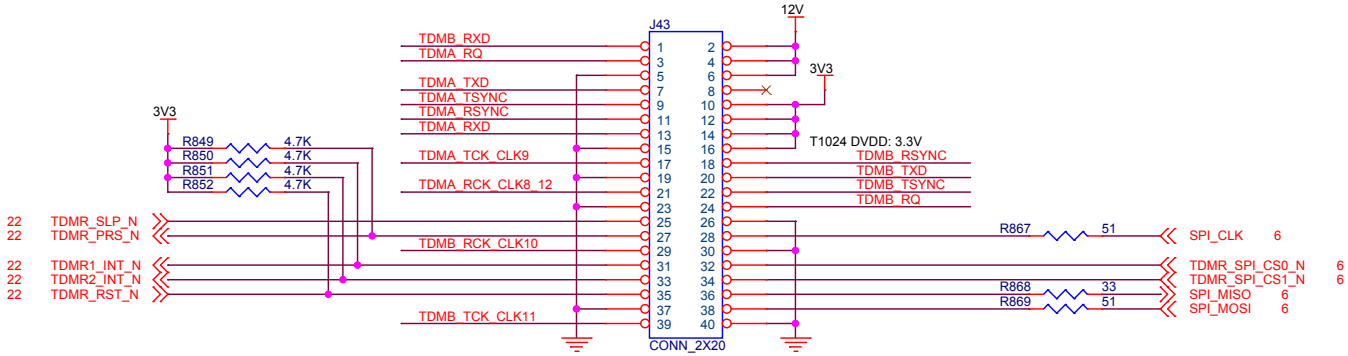
T1024 QE INTERFACE





TDM RISER CARD CONNECTOR



Title: T1024RDB			
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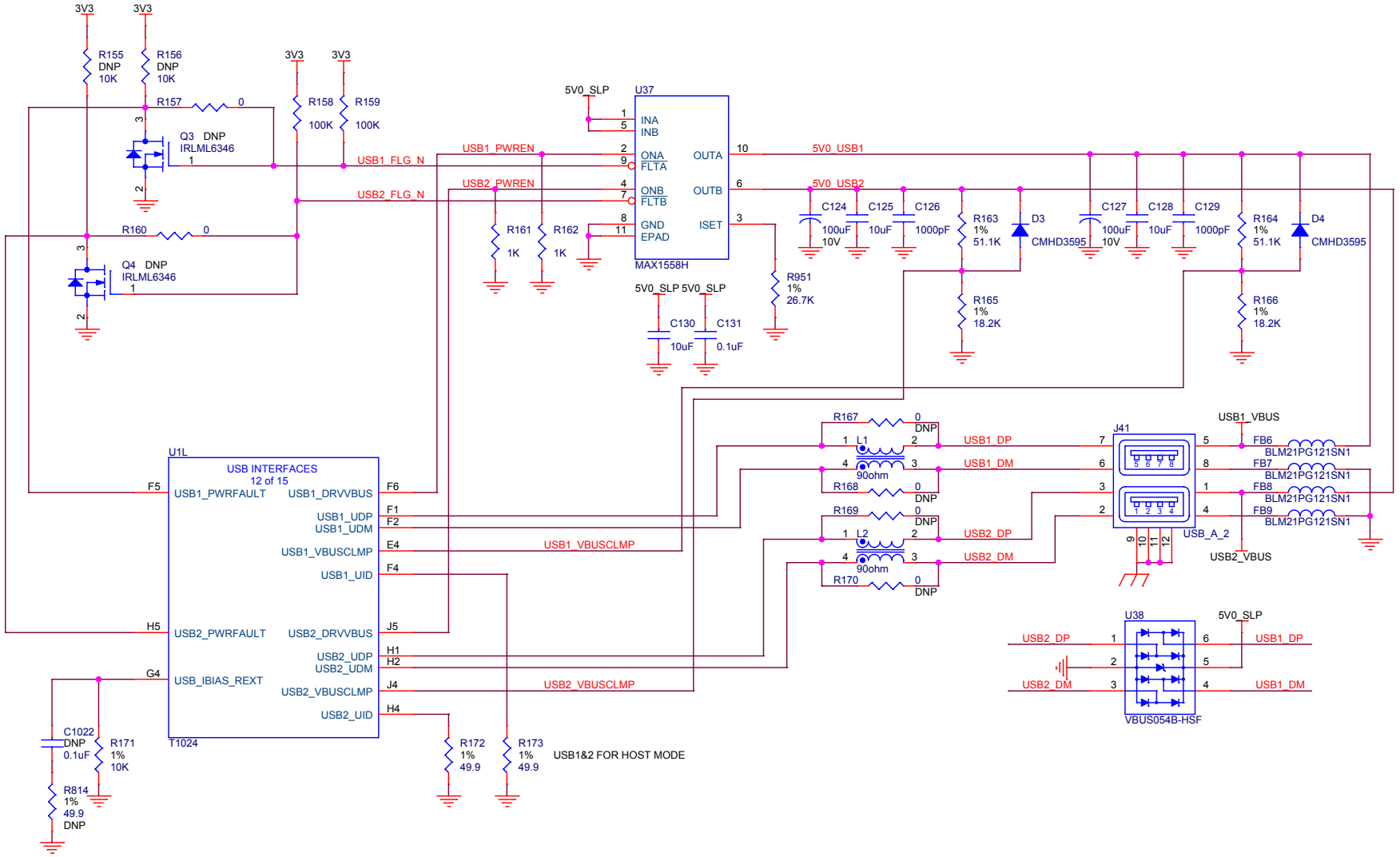
T1024 USB INTERFACE



Title: T1024RDB			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: C
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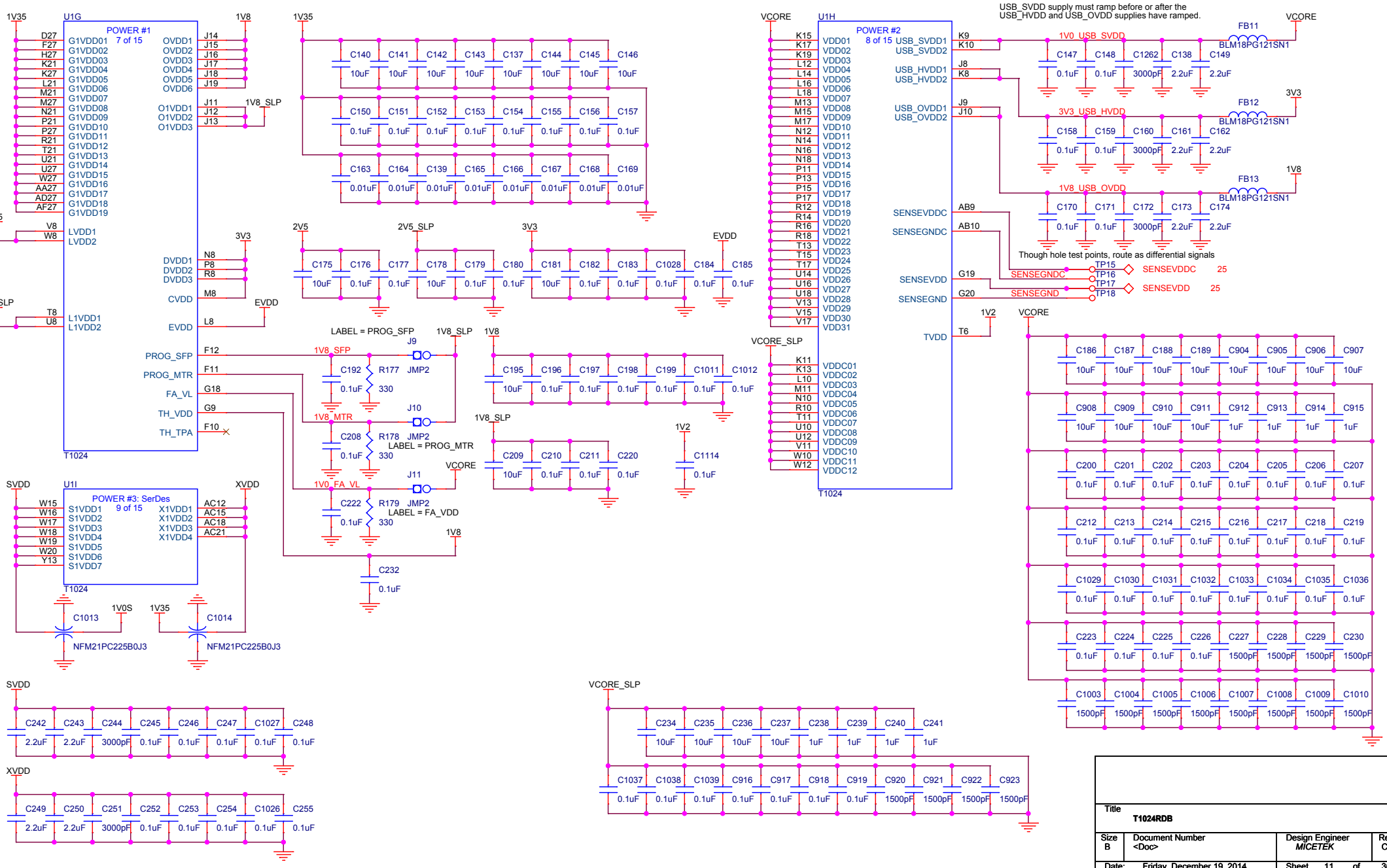
T1024 POWER SUPPLY



Title: T1024RDB			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: C
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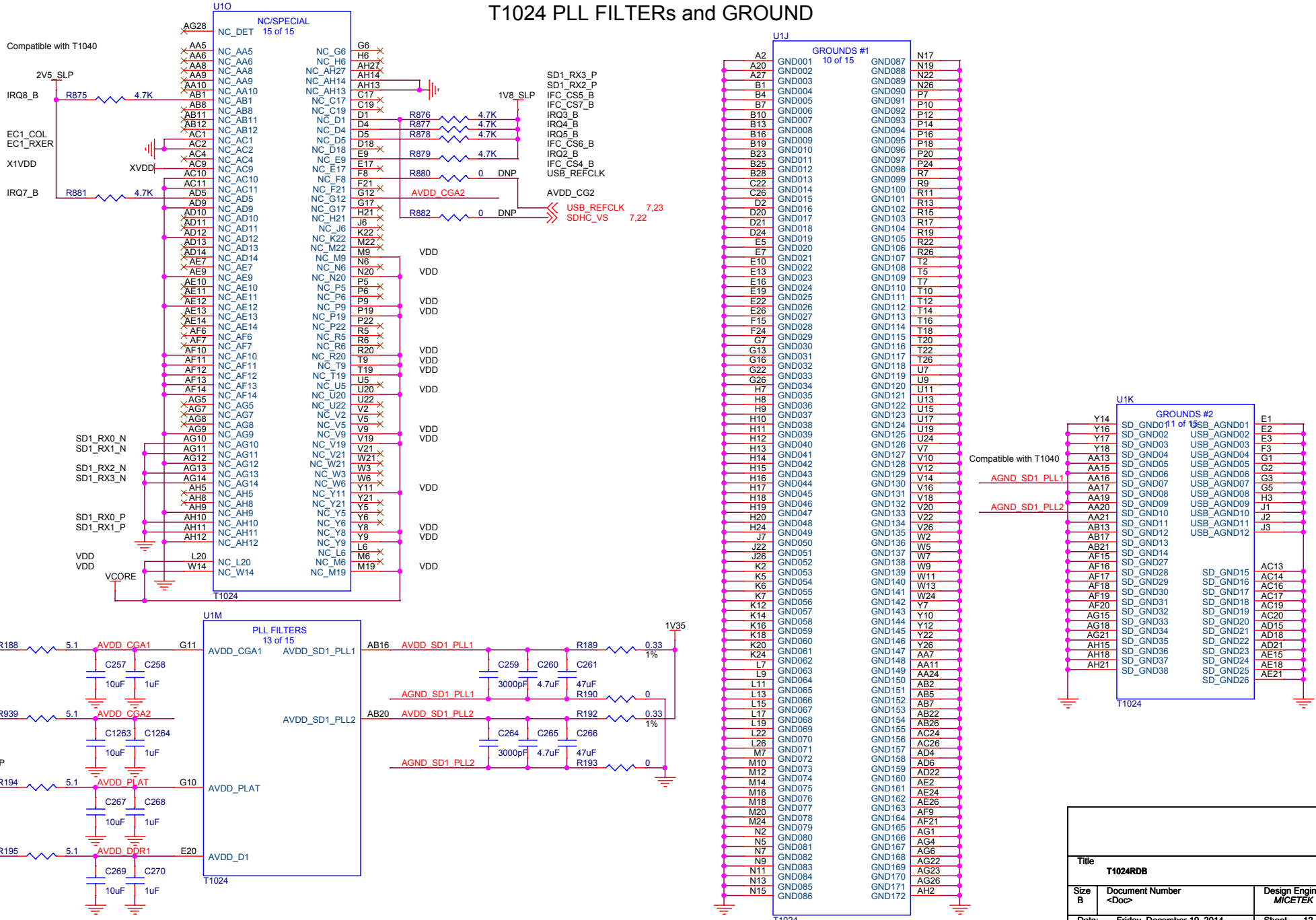
T1024 PLL FILTERs and GROUND



Title: T1024RDB			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: C
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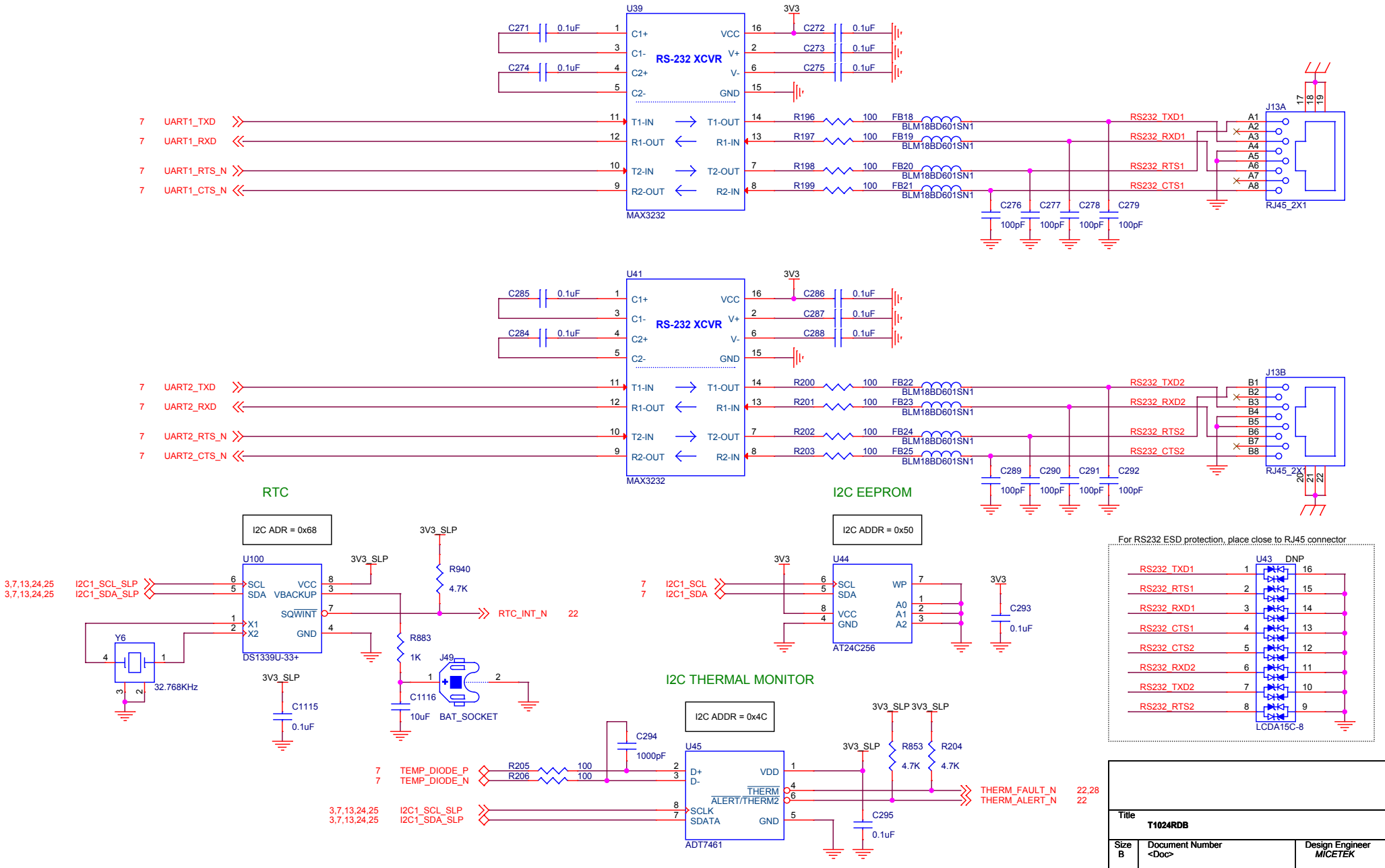
T1024 DUART and I2C DEVICE INTERFACE



Title: T1024RDB			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: C
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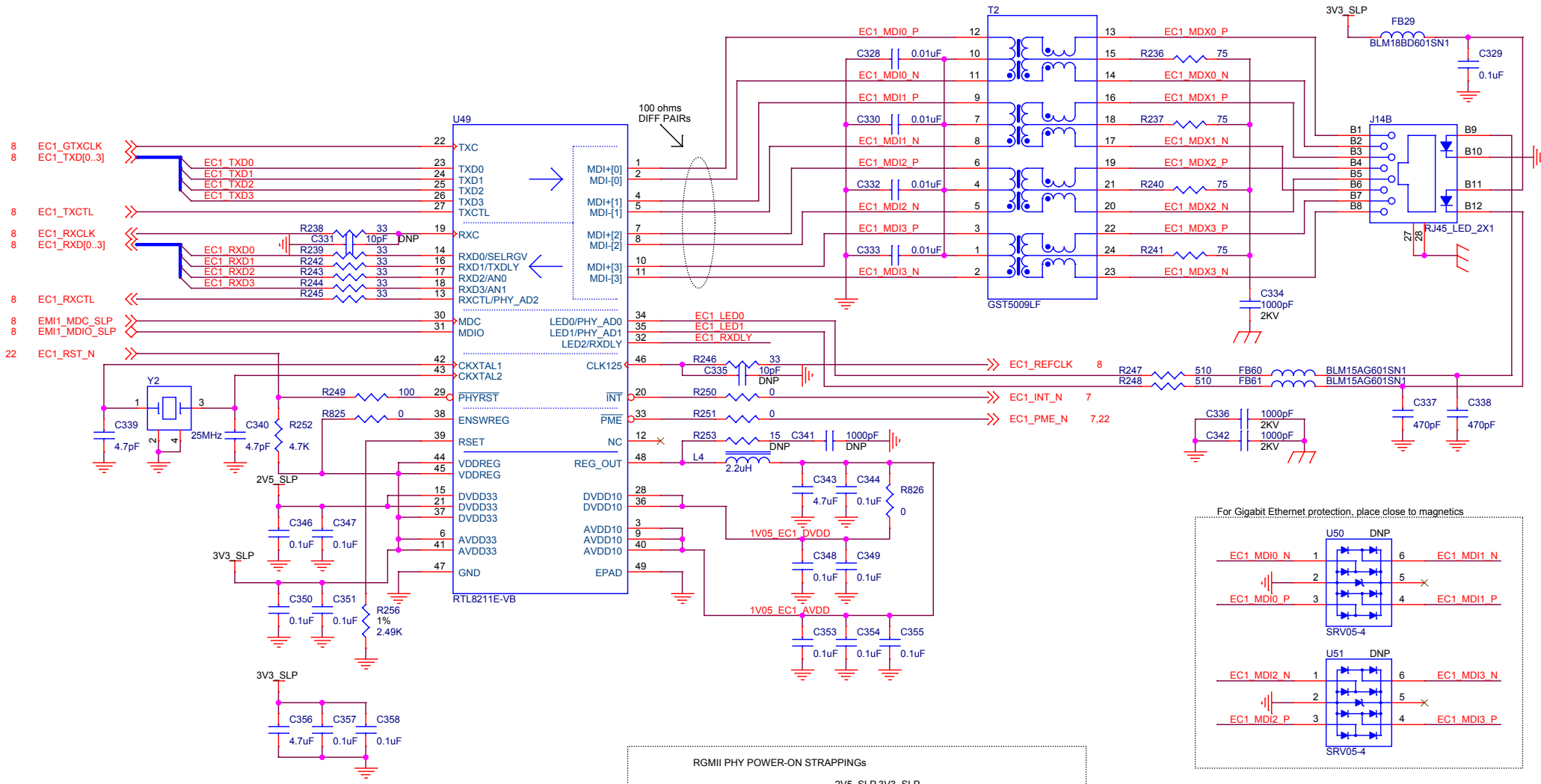
RGMII ETHERNET PORT 1



Title: T1024RDB			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: C
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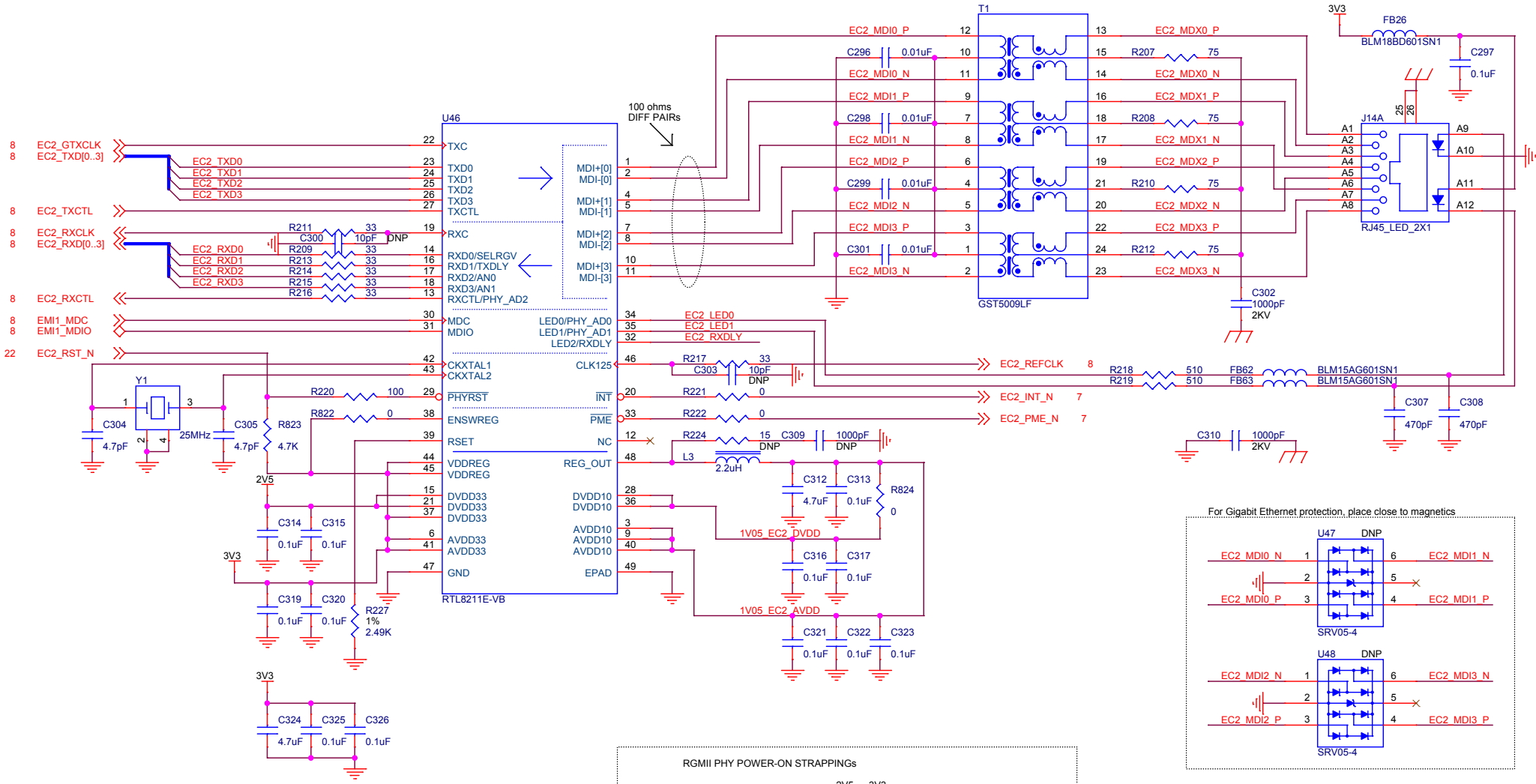
RGMII ETHERNET PORT 2



Title: T1024RDB			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: C
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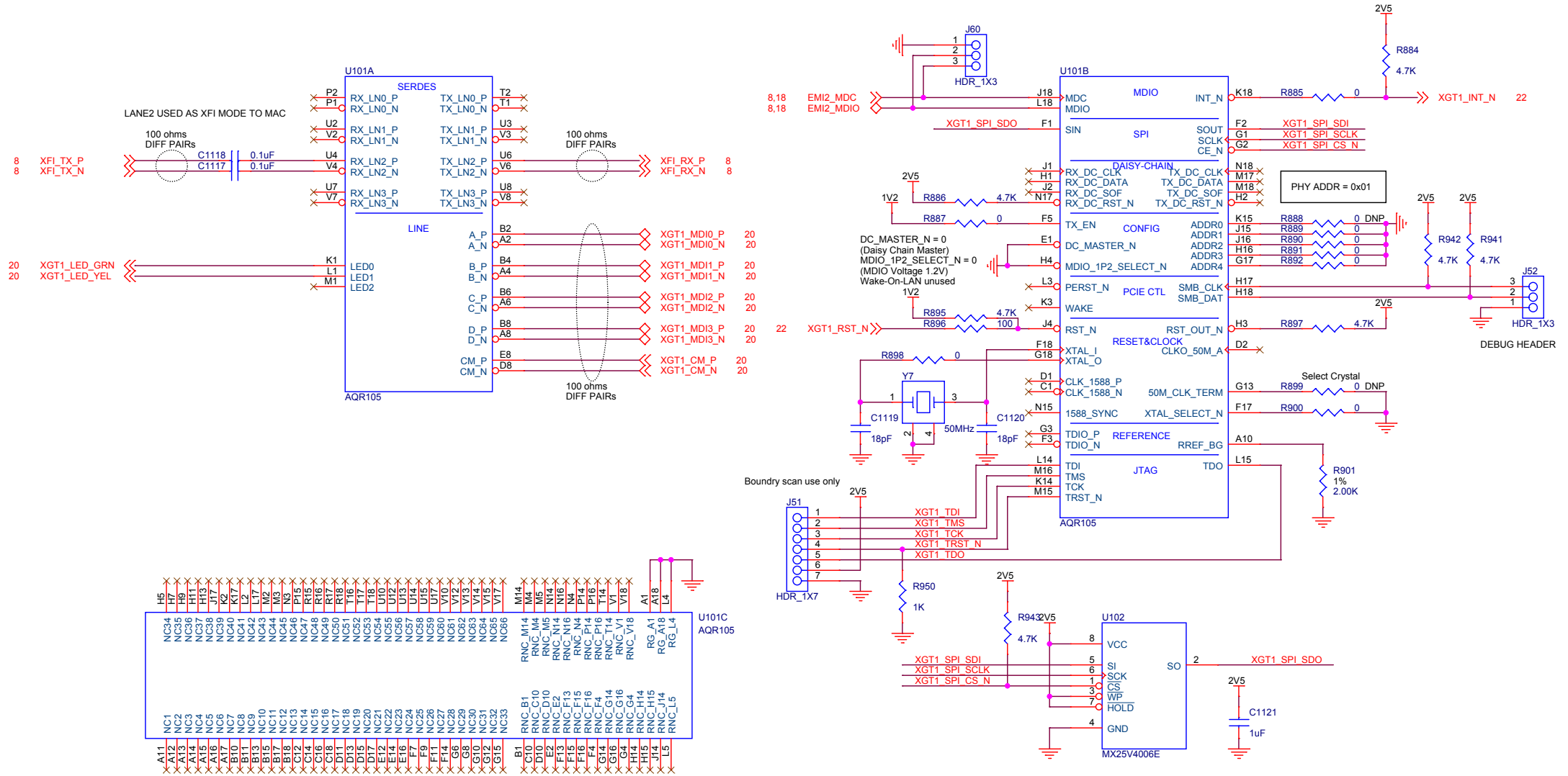
10G BASE-T PHY 1 AQR105



Title: T1024RDB			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: C
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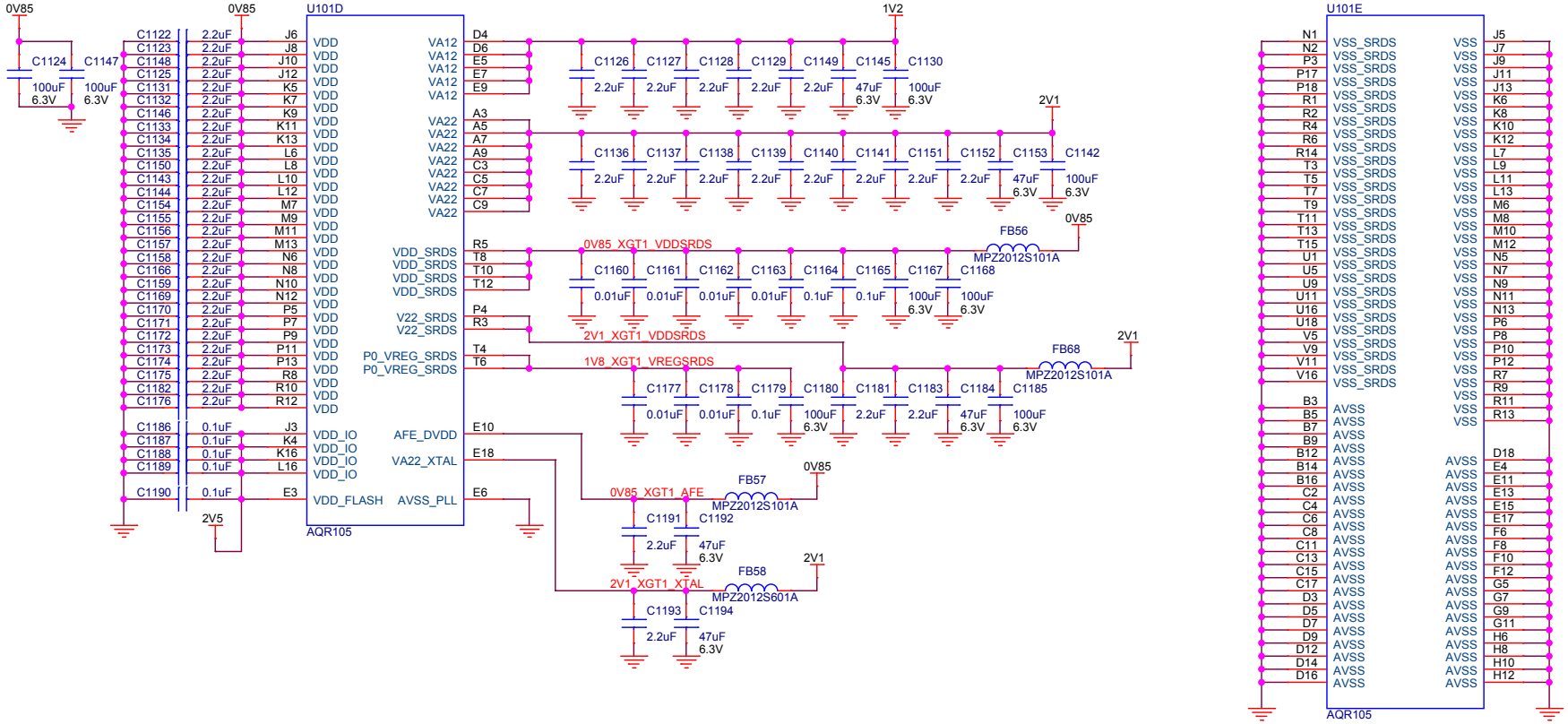
10G BASE-T PHY 1 AQR105 POWER SUPPLY



Title: T1024RDB			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: C
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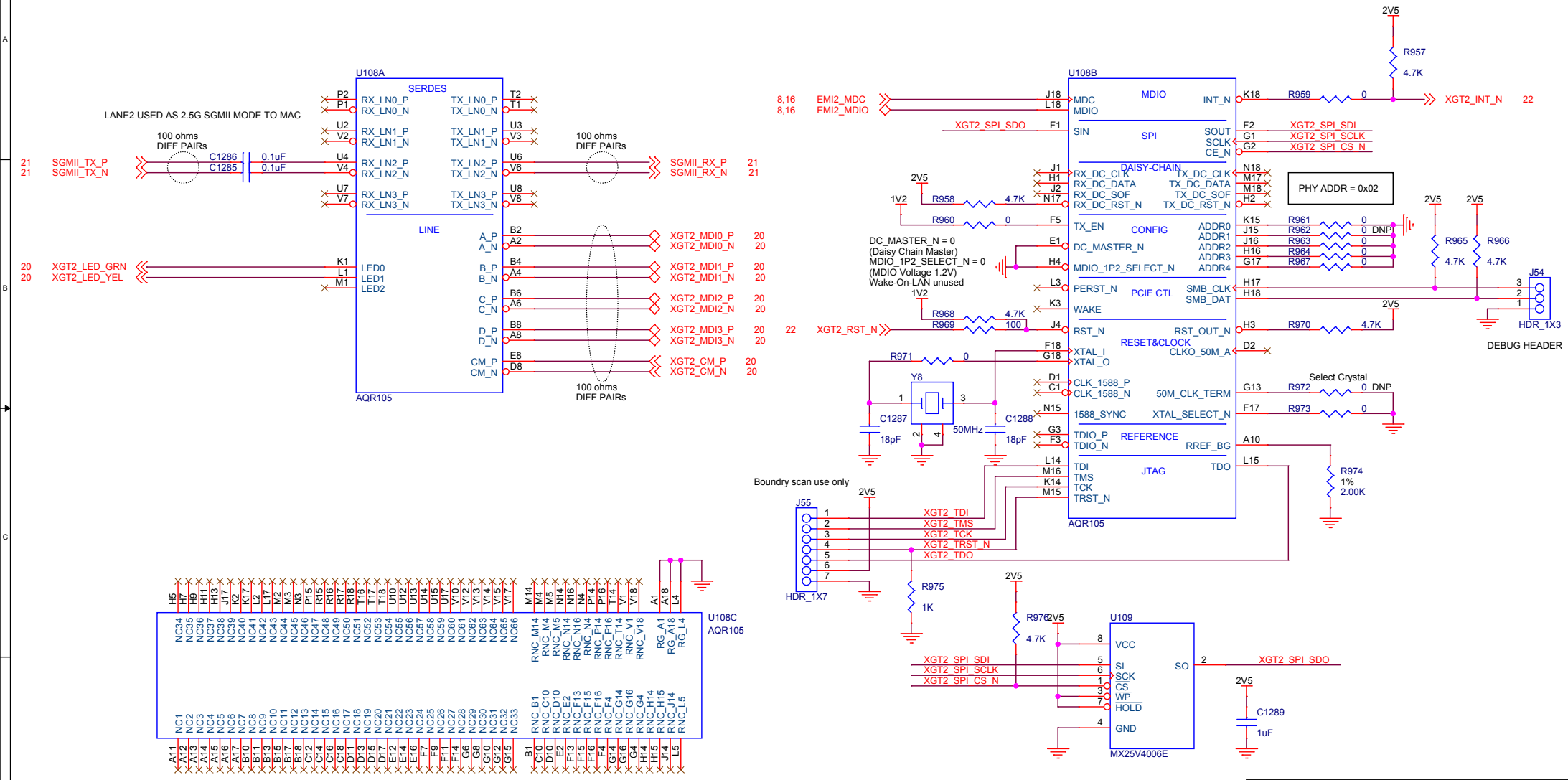
2.5G BASE-T PHY 2 AQR105



Title: T1024RDB			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: C
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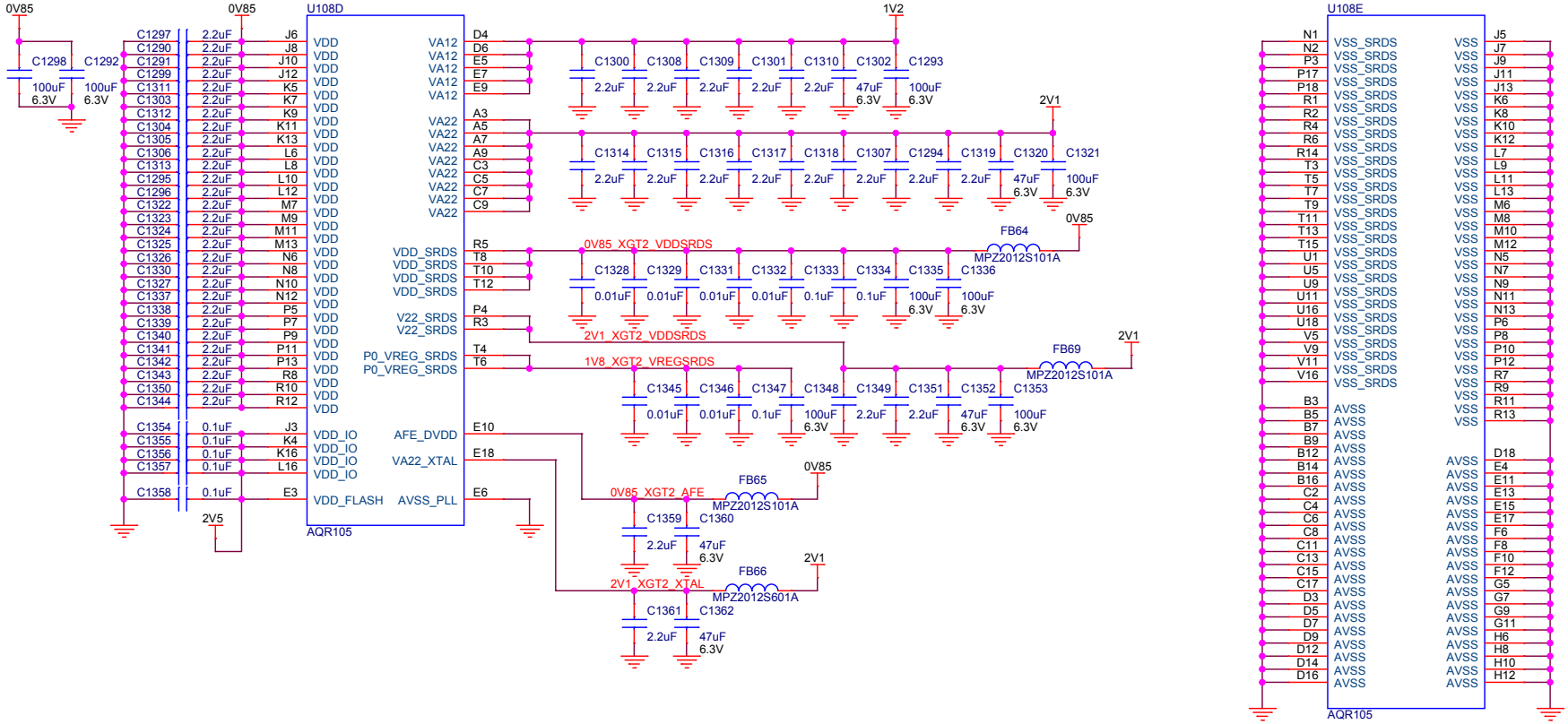
2.5G BASE-T PHY 2 AQR105 POWER SUPPLY



Title: T1024RDB			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: C
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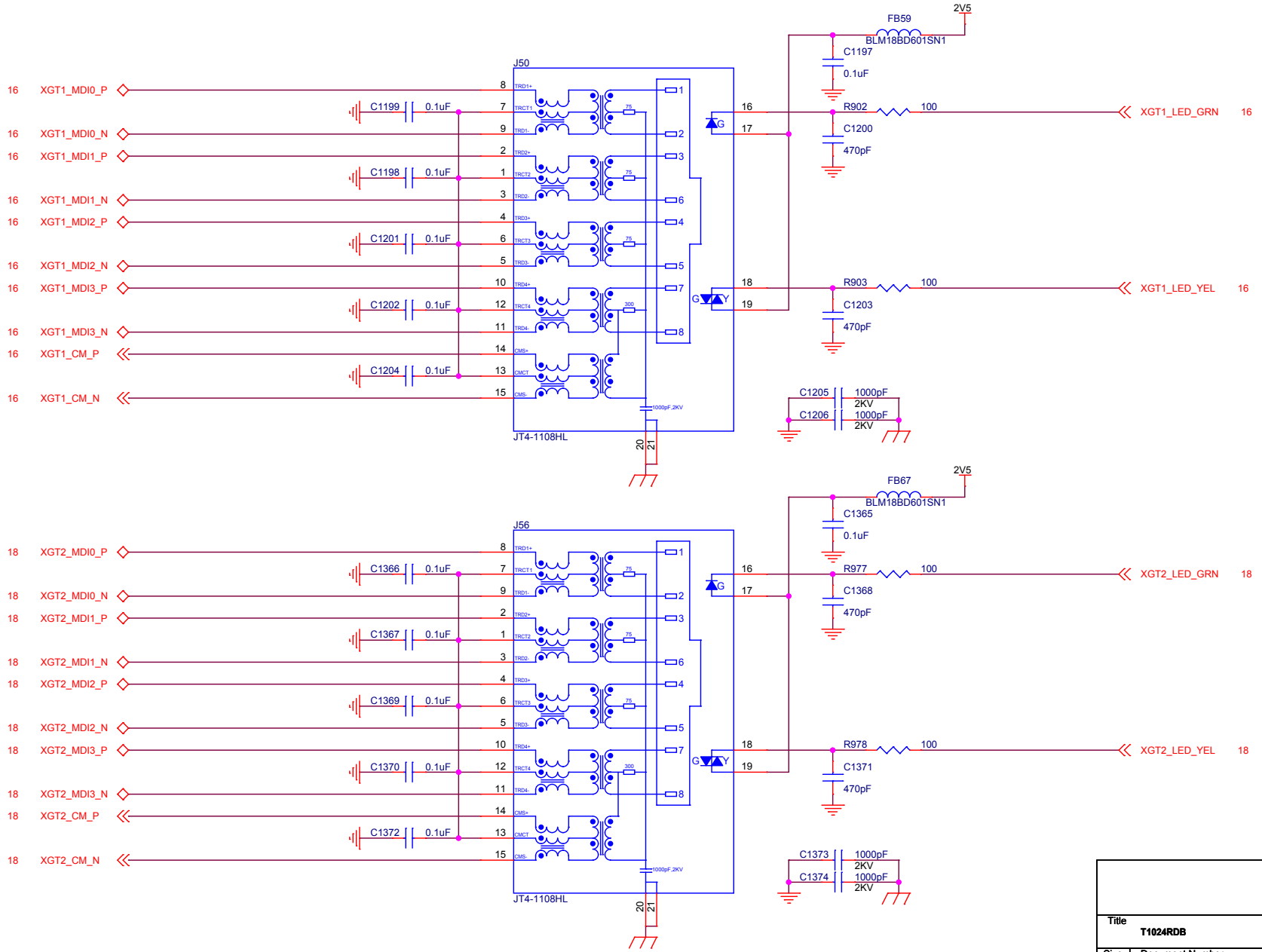
10G/2.5G BASE-T RJ46 CONNECTORs



Title: T1024RDB			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: C
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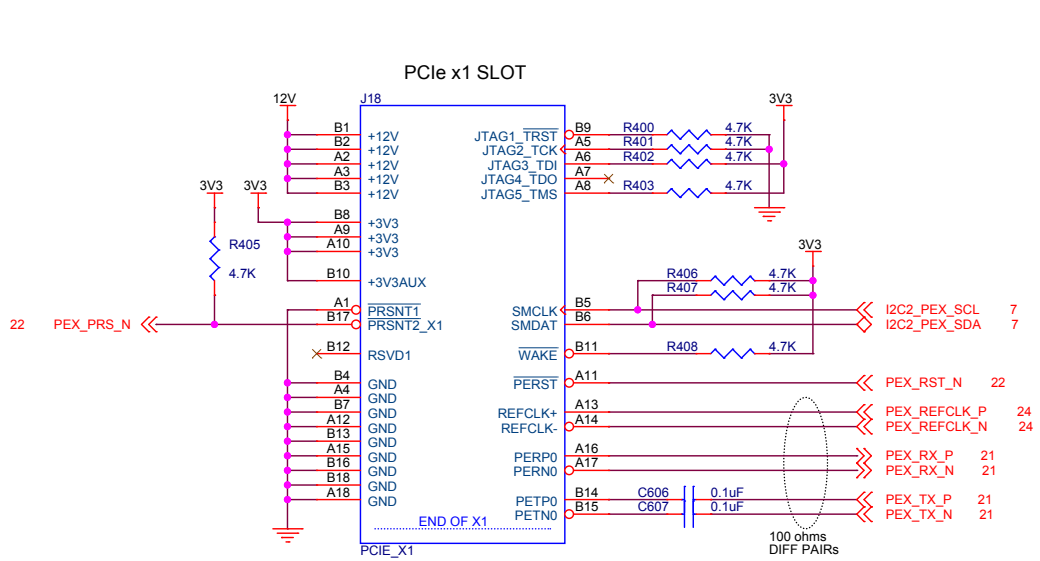
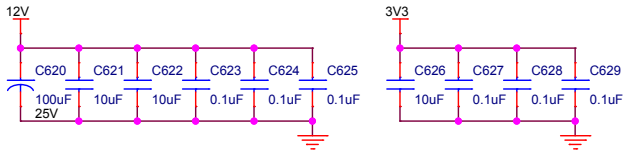
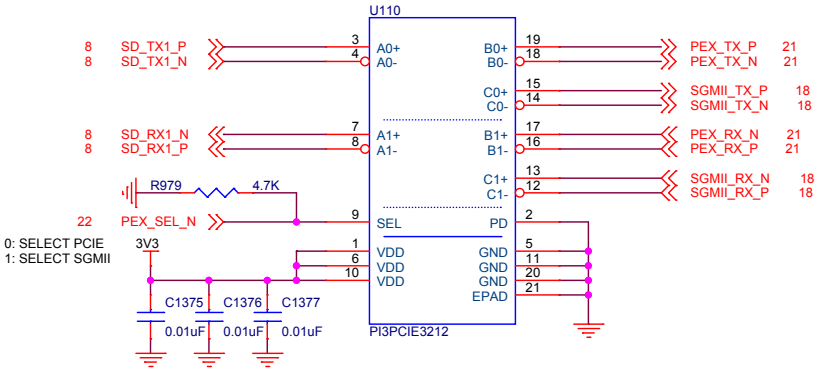
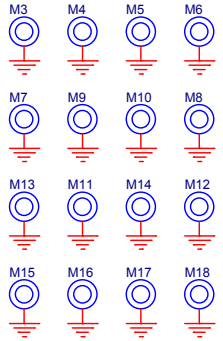
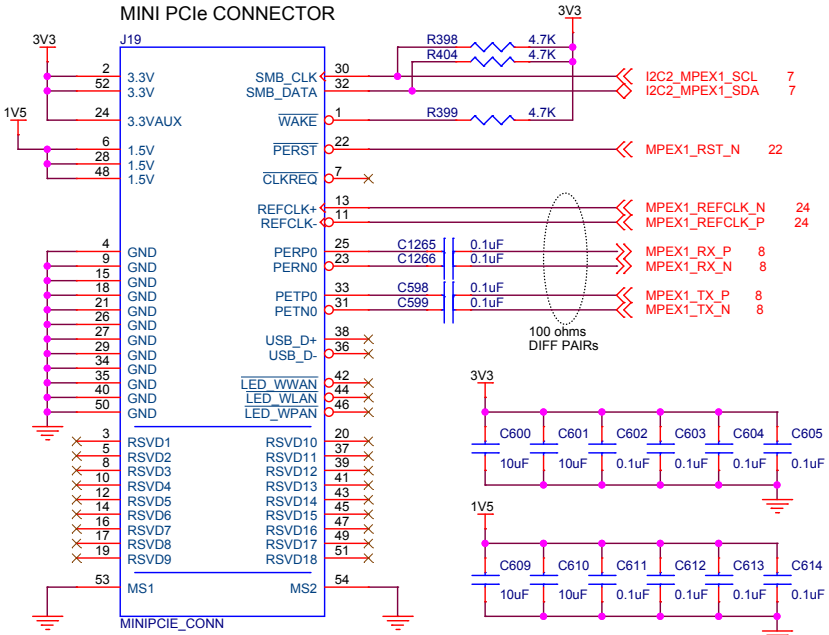
PCIe X1 SLOT and MINI PCIe CONNECTORs

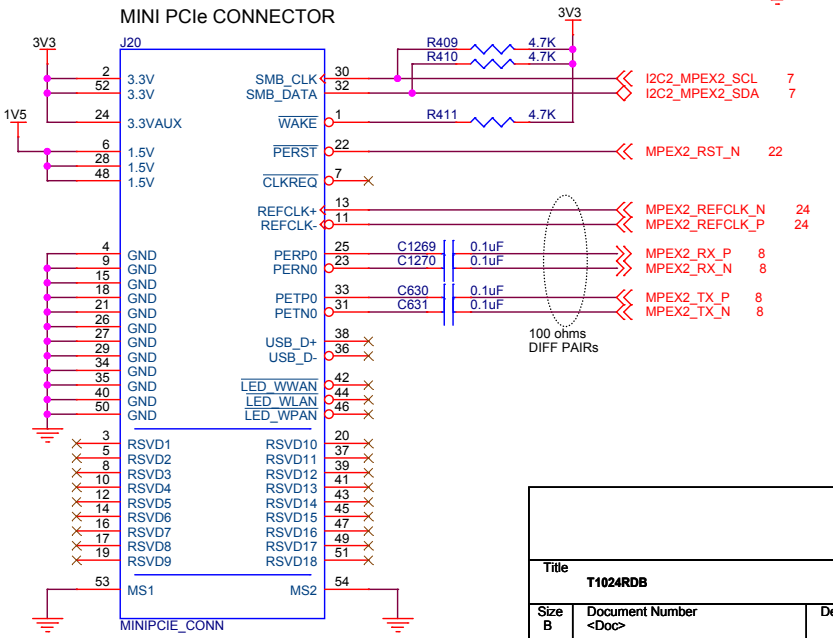












Title: T1024RDB			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: C
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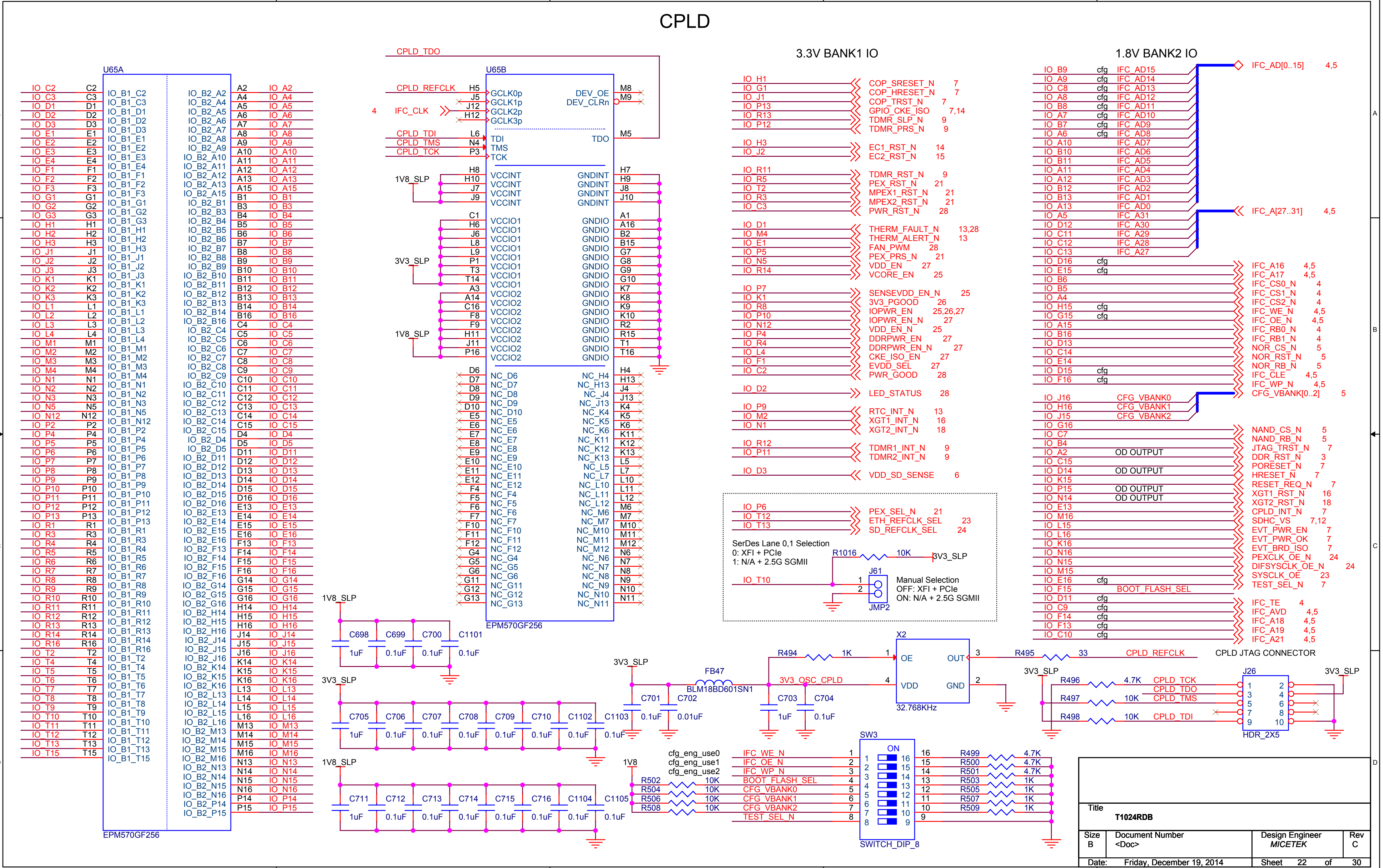

CPLD
3.3V BANK1 IO
1.8V BANK2 IO
U65A
EPM570GF256
U65B
EPM570GF256
CPLD_TDO
CPLD_REFCLK
IFC_CLK
CPLD_TDI
CPLD_TMS
CPLD_TCK
1V8_SLP
3V3_SLP
IFC_AD[0..15] 4,5
IFC_A[27..31] 4,5
CFG_VBANK[0..2] 5
SerDes Lane 0,1 Selection
0: XFI + PCIe
1: N/A + 2.5G SGMII
Manual Selection
OFF: XFI + PCIe
ON: N/A + 2.5G SGMII
J61
JMP2
R1016 10K
X2
32.768KHz
OE
OUT
VDD
GND
3V3_OSC_CPLD
FB47
BLM18BD601SN1
R494 1K
R495 33
CPLD JTAG CONNECTOR
J26
HDR_2X5
R496 4.7K
R497 10K
R498 10K
SW3
SWITCH_DIP_8
cfg_eng_use0
cfg_eng_use1
cfg_eng_use2
IFC_WE_N
IFC_OE_N
IFC_WP_N
BOOT_FLASH_SEL
CFG_VBANK0
CFG_VBANK1
CFG_VBANK2
TEST_SEL_N
OD OUTPUT
Title
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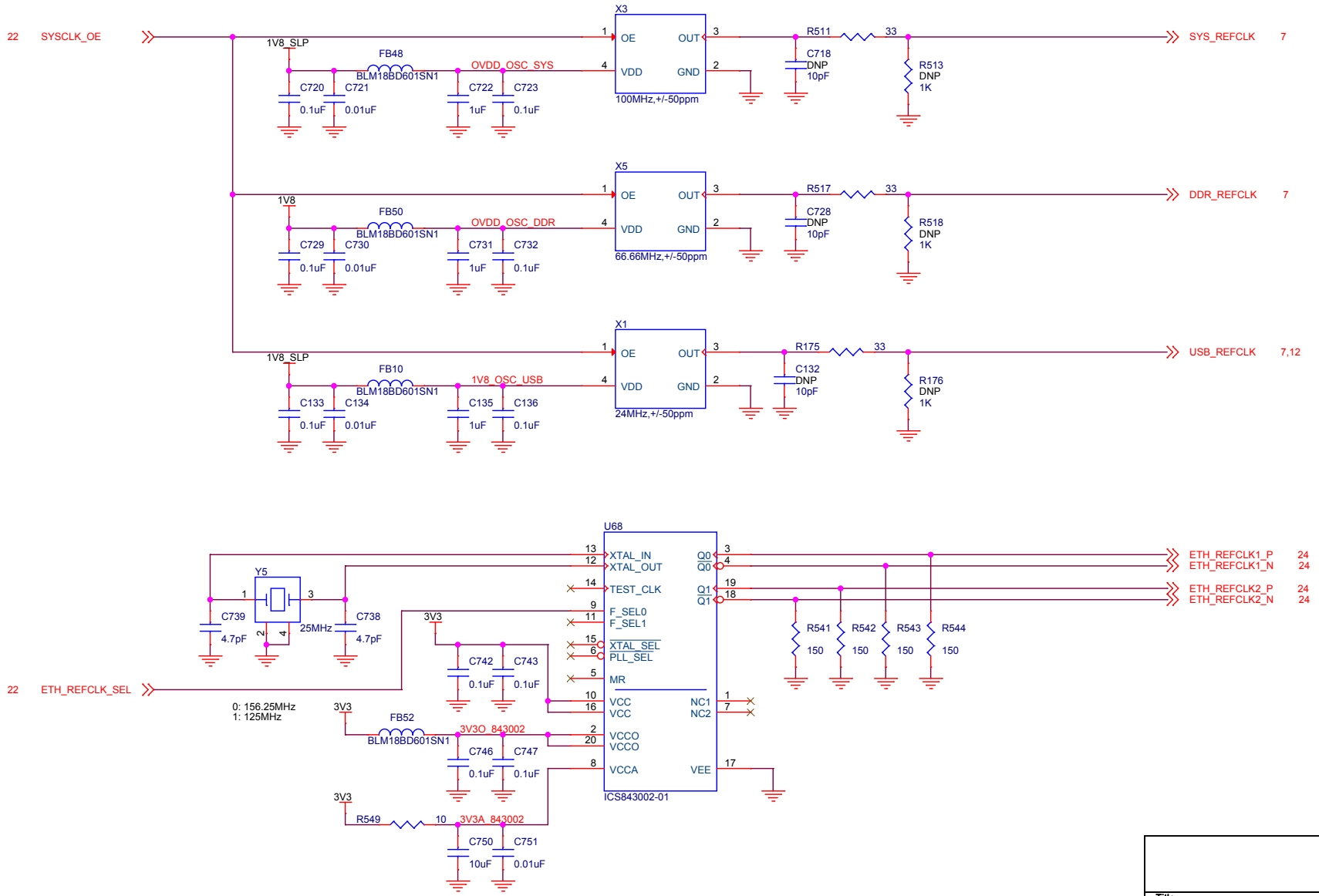
SYSTEM CLOCK GENERATORs



Title: T1024RDB			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: C
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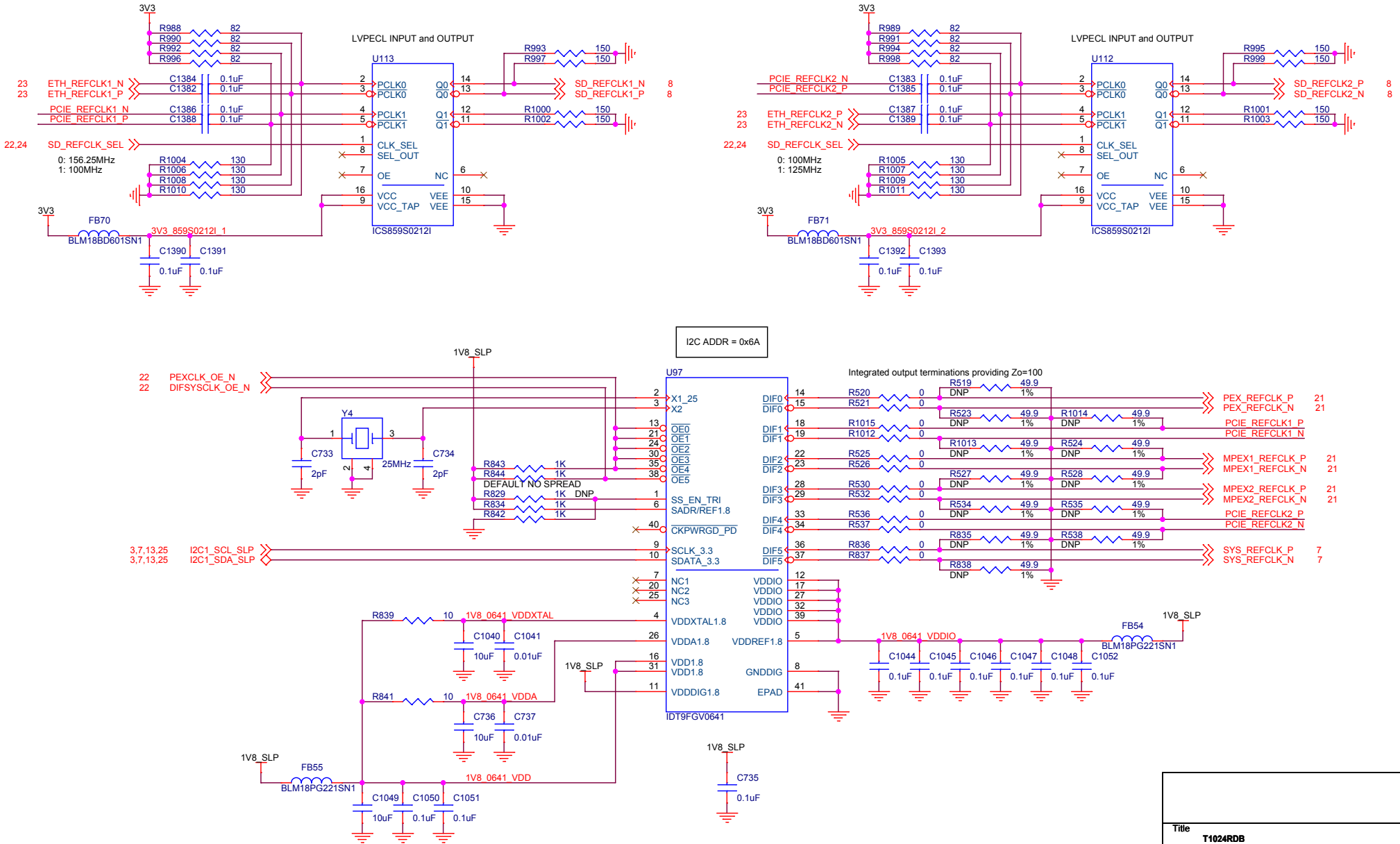
SYSTEM CLOCK GENERATORs (cont.)



Title: T1024RDB			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: C
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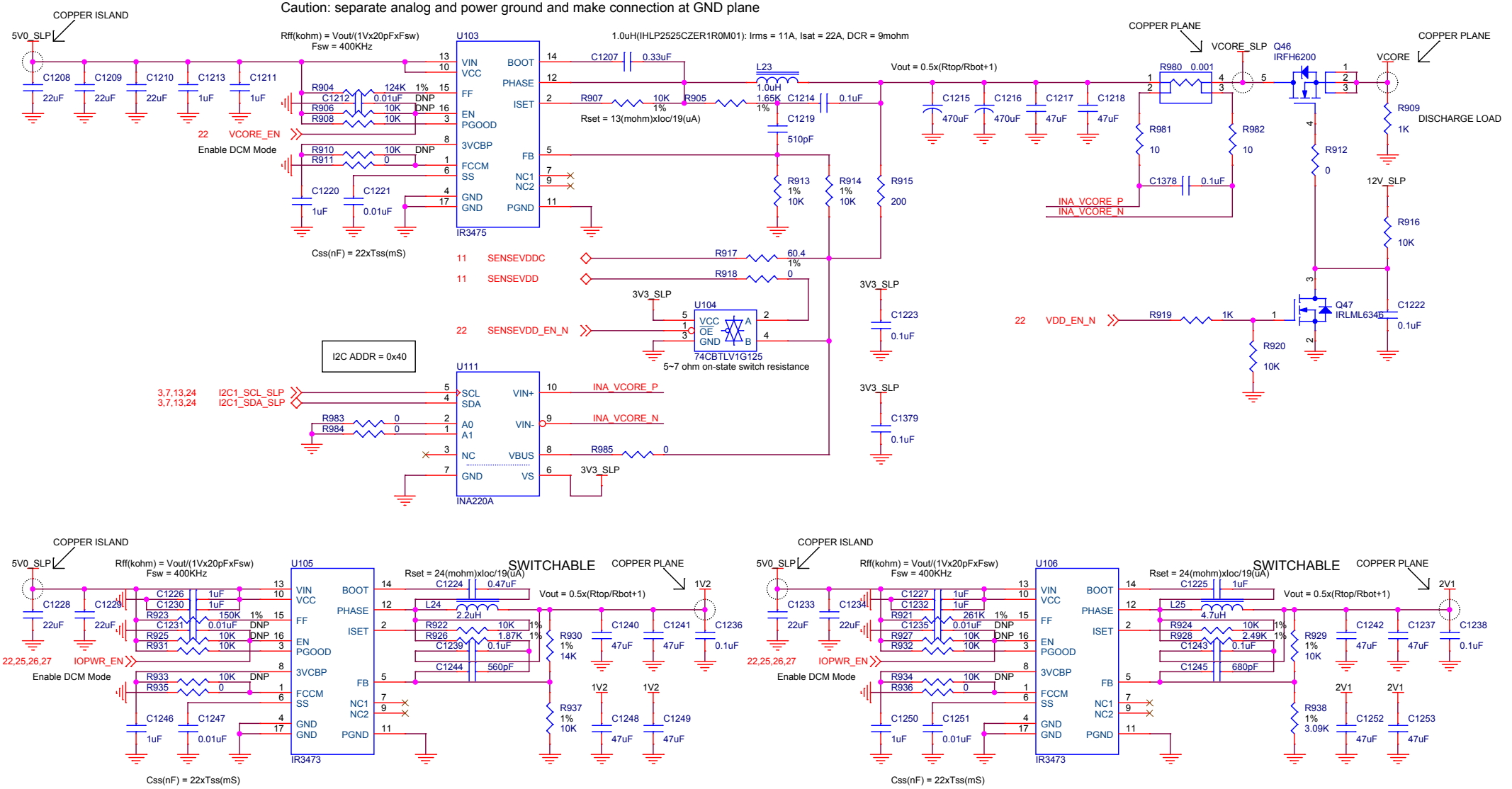
T1024 CORE POWER CONVERTOR and SYSTEM POWER CONVERTORs



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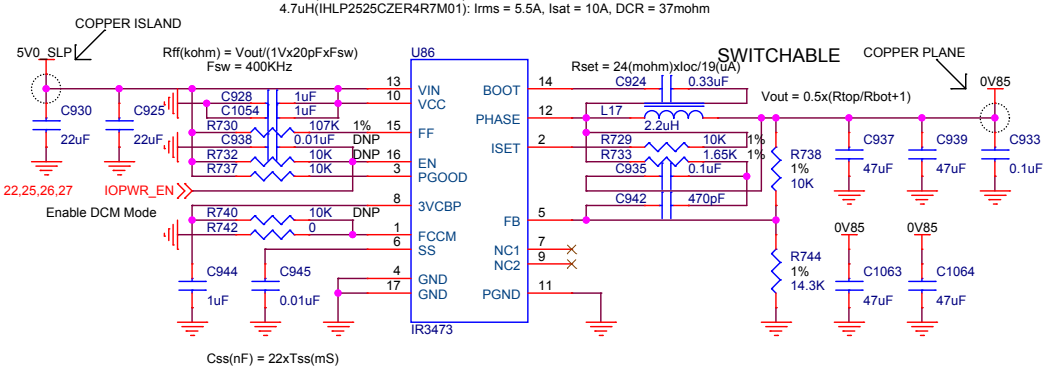
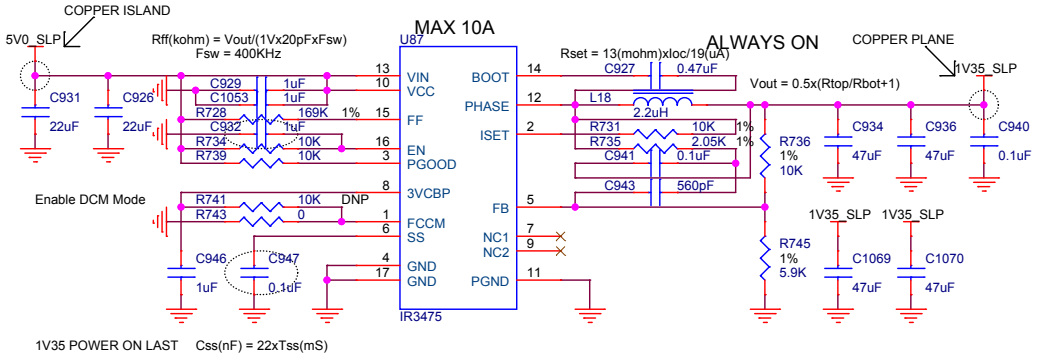
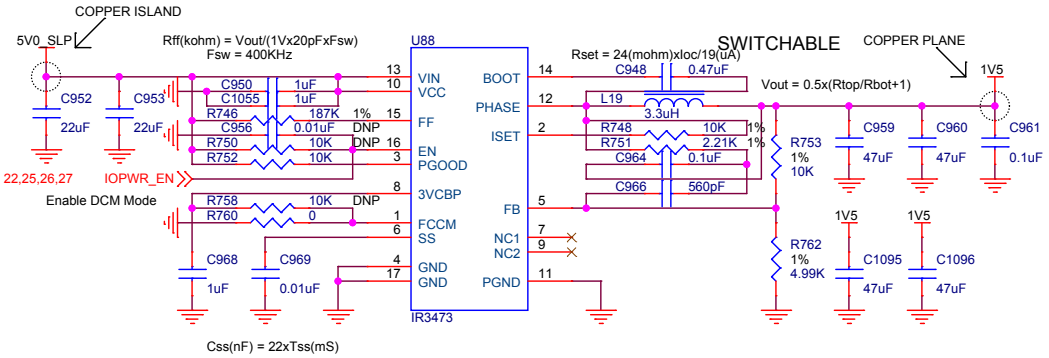
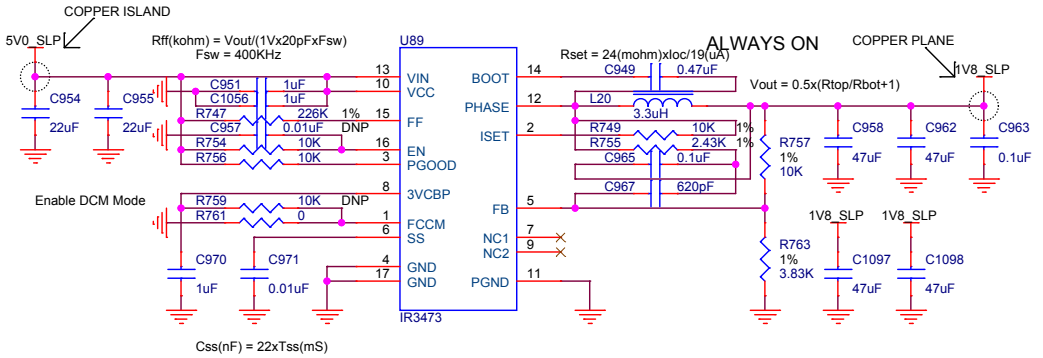
SYSTEM POWER CONVERTORs

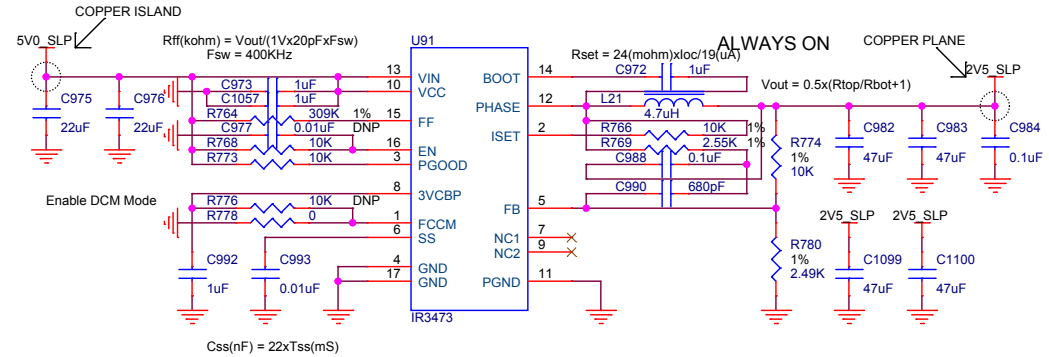
2.2uH(IHLP2525CZER2R2M01): Irms = 8A, Isat = 14A, DCR = 18mohm
3.3uH(IHLP2525CZER3R3M01): Irms = 6A, Isat = 13.5A, DCR = 28mohm
4.7uH(IHLP2525CZER4R7M01): Irms = 5.5A, Isat = 10A, DCR = 37mohm

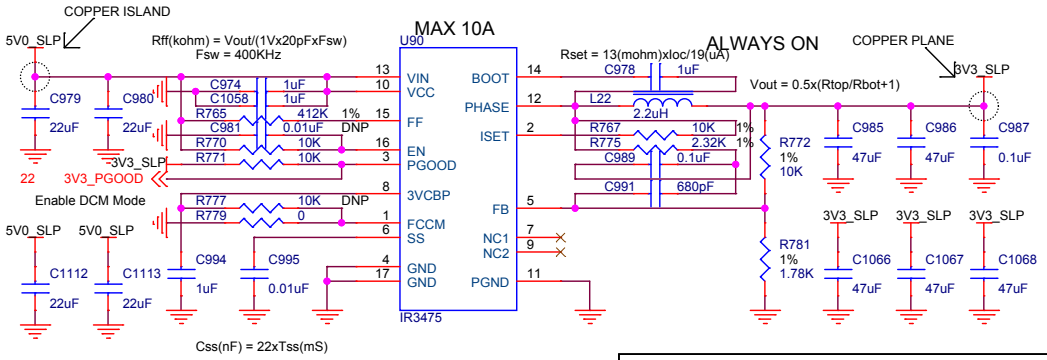












Caution: separate analog and power ground and make connection at GND plane

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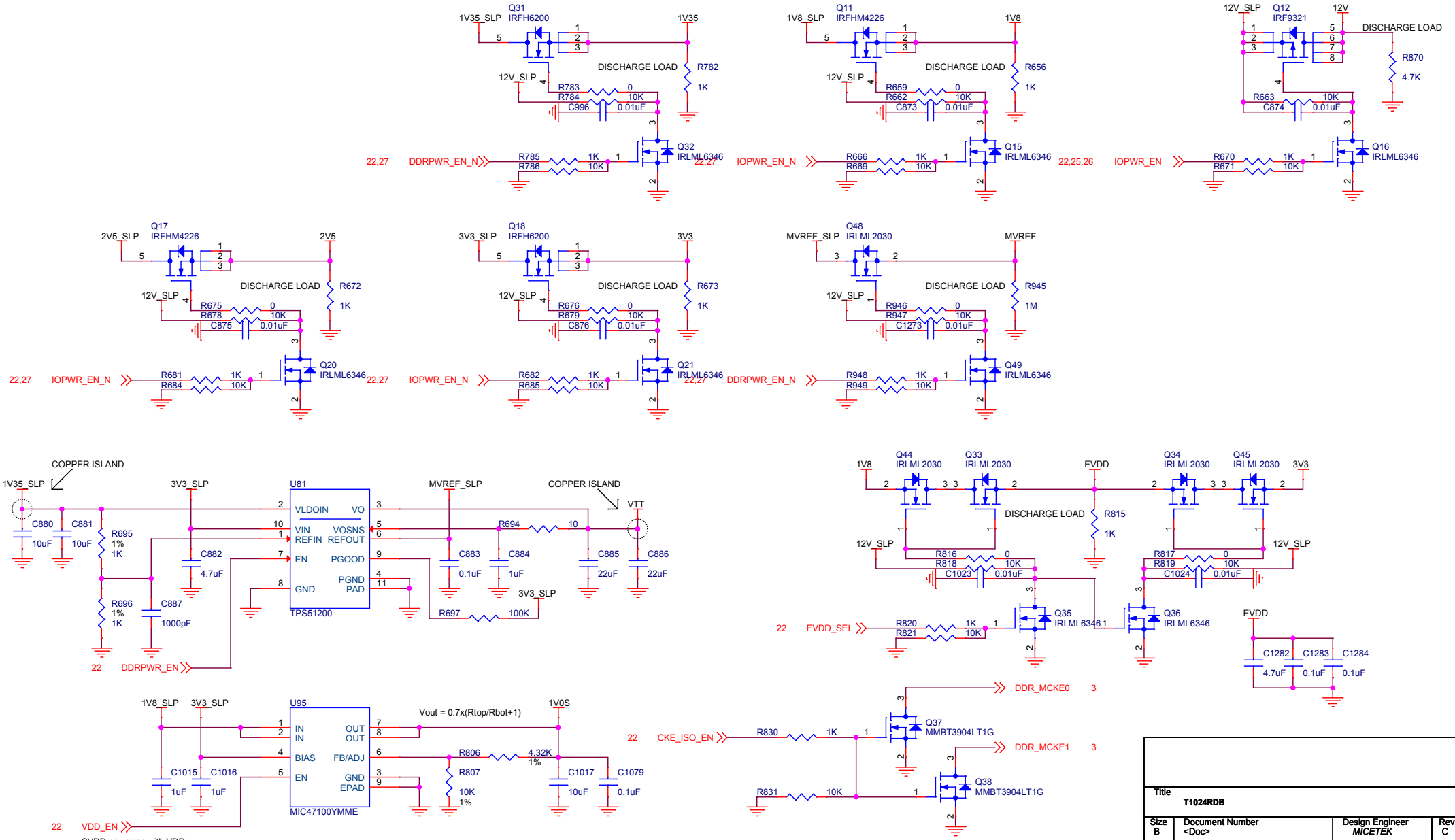
SYSTEM POWER SWITCHs



Title: T1024RDB			
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: C
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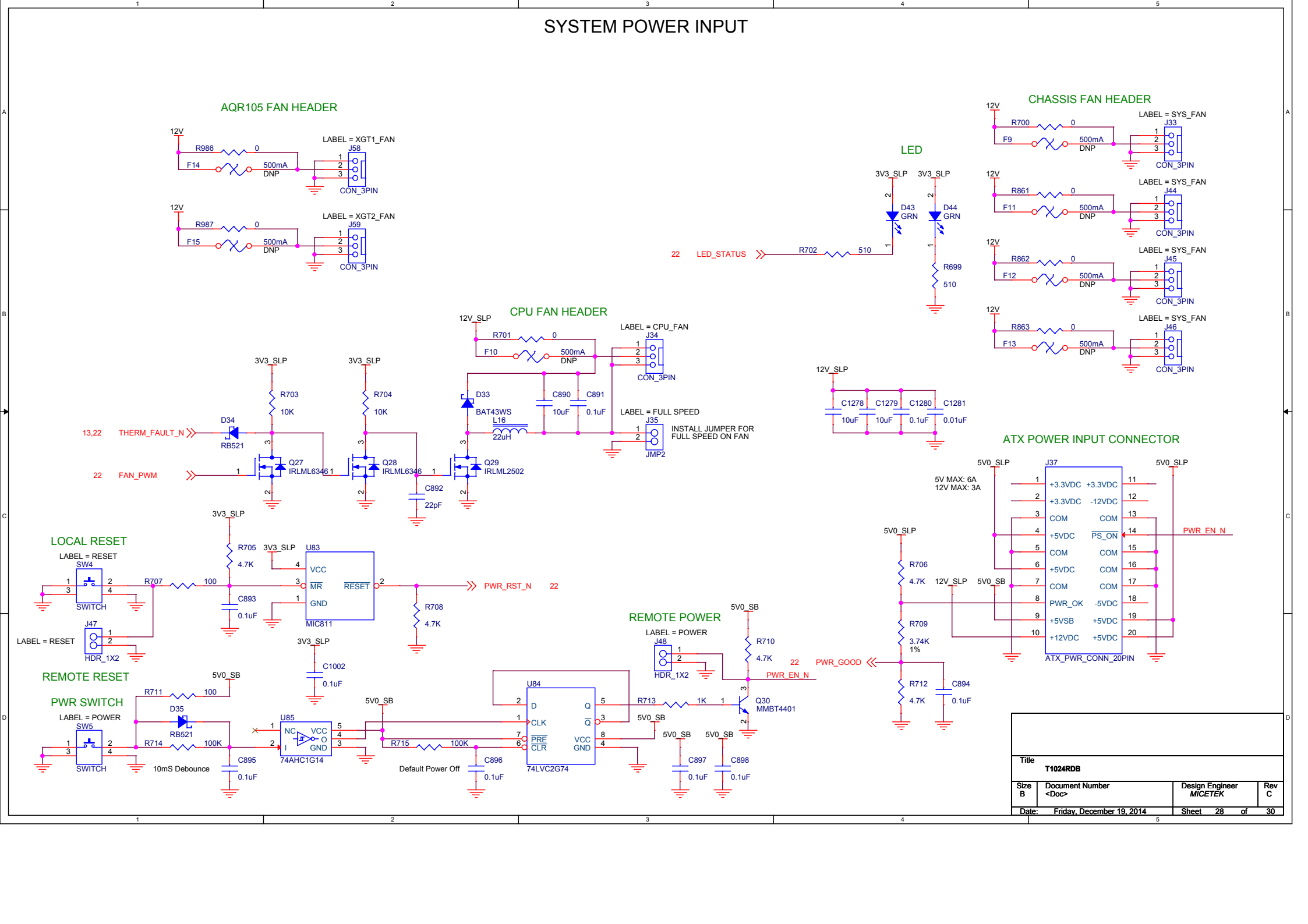
SYSTEM POWER INPUT



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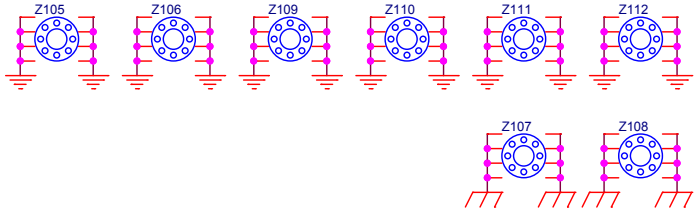
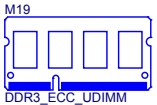
MECHANICALs

Fiducial Marks

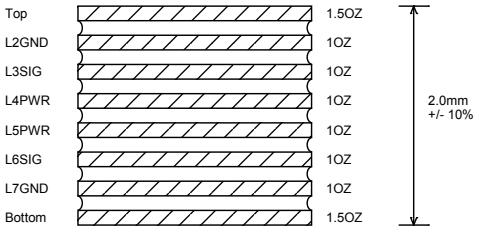
Mouting Holes





DDR3_ECC_UDIMM
Micron MPN(4GB,1600): MT18KSF51272AZ-1G6

Layer Detail



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CHANGE LIST

2014/5/19
1. Change T1040 part value to T1024
2. Add AQ2104 JTAG connector for boundry-scan
3. Change T1024 DDR power to be switched off in deep sleep mode (include D1-MVREF, GVDD, AVDD-D1)
4. Change DDR3 SPD power from 3V3 to 3V3_SLP
5. Mount R802,R803,R804 20K pull-up resistors
6. Add NOR Flash RDY/BUSY signal to CPLD
7. Connect SD card VDD pin to EVDD and correct C38, C39 power also
8. Change R158,R159 from 10K to 100K, make R155,R156 as DNP
9. Float pin1 of U38 and U96
10. Add one 3000pF capacitor on 1V0_USB_SVDD
11. Add power filter for G12 pin as AVDD_CGA2 of T1040
12. Change I2C thermal monitor power supply from 3V3 to 3V3_SLP
13. Add pull-up resistor for RTC_INT_N
14. Change EC1 RJ45 LED connection as EC2, so EC1 PHY address change to 0x02 and EC2 PHY address change to 0x06
15. Add EC1_PME_N connect to IRQ3
16. Change C336,C342,C306,C310,C1205,C1206 to 1000pF, 2KV cap
17. Add pull-up to XGT_SPI_CS_N
18. Add 3pin debug header for AQ2104 SMBUS
19. Add AC coupling capacitors on PCIe RX lines for safe
20. Change CPLD power OVDD_SLP to 1V8_SLP
21. Add 2pin Jumper for EVDD manual selection
22. Add X1 and X5 OE control from SYSCLK_OE signal
23. Change R938 to 3.09K to make 2.1V out put and correct C1252,C1253 power connection
24. Correct R916 connection from 12V_M to 12V_SLP
25. Change R744 to 14.3K to make 0.85V out put and correct C1063,C1064 power connection
26. Remove jumper for DDR3 1.5V power support

2014/5/26
1. Change USB power switch from MIC2506YM to MAX1558H
2. Change AQ2104 SPI flash AT45DB041D to MX25V4006E

2014/5/27
1. Change TVDD connect to 1V2, TVDD can be off in deep sleep mode

2014/6/1
1. Change NAND flash to 1.8V BGA NAND
2. change 2 USB protect IC to 1 for cost saving

2014/6/6
1. Change SD card VDD select by 3pin Jumper, and add sense to CPLD
2. Add all switch signals to CPLD

2014/7/2
1. Add more capacitors for EVDD

2014/7/4
1. Add beads for 2xGE port RJ45 LED signals

2014/9/18
1. Change AQ2104 to AQR105, add another AQR105 for 2.5G SGMII
2. Add serdes mux for PCIe and 2.5G SGMII
3. Add VCORE power measurement

2014/9/28
1. Change the title from 10G Base-T to 2.5G Base-T for second AQR105
2. Correct the comments above the SerDes TX pair to Lane2 used for 2.5G SGMII Mode to MAC
3. Change the signal names for 2 AQR105 JTAG and SPI to XGT1_xxx and XGT2_xxx
4. Add all XREFs for missing XREF signals
5. Add 1x1 header near VDD_SD 1x3 header for VDD_SD to connect to EVDD
6. Add 2 fan header for AQR105

2014/10/8
1. Remove C1195+C1196 and C1363+C1364 from CT of the magnetics, Change 2.2uF to 0.1uF per CT pin
2. Add a EMI2 header for debug
3. Add ferrite bead for AQR105 V22_SRDS power rails
4. Change FB57, FB65 to MPZ2012S101A
5. Change AQR105 SMB debug header pin order per reference design

2014/11/26
1. Add 2 clock mux for SD1/2_REFCLK selection
2. Change T1040 debug version resistors "V40" to "DNP"

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