**T104XRDB CPLD Registers**

**Specification**

Revision History

|  |  |  |
| --- | --- | --- |
| Rev No. | Date | Description |
| R1.0 | Jan 19, 2015 | first draft |
| R1.1 | March 3,2015 | Add MUX for QSGMII/SGMII |
| R1.2 | April 9,2015 | Reduce power on reset wait time |
| R1.3 | April 28,2015 | Add Interrupt mask |
|  |  |  |

**Register map**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Address** | **Name** | **Bit functions** | | | | | | | |
| **offset** |  | **bit0** | **bit1** | **bit2** | **bit3** | **bit4** | **bit5** | **bit6** | **bit7** |
| **00** | **CHIPID1** | CHIPID1 | | | | | | | |
| **01** | **CHIPID2** | CHIPID2 | | | | | | | |
| **02** | **HWVER** | HW\_VER | | | | | | | |
| **03** | **SWVER** | SW\_VER | | | | | | | |
| **10** | **RSTCON1** | SW\_RST | DDR\_RST | EC1\_RST | EC2\_RST | SG\_RST | QSG1\_RST | QSG2\_RST | - |
| **11** | **RSTCON2** | SG1\_RST | SG2\_RST | DVI\_RST | DFP\_RST | TDMR\_RST | PEX\_RST | MPEX1\_RST | MPEX2\_RST |
| **12** | **INTSR** | THERM\_INT | DVI/DFP\_INT | QSG1\_INT | QSG2\_INT | SG1\_INT | SG2\_INT | TDMR1\_INT | TDMR2\_INT |
| **13** | **FLHCSR** | BOOT\_SEL | BANK\_OR | SW\_BANK\_SEL0 | SW\_BANK\_SEL1 | SW\_BANK\_SEL2 | BANK\_SEL0 | BANK\_SEL1 | BANK\_SEL2 |
| **14** | **FANCSR** | STS\_LED | - | - | - | FAN\_PWM | | | |
| **15** | **INTMASKR** | THERM\_M | DVI/DFP\_M | QSG1\_M | QSG2\_M | SG1\_M | SG2\_M | TDMR1\_M | TDMR2\_M |
| **16** | **QECSR** | QE\_MUX | | PROFI\_MUX | DFP\_MODE | DFP\_BL | DFP\_BL\_PWM | | |
| **17** | **MISCCSR** | SG\_SEL | SLEEP\_EN | REQ\_MD | | TDMR\_PRS | PEX\_PRS | AURORA\_SEL | TEST\_SEL\_N |
| **18** | **BOOTOR** | - | - | - | - | - | - | - | BOOT\_OR |
| **19** | **BOOTCFG1** | rcw\_src[0:7] | | | | | | | |
| **1A** | **BOOTCFG2** | rcw\_src8 | - | svr[0:1] | | - | eng\_use[0:2] | | |

**INTMASKR: Write '1' mask related INT, Write '0' disable mask of related INT.**

**Registers detail description**

**(1) Chip ID1 register (CHIPID1 – address 0x00) bit allocation**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Bit** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
| **Symbol** | CHIPID1 | | | | | | | |
| **Access** | RO | | | | | | | |
| **Reset** | 0x55 | | | | | | | |

**Note: RO – Read Only**

**(2) Chip ID2 register (CHIPID2 – address 0x01) bit allocation**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Bit** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
| **Symbol** | CHIPID2 | | | | | | | |
| **Access** | RO | | | | | | | |
| **Reset** | 0xAA | | | | | | | |

**(3) Hardware version register (HWVER – address 0x02) bit allocation**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Bit** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
| **Symbol** | HW\_VER | | | | | | | |
| **Access** | RO | | | | | | | |
| **Reset** | x | | | | | | | |

**Hardware version register (HWVER – address 0x02) bit description**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Bit** | **Symbol** | **Value** | **Description** | **Reset** |
| 7:0 | HW\_VER |  | the version field of the hardware board. | x |

**(4) Software version register (SWVER – address 0x03) bit allocation**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Bit** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
| **Symbol** | SW\_VER | | | | | | | |
| **Access** | RO | | | | | | | |
| **Reset** | x | | | | | | | |

**Software version register (SWVER – address 0x03) bit description**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Bit** | **Symbol** | **Value** | **Description** | **Reset** |
| 7:0 | SW\_VER |  | the version field of the CPLD software. | x |

**(5) Reset control register (RSTCON – address 0x10) bit allocation**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Bit** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
| **Symbol** | SW\_RST | DDR\_RST | EC1\_RST | EC2\_RST | SG\_RST | QSG1\_RST | QSG2\_RST | - |
| **Access** | WC | WC | WC | WC | WC | WC | WC | - |
| **Reset** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Note: WC – Write Clear**

**Reset control register (RSTCON1 – address 0x10) bit description**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Bit** | **Symbol** | **Value** | **Description** | **Reset** |
| 0 | SW\_RST | 0 | No reset occurs | 0 |
|  |  | 1 | Write a logic 1 will produce whole board reset# signal, this bit can auto clear |  |
| 1 | DDR\_RST | 0 | No reset occurs | 0 |
|  |  | 1 | Write a logic 1 will produce DDR4 reset# signal, this bit can auto clear |  |
| 2 | EC1\_RST | 0 | No reset occurs | 0 |
|  |  | 1 | Write a logic 1 will produce RGMII PHY1(RTL8211E-VB) reset# signal, this bit can auto clear |  |
| 3 | EC2\_RST | 0 | No reset occurs | 0 |
|  |  | 1 | Write a logic 1 will produce RGMII PHY2(RTL8211E-VB) reset# signal, this bit can auto clear |  |
| 4 | SG\_RST | 0 | No reset occurs | 0 |
|  |  | 1 | Write a logic 1 will produce SGMII PHY(RTL8211DN) reset# signal, this bit can auto clear |  |
| 5 | QSG1\_RST | 0 | No reset occurs | 0 |
|  |  | 1 | Write a logic 1 will produce QSGMII PHY1(F104S8A) reset# signal, this bit can auto clear |  |
| 6 | QSG2\_RST | 0 | No reset occurs | 0 |
|  |  | 1 | Write a logic 1 will produce QSGMII PHY2(F104S8A) reset# signal, this bit can auto clear |  |
| 7 | - |  |  | 0 |

**(6) Reset control register (RSTCON2 – address 0x11) bit allocation**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Bit** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
| **Symbol** | SG1\_RST | SG2\_RST | DVI\_RST | DFP\_RST | TDMR\_RST | PEX\_RST | MPEX1\_RST | MPEX2\_RST |
| **Access** | WC | WC | WC | WC | WC | WC | WC | WC |
| **Reset** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Reset control register (RSTCON – address 0x11) bit description**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Bit** | **Symbol** | **Value** | **Description** | **Reset** |
| 0 | SG1\_RST | 0 | No reset occurs | 0 |
|  |  | 1 | Write a logic 1 will produce SGMII1 PHY(RTL8211DN) reset# signal, this bit can auto clear |  |
| 1 | SG2\_RST | 0 | No reset occurs | 0 |
|  |  | 1 | Write a logic 1 will produce SGMII2 PHY(RTL8211DN) reset# signal, this bit can auto clear |  |
| 2 | DVI\_RST | 0 | No reset occurs | 0 |
|  |  | 1 | Write a logic 1 will produce DVI chip CH7301C reset# signal, this bit can auto clear |  |
| 3 | DFP\_RST | 0 | No reset occurs | 0 |
|  |  | 1 | Write a logic 1 will produce DFP chip DS90C387R reset# signal, this bit can auto clear |  |
| 4 | TDMR\_RST | 0 | No reset occurs | 0 |
|  |  | 1 | Write a logic 1 will produce TDM riser card reset# signal, this bit can auto clear |  |
| 5 | PEX\_RST | 0 | No reset occurs | 0 |
|  |  | 1 | Write a logic 1 will produce PCIe x1 slot reset# signal, this bit can auto clear |  |
| 6 | MPEX1\_RST | 0 | No reset occurs | 0 |
|  |  | 1 | Write a logic 1 will produce miniPCIe card1 reset# signal, this bit can auto clear |  |
| 7 | MPEX2\_RST | 0 | No reset occurs | 0 |
|  |  | 1 | Write a logic 1 will produce miniPCIe card2 reset# signal, this bit can auto clear |  |

**(7) Interrupt status register (INTSR – address 0x12) bit allocation**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Bit** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
| **Symbol** | THERM\_INT | DVI/DFP\_INT | QSG1\_INT | QSG2\_INT | SG1\_INT | SG2\_INT | TDMR1\_INT | TDMR2\_INT |
| **Access** | RO | RO | RO | RO | RO | RO | RO | RO |
| **Reset** | x | x | x | x | x | x | x | x |

**Interrupt status register (INTSR – address 0x12) bit description**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Bit** | **Symbol** | **Value** | **Description** | **Reset** |
| 0 | THERM\_INT | 0 | No interrupt occurs | x |
|  |  | 1 | Board over temperature interrupt occurs |  |
| 1 | DVI/DFP\_INT | 0 | No interrupt occurs | x |
|  |  | 1 | DVI chip CH7301C or DFP chip DS90C387R interrupt occurs |  |
| 2 | QSG1\_INT | 0 | No reset occurs | x |
|  |  | 1 | QSGMII PHY1(F104S8A) interrupt occurs |  |
| 3 | QSG2\_INT | 0 | No reset occurs | x |
|  |  | 1 | QSGMII PHY2(F104S8A) interrupt occurs |  |
| 4 | SG1\_INT | 0 | No reset occurs | x |
|  |  | 1 | SGMII1 PHY(RTL8211DN) interrupt occurs |  |
| 5 | SG2\_INT | 0 | No reset occurs | x |
|  |  | 1 | SGMII2 PHY(RTL8211DN) interrupt occurs |  |
| 6 | TDMR1\_INT | 0 | No reset occurs | x |
|  |  | 1 | TDM riser card interrupt 1 occurs |  |
| 7 | TDMR2\_INT | 0 | No reset occurs | x |
|  |  | 1 | TDM riser card interrupt 2 occurs |  |

**Note: INTSR register is related with system IRQ0(CPLD\_INT1\_N) signal, when interrupt occurs, IRQ0 will be logic 0 until all interrupts of INTSR register clear.**

**(8) Flash control and status register (FLHCSR – address 0x13) bit allocation**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Bit** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
| **Symbol** | BOOT\_SEL | BANK\_OR | SW\_BANK\_SEL0 | SW\_BANK\_SEL1 | SW\_BANK\_SEL2 | BANK\_SEL0 | BANK\_SEL1 | BANK\_SEL2 |
| **Access** | RO | RW | RO | RO | RO | RW | RW | RW |
| **Reset** | x | 0 | x | x | x | 0 | 0 | 0 |

**Note : RW - Read and Write**

**Flash control and status register (FLHCSR – address 0x13) bit description**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Bit** | **Symbol** | **Value** | **Description** | **Reset** |
| 0 | BOOT\_SEL | 0 | Boot from 16bit NOR flash | x |
|  |  | 1 | Boot from 8bit NAND flash |  |
| 1 | BANK\_OR | 0 | NOR flash bank select from CPLD override disable | 0 |
|  |  | 1 | NOR flash bank select from CPLD override enable |  |
| 2 | SW\_BANK\_SEL0 | 0 | NOR flash bank select bit0 of switch status is 0 | x |
|  |  | 1 | NOR flash bank select bit0 of switch status is 1 |  |
| 3 | SW\_BANK\_SEL1 | 0 | NOR flash bank select bit1 of switch status is 0 | x |
|  |  | 1 | NOR flash bank select bit1 of switch status is 1 |  |
| 4 | SW\_BANK\_SEL2 | 0 | NOR flash bank select bit2 of switch status is 0 | x |
|  |  | 1 | NOR flash bank select bit2 of switch status is 1 |  |
| 5 | BANK\_SEL0 | 0 | NOR flash bank select bit0 set 0 | 0 |
|  |  | 1 | NOR flash bank select bit0 set 1 |  |
| 6 | BANK\_SEL1 | 0 | NOR flash bank select bit1 set 0 | 0 |
|  |  | 1 | NOR flash bank select bit1 set 1 |  |
| 7 | BANK\_SEL2 | 0 | NOR flash bank select bit2 set 0 | 0 |
|  |  | 1 | NOR flash bank select bit2 set 1 |  |

**(9) Fan control and status register (FANCSR – address 0x14) bit allocation**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Bit** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
| **Symbol** | STS\_LED |  |  |  | FAN\_PWM | | | |
| **Access** | RW |  |  |  | RW | | | |
| **Reset** | 0 |  |  |  | 1111 | | | |

**Fan control and status register (FANCSR – address 0x14) bit description**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Bit** | **Symbol** | **Value** | **Description** | **Reset** |
| 0 | STS\_LED | 0 | LED is off | 0 |
|  |  | 1 | LED is blink |  |
| 4:7 | FAN\_PWM | 0000 | PWM duty cycle is 0%, fan stop running | 1111 |
|  |  | 0001~1110 | PWM duty cycle is 6.7%~93.3%, fan speed control |  |
|  |  | 1111 | PWM duty cycle is 100%, fan full speed |  |

**(10) Interrupt mask register (INTMASKR – address 0x15) bit allocation**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Bit** | | **0** | **1** | | **2** | | | **3** | | **4** | | **5** | | **6** | | **7** |
| **Bit** | **0** | | | **1** | | **2** | **3** | | **4** | | **5** | | **6** | | **7** | |
| **Symbol** | THERM\_M | | | DVI/DFP\_M | | QSG1\_M | QSG2\_M | | SG1\_M | | SG2\_M | | TDMR1\_M | | TDMR2\_M | |
| **Access** | RW | | | RW | | RW | RW | | RW | | RW | | RW | | RW | |
| **Reset** | 0 | | | 0 | | 0 | 0 | | 0 | | 0 | | 0 | | 0 | |

**Interrupt status register (INTSR – address 0x12) bit description**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Bit** | **Symbol** | **Value** | **Description** | **Reset** |
| 0 | THERM\_M | 0 | Thermal interrupt is not masked. | 0 |
|  |  | 1 | Thermal interrupt is masked. |  |
| 1 | DVI/DFP\_M | 0 | DVI chip CH7301C or DFP chip DS90C387R interrupt is enabled | 0 |
|  |  | 1 | DVI chip CH7301C or DFP chip DS90C387R interrupt is disabled |  |
| 2 | QSG1\_M | 0 | QSGMII PHY1(F104S8A) interrupt is enabled | 0 |
|  |  | 1 | QSGMII PHY1(F104S8A) interrupt is disabled |  |
| 3 | QSG2\_M | 0 | QSGMII PHY2(F104S8A) interrupt is enabled | 0 |
|  |  | 1 | QSGMII PHY2(F104S8A) interrupt is disabled |  |
| 4 | SG1\_M | 0 | SGMII1 PHY(RTL8211DN) interrupt is enabled | 0 |
|  |  | 1 | SGMII1 PHY(RTL8211DN) interrupt is disabled |  |
| 5 | SG2\_M | 0 | SGMII2 PHY(RTL8211DN) interrupt is enabled | 0 |
|  |  | 1 | SGMII2 PHY(RTL8211DN) interrupt is disabled |  |
| 6 | TDMR1\_M | 0 | TDM riser card interrupt 1 is enabled | 0 |
|  |  | 1 | TDM riser card interrupt 1 is disabled |  |
| 7 | TDMR2\_M | 0 | TDM riser card interrupt 2 is enabled | 0 |
|  |  | 1 | TDM riser card interrupt 2 is disabled |  |

**(11) QE control and status register (QECSR – address 0x16) bit allocation**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Bit** | **0** | **1** | **2** | **3** | **4** | **5** | | **6** | **7** |
| **Symbol** | QE\_MUX | | PROFI\_MUX | DFP\_MODE | DFP\_BL | DFP\_BL\_PWM | | | |
| **Access** | RW | | RW | RW | RW | RW | | | |
| **Reset** | 0 | 0 | 0 | 0 | 0 | 1 | 1 | | 1 |

**QE control and status register (SFPCSR – address 0x16) bit description**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Bit** | **Symbol** | **Value** | | | **Description** | | | **Reset** | |
| 0:1 | QE\_MUX | | | 00 | | | QE connect to DVI interface | | 00 |
|  |  | | | 01 | | | QE connect to DFP interface | |  |
|  |  | | | 10 | | | QE connect to PROFIBUS interface | |  |
|  |  | | | 11 | | | QE connect to TDM riser card interface | |  |
| 2 | PROFI\_MUX | | 0 | | | UC1 used as PROFIBUS interface | | 0 | |
|  |  | | 1 | | | UC3 used as PROFIBUS interface | |  | |
| 3 | DFP\_MODE | | 0 | | | LCD MODE pin logic 0 | | 0 | |
|  |  | | 1 | | | LCD MODE pin logic 1 | |  | |
| 4 | DFP\_BL | | 0 | | | LCD backlight off | | 0 | |
|  |  | | 1 | | | LCD backlight on | |  | |
| 5:7 | DFP\_BL\_PWM | | | 000 | | | PWM duty cycle is 0%, backlight off | | 111 |
|  |  | | | 001~110 | | | PWM duty cycle is 14.3.7%~85.7%, backlight control | |  |
|  |  | | | 111 | | | PWM duty cycle is 100%, highest backlight | |  |

**(12) Miscellanies control and status register (MISCCSR – address 0x17) bit allocation**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Bit** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
| **Symbol** | SG\_SEL | SLEEP\_EN | REQ\_MD | | TDMR\_PRS | PEX\_PRS | AURORA\_SEL | TEST\_SEL\_N |
| **Access** | RW | RW | RW | | RO | RO | RW | RO |
| **Reset** | 0 | 0 | 01 | | x | x | 0 | x |

**Miscellanies control and status register (MISCCSR – address 0x17) bit description**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Bit** | **Symbol** | | **Value** | **Description** | | **Reset** |
| 0 | SG\_SEL | | 0 | QSGMII1&2 PHY connect to SerDes lane2&3 | | 0 |
|  |  | | 1 | SGMII1&2 PHY connect to SerDes lane2&3 | |  |
| 1 | SLEEP\_EN | | 0 | Normal operation | | 0 |
|  |  | | 1 | Deep sleep enable bit  Before enter deep sleep mode, set ‘1’ to this bit, after exit deep sleep mode, set ‘0’ to this bit | |  |
| 2:3 | REQ\_MD | 00 | | No reset occurs when HRESET\_REQ triggered | 0x01 | |
|  |  | 01 | | HRESET occurs when HRESET\_REQ triggered |  | |
|  |  | 10 | | NA |  | |
|  |  | 11 | | PORESET occurs when HRESET\_REQ triggered |  | |
| 4 | TDMR\_PRS | | 0 | TDM riser card not present | | x |
|  |  | | 1 | TDM riser card present | |  |
| 5 | PEX\_PRS | | 0 | PCIe x4 card not present | | x |
|  |  | | 1 | PCIe x4 card present | |  |
| 6 | AURORA\_SEL | | 0 | PCIe x1 slot connect to SerDes lane4 | | 0 |
|  |  | | 1 | Aurora port connect to SerDes lane4 | |  |
| 7 | TEST\_SEL\_N | | 0 | TEST\_SEL\_N pin status is 0 | | x |
|  |  | | 1 | TEST\_SEL\_N pin status is 1 | |  |

**(13) Boot configuration override register (BOOTOR – address 0x18) bit allocation**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Bit** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
| **Symbol** | - | - | - | - | - | - | - | BOOT\_OR |
| **Access** |  |  |  |  |  |  |  | RW |
| **Reset** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Boot configuration override register (BOOTOR – address 0x18) bit description**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Bit** | **Symbol** | **Value** | **Description** | **Reset** |
| 7:1 | - |  |  | 0x0 |
| 0 | BOOT\_OR | 0 | Boot configuration from CPLD override disable | 0 |
|  |  | 1 | Boot configuration from CPLD override enable |  |

**(14) Boot configuration register 1 (BOOTCFG1 – address 0x19) bit allocation**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Bit** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
| **Symbol** | cfg\_rcw\_src[0:7] | | | | | | | |
| **Access** | RW | | | | | | | |
| **Reset** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Note: for more information, refer to T1040 datasheet.**

**(15) Boot configuration register 2 (BOOTCFG2 – address 0x1A) bit allocation**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Bit** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
| **Symbol** | cfg\_rcw\_src8 | - | cfg\_svr[0:1] | | - | cfg\_eng\_use[0:2] | | |
| **Access** | RW |  | RW | RW |  | RW | RW | RW |
| **Reset** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Note: for more information, refer to T1040 datasheet.**