8MPLUSLPD4-CPU

(i.MX8M Plus Reference Board)

Table of Content

Revision History

Rev. Code	Date	By	Description
A	*2019-10-25*	*Frank*	*Initial version*
A1	*2020-04-28*	*Frank*	*1. Update the block diagram, change "OTG" to "Dual Role"* *2. Change R74 to 4.7M, and change the state from DNP to populate.* *3. Change U1 part number from "MIMX8MP8DVNLZAA" to "MIMX8ML8DVNLZAA".*
A2	*2020-10-20*	*Frank*	*1. Update U1 part number from "MIMX8ML8DVNLZAA" to "MIMX8ML8DVNLZAB".* *2. Update U1 symbol:* *Change USB1_ID to USB1_DNU, USB2_ID to USB2_DNU, MIPI_VREG2_CAP to MIPI_TEST_DNU;* *Remove DDR3L option for DDR interface.* *3. Remove the signal connections for USB1_DNU(USB1_ID), USB2_DNU(USB2_ID).* *4. DNP the decoupling capacitor C106 for MIPI_TEST_DNU(MIPI_VREG2_CAP), can be floating for normal use.* *5. Update the Power Sequence and Operating Range Table on Page 11.*
A3	*2021-01-11*	*Frank*	*1. Change "X-8MPLUSLPD4-CPU" to "8MPLUSLPD4-CPU" for mass production.* *2. Remove the text "NXP CONFIDENTIAL AND PROPRIETARY" on each page.*

1. Interrupted lines coded with the same letter or letter combinations are electrically connected.

2. Device type number is for reference only. The number varies with the manufacturer.

3. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

4. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

Preliminary - Subject to Change without Notice!

This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with i.MX processors. Although best design practices have been applied, some areas may not be suitable for a mass-production design.

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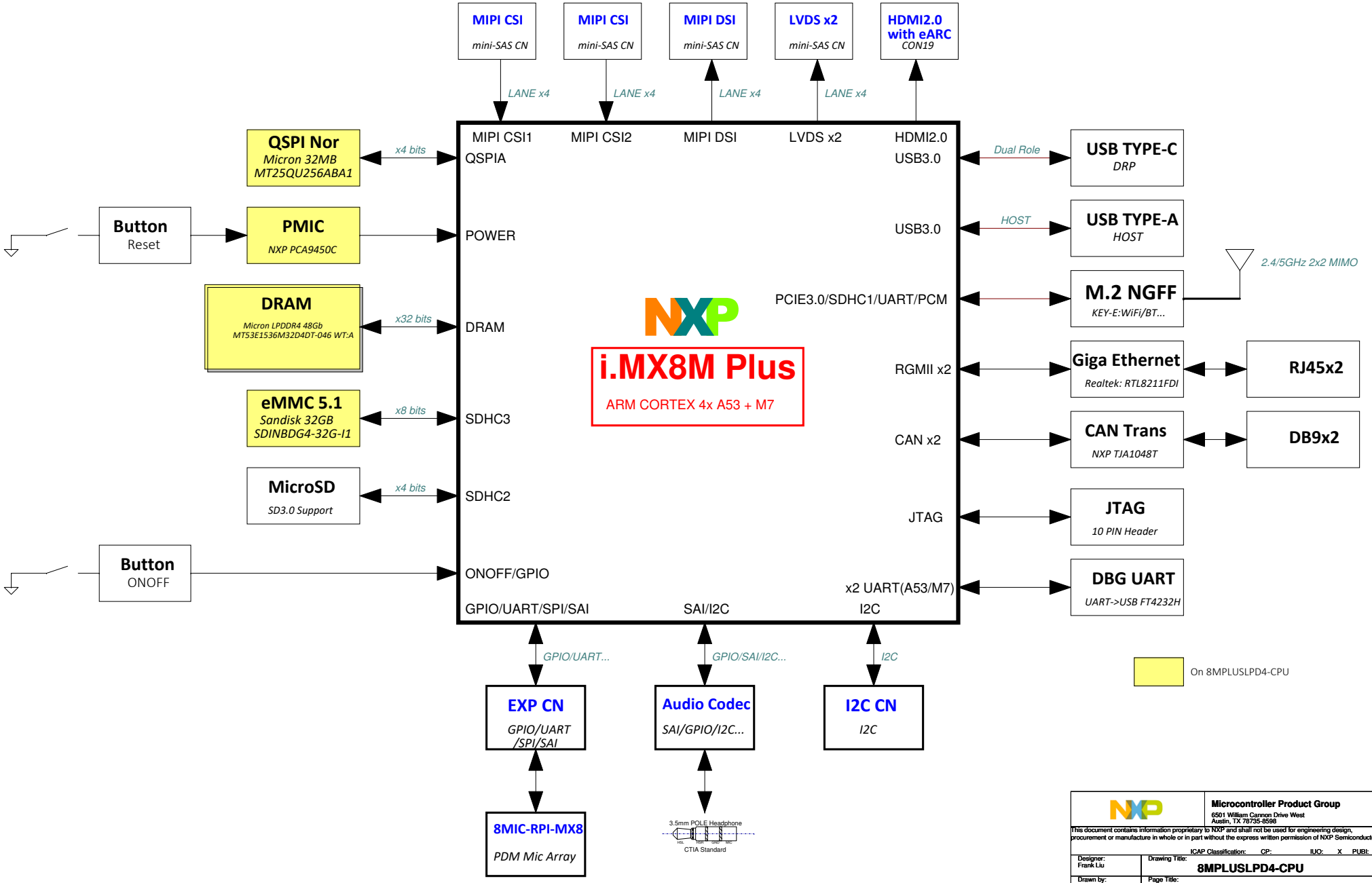
Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: IUO: X PUBI:

Designer: Frank Liu	Drawing Title: 8MPLUSLPD4-CPU	
Drawn by: Frank Liu	Page Title: Title and Rev History	
Approved: <Approver>	Size C / Document Number SCH-46368 PDF: SPF-46368	Rev A3
	Date: Monday, January 11, 2021	Sheet 1 of 12

IMX8MPLUSLPD4-EVK Block Diagram



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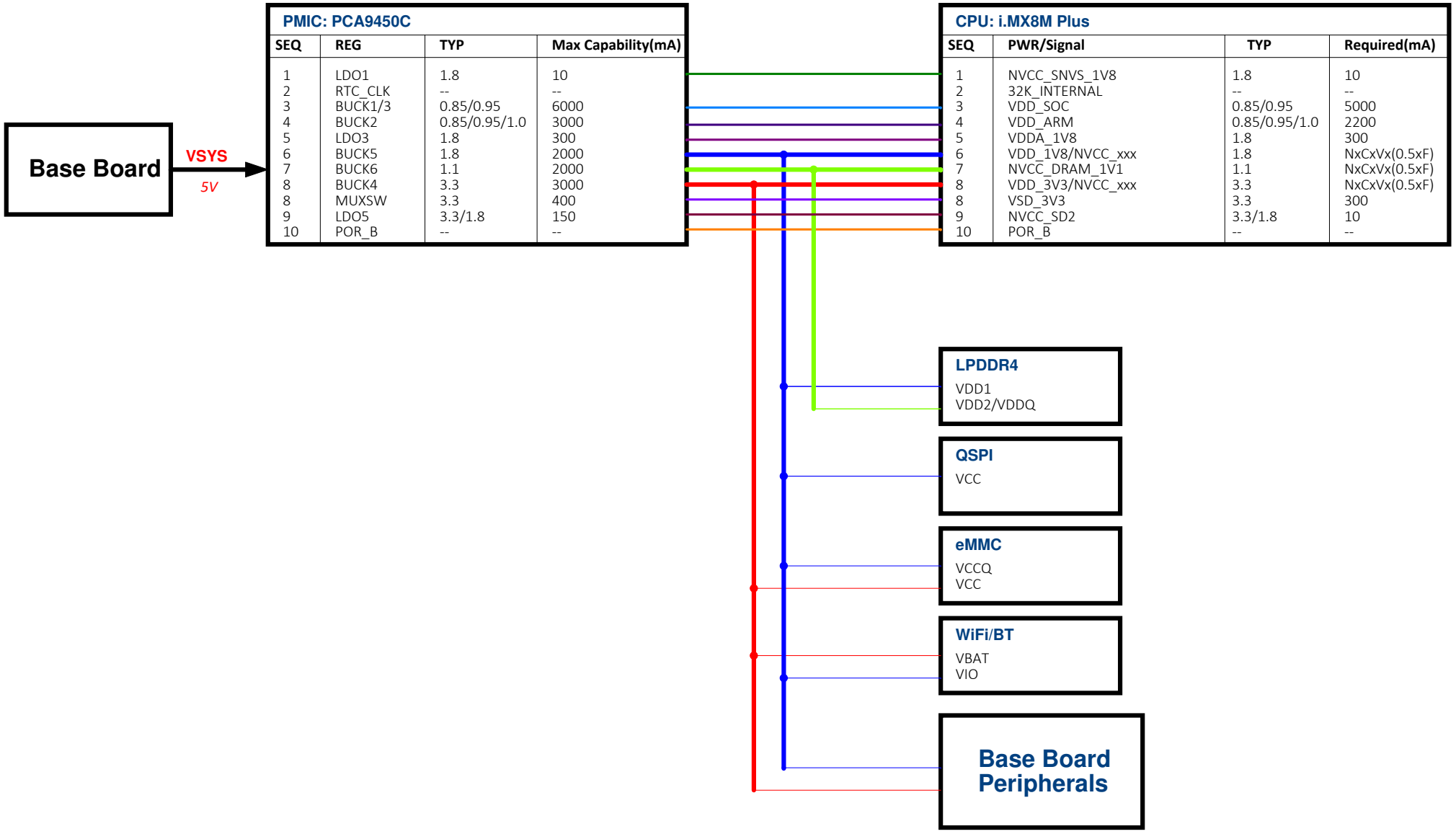
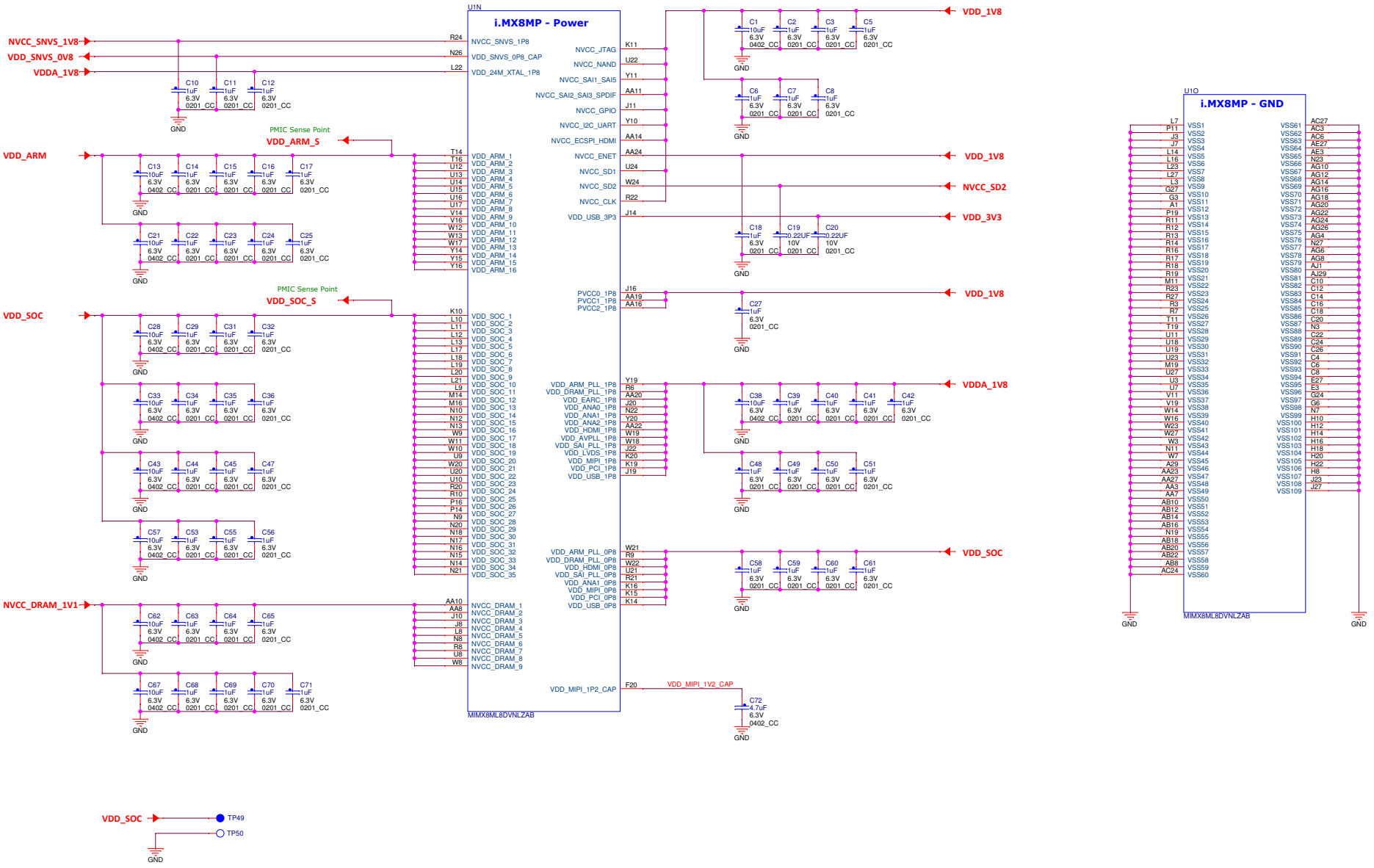
Designer: Frank Liu	Drawing Title:	8MPLUSLPD4-CPU
Drawn by: Frank Liu	Page Title:	Block Diagram
Approved: <Approver>	Size: C / Document Number: SCH-46368 PDF: SPF-46368	Rev: A3
	Date: Wednesday, November 18, 2020	Sheet 2 of 12

8MPLPD4-EVK PWR TREE



Designer: Frank Liu	Drawing Title: 8MPLUSLPD4-CPU	
Drawn by: Frank Liu	Page Title: Power Tree	
Approved: <Approver>	Size C	Document Number SCH-46368 PDF: SPF-46368 Rev A3
	Date: Wednesday, November 18, 2020	Sheet 3 of 12

i.MX8M Plus PWR



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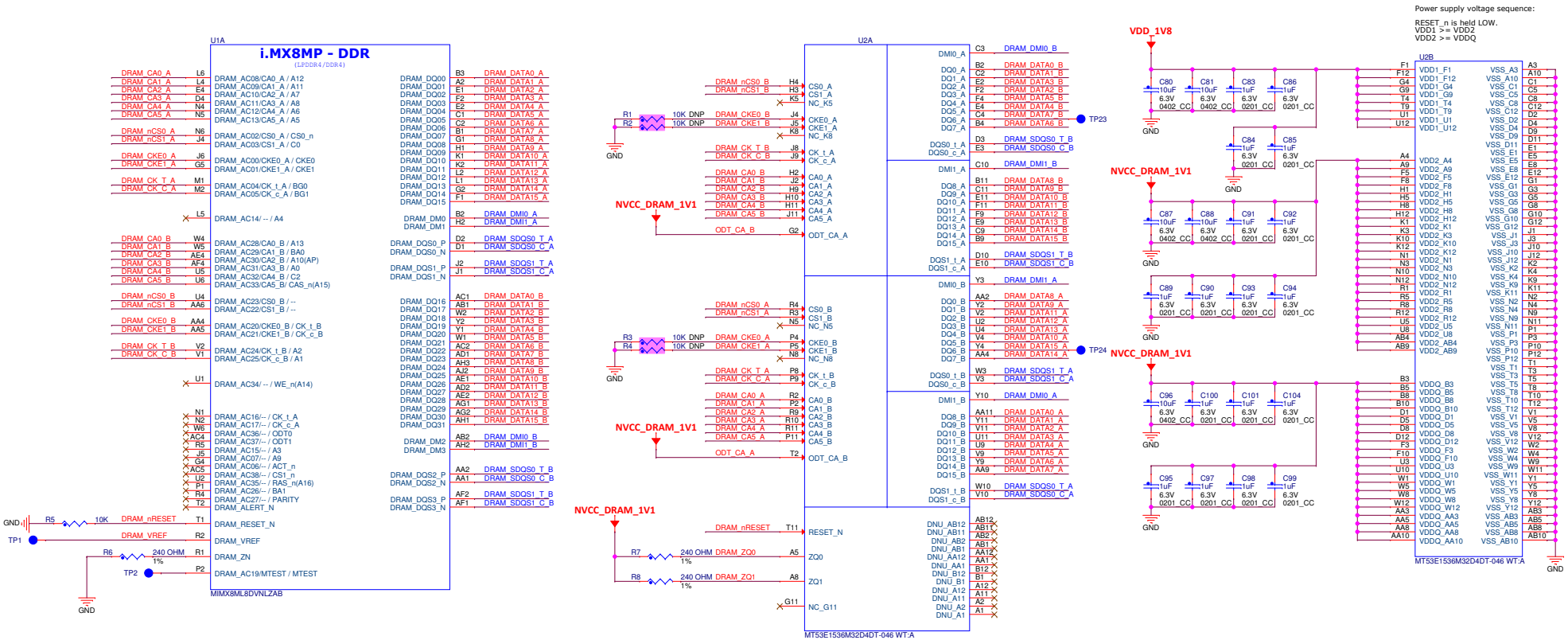
	Date: Wednesday, November 18, 2020	Sheet 4 of 12

LPDDR4 6GB

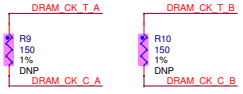


Data Bus

Pin Name	LPDDR4	DDR4
DRAM_DQS0_P	DQS0_t_A	DQSL_t_A
DRAM_DQS0_N	DQS0_c_A	DQSL_c_A
DRAM_DM0	DMI0_A	DML_n_A / DBIL_n_A
DRAM_DQ00	DQ0_A	DQL0_A
DRAM_DQ01	DQ1_A	DQL1_A
DRAM_DQ02	DQ2_A	DQL2_A
DRAM_DQ03	DQ3_A	DQL3_A
DRAM_DQ04	DQ4_A	DQL4_A
DRAM_DQ05	DQ5_A	DQL5_A
DRAM_DQ06	DQ6_A	DQL6_A
DRAM_DQ07	DQ7_A	DQL7_A
DRAM_DQS1_P	DQS1_t_A	DQSU_t_A
DRAM_DQS1_N	DQS1_c_A	DQSU_c_A
DRAM_DM1	DMI1_A	DMU_n_A / DBIU_n_A
DRAM_DQ08	DQ8_A	DQU0_A
DRAM_DQ09	DQ9_A	DQU1_A
DRAM_DQ10	DQ10_A	DQU2_A
DRAM_DQ11	DQ11_A	DQU3_A
DRAM_DQ12	DQ12_A	DQU4_A
DRAM_DQ13	DQ13_A	DQU5_A
DRAM_DQ14	DQ14_A	DQU6_A
DRAM_DQ15	DQ15_A	DQU7_A
DRAM_DQS2_P	DQS0_t_B	DQSL_t_B
DRAM_DQS2_N	DQS0_c_B	DQSL_c_B
DRAM_DM2	DMI0_B	DML_n_B / DBIL_n_B
DRAM_DQ16	DQ0_B	DQL0_B
DRAM_DQ17	DQ1_B	DQL1_B
DRAM_DQ18	DQ2_B	DQL2_B
DRAM_DQ19	DQ3_B	DQL3_B
DRAM_DQ20	DQ4_B	DQL4_B
DRAM_DQ21	DQ5_B	DQL5_B
DRAM_DQ22	DQ6_B	DQL6_B
DRAM_DQ23	DQ7_B	DQL7_B
DRAM_DQS3_P	DQS1_t_B	DQSU_t_B
DRAM_DQS3_N	DQS1_c_B	DQSU_c_B
DRAM_DM3	DMI1_B	DMU_n_B / DBIU_n_B
DRAM_DQ24	DQ8_B	DQU0_B
DRAM_DQ25	DQ9_B	DQU1_B
DRAM_DQ26	DQ10_B	DQU2_B
DRAM_DQ27	DQ11_B	DQU3_B
DRAM_DQ28	DQ12_B	DQU4_B
DRAM_DQ29	DQ13_B	DQU5_B
DRAM_DQ30	DQ14_B	DQU6_B
DRAM_DQ31	DQ15_B	DQU7_B

Command/Address

Pin Name	LPDDR4	DDR4
DRAM_RESET_N	RESET_N	RESET_n
DRAM_ALERT_N	MTEST1	ALERT_n / MTEST1
DRAM_AC00	CKE0_A	CKE0
DRAM_AC01	CKE1_A	CKE1
DRAM_AC02	CS0_A	CS0_n
DRAM_AC03	CS1_A	C0
DRAM_AC04	CK_t_A	BG0
DRAM_AC05	CK_c_A	BG1
DRAM_AC06	/	ACT_n
DRAM_AC07	/	A9
DRAM_AC08	CA0_A	A12
DRAM_AC09	CA1_A	A11
DRAM_AC10	CA2_A	A7
DRAM_AC11	CA3_A	A8
DRAM_AC12	CA4_A	A6
DRAM_AC13	CA5_A	A5
DRAM_AC14	/	A4
DRAM_AC15	/	A3
DRAM_AC16	/	CK_t_A
DRAM_AC17	/	CK_c_A
DRAM_AC19	MTEST	MTEST
DRAM_AC20	CKE0_B	CK_t_B
DRAM_AC21	CKE1_B	CK_c_B
DRAM_AC22	CS1_B	/
DRAM_AC23	CS0_B	/
DRAM_AC24	CK_t_B	A2
DRAM_AC25	CK_c_B	A1
DRAM_AC26	/	BA1
DRAM_AC27	/	PARITY
DRAM_AC28	CA0_B	A13
DRAM_AC29	CA1_B	BA0
DRAM_AC30	CA2_B	A10 / AP
DRAM_AC31	CA3_B	A0
DRAM_AC32	CA4_B	C2
DRAM_AC33	CA5_B	CAS_n / A15
DRAM_AC34	/	WE_n / A14
DRAM_AC35	/	RAS_n / A16
DRAM_AC36	/	ODT0
DRAM_AC37	/	ODT1
DRAM_AC38	/	CS1_n
DRAM_ZN	ZQ	ZQ
DRAM_VREF	VREF	VREF



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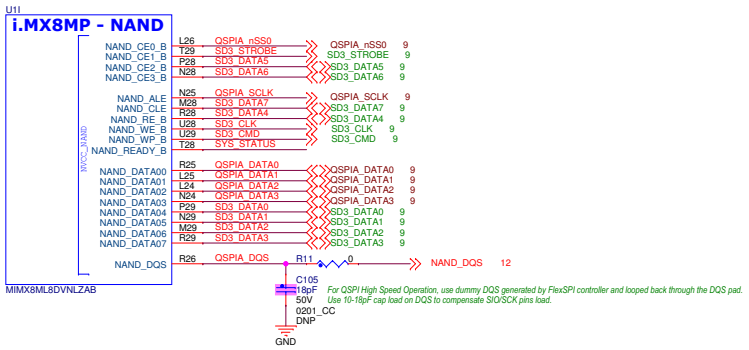
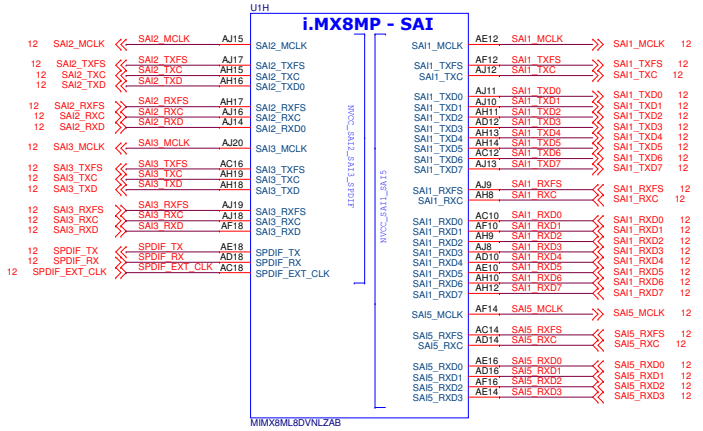
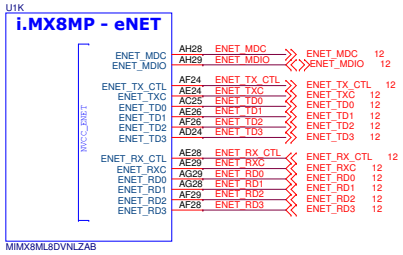
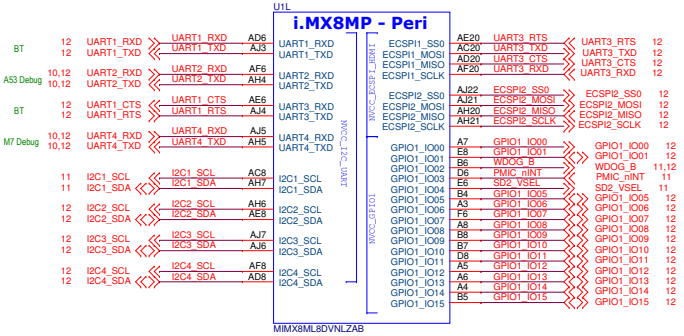
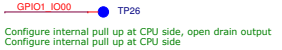
i.MX8M Plus IO Interface

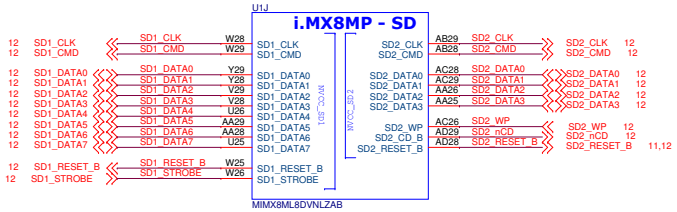


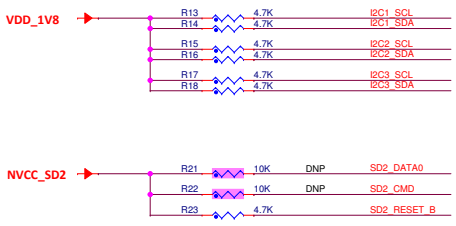


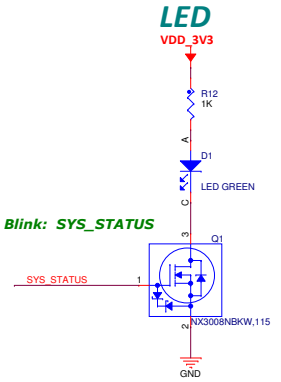












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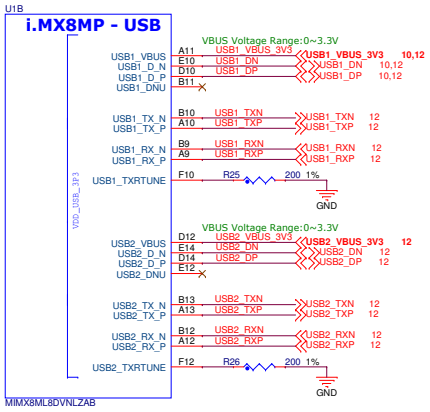
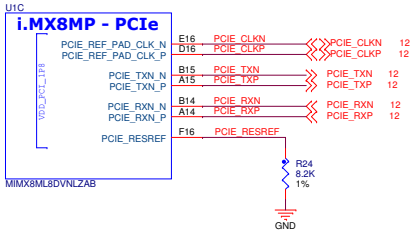
i.MX8M Plus PHYs

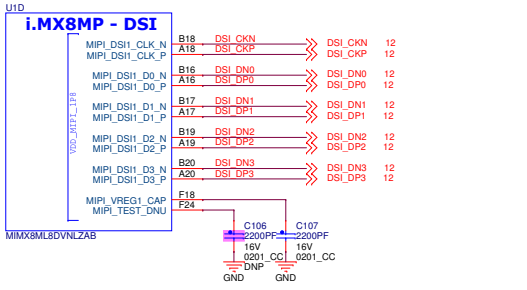


Note:

1. USB1_DNU, USB2_DNU are not functional, if USB ID function is needed, use common GPIO.

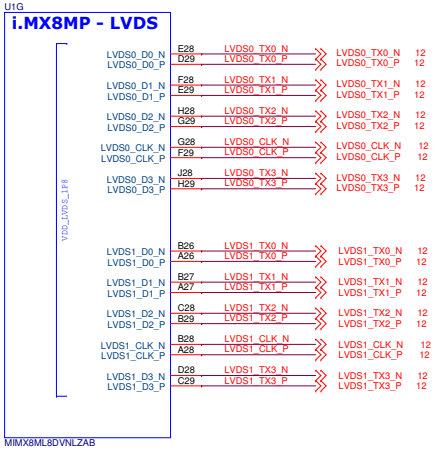
2. If USB connector is MicroAB or MicroB, USBx_VBUS MUST not connect directly to the 5V VBUS voltage of connector; Instead, this pin must be isloated with an external 30K 1% resistor.

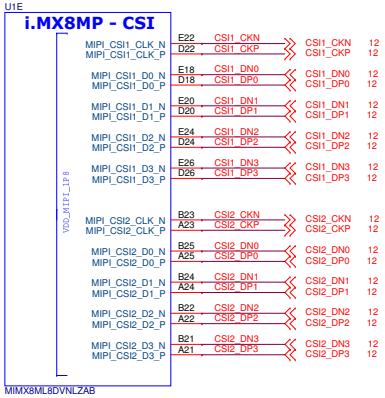


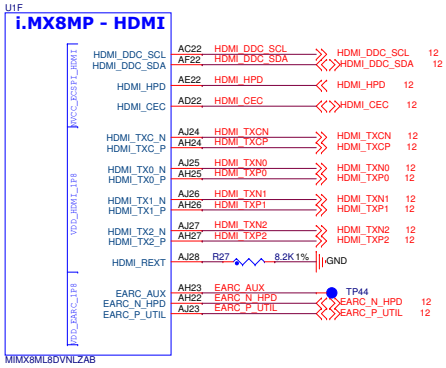


Note:

MIPI_TEST_DNU is for internal test, can be floating for normal use.







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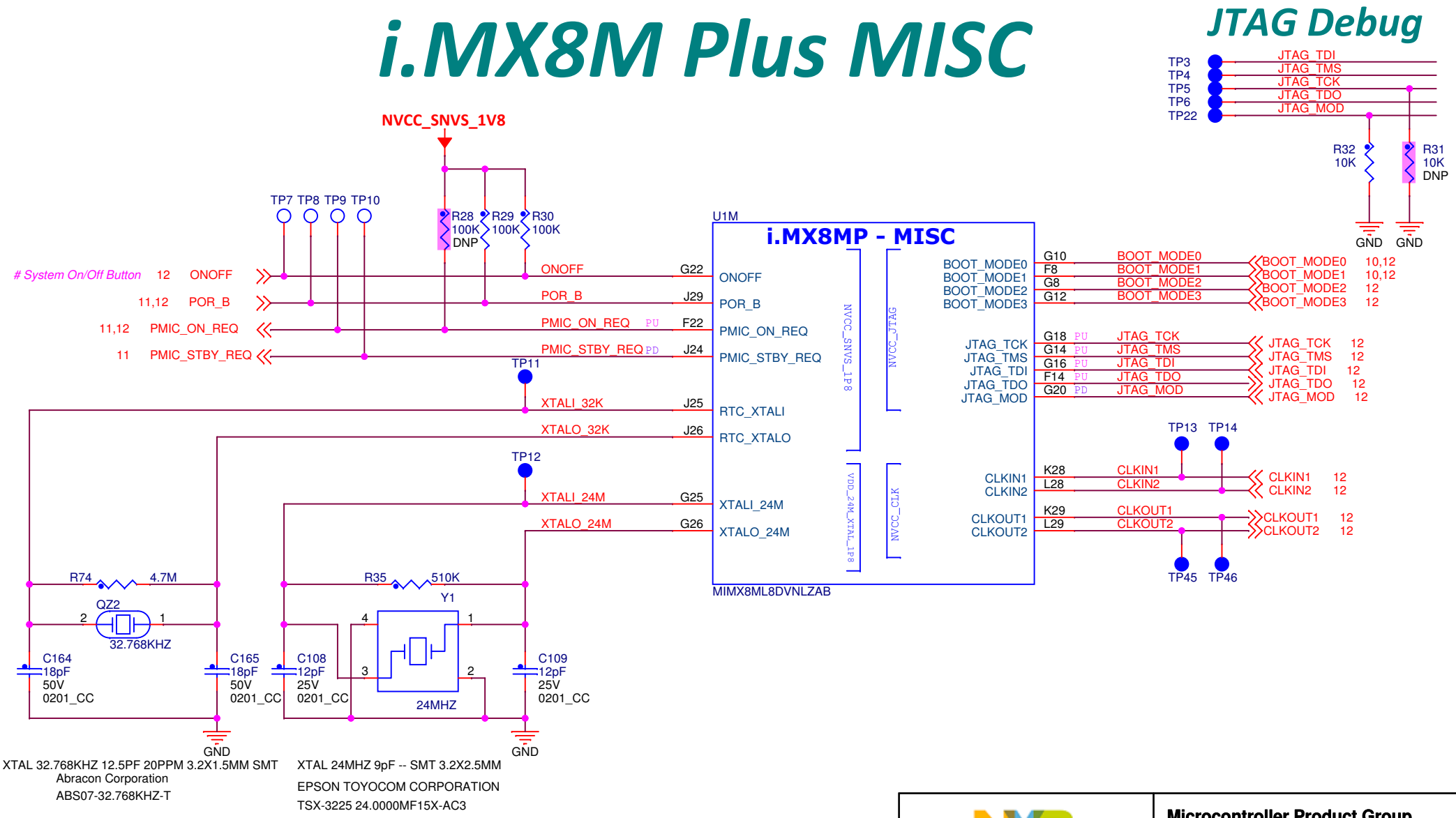
	Date: Wednesday, November 18, 2020	Sheet 7 of 12	

i.MX8M Plus MISC



XTAL 32.768KHZ 12.5PF 20PPM 3.2X1.5MM SMT
Abracon Corporation
ABS07-32.768KHZ-T

XTAL 24MHZ 9pF -- SMT 3.2X2.5MM
EPSON TOYOCOM CORPORATION
TSX-3225 24.0000MF15X-AC3

Caution:
BOOT_MODE0, BOOT_MODE1, BOOT_MODE2, BOOT_MODE3, JTAG_MOD and POR_B must be pulled to "111111" for i.MX8M Plus to enter Boundary Scan mode.

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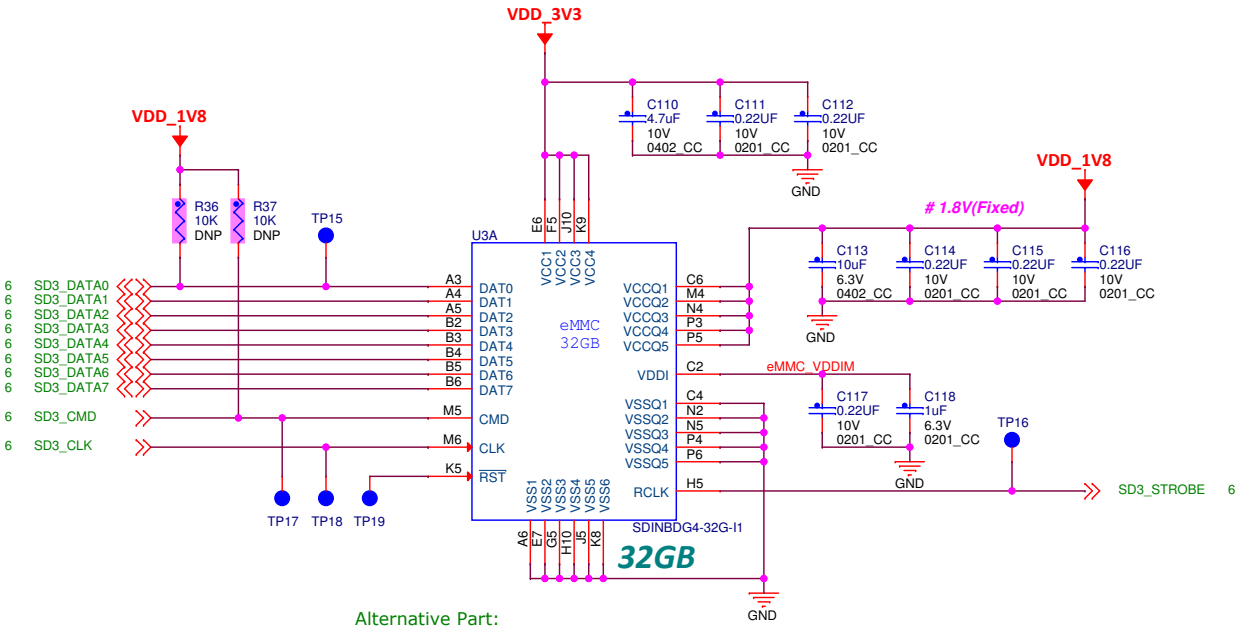
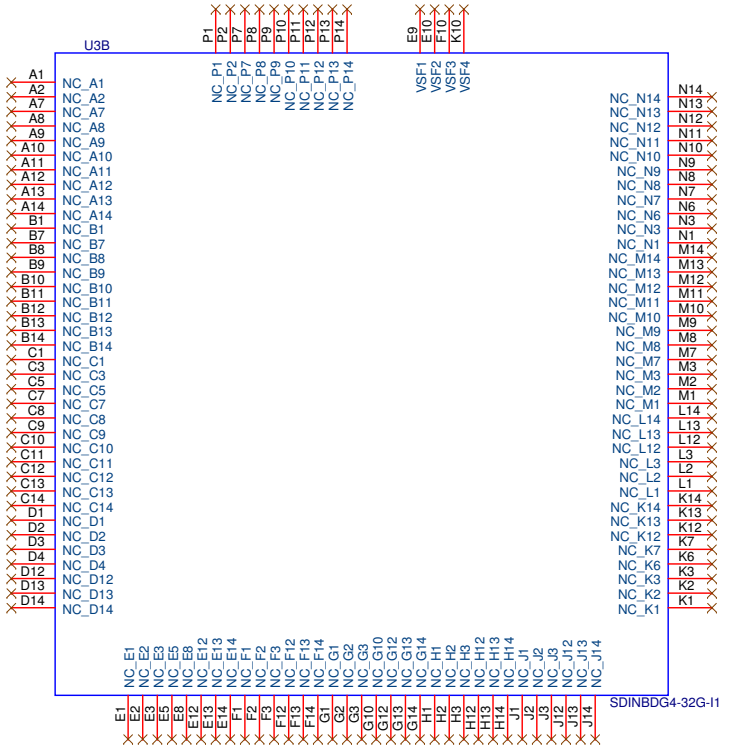
Storage

eMMC5.1

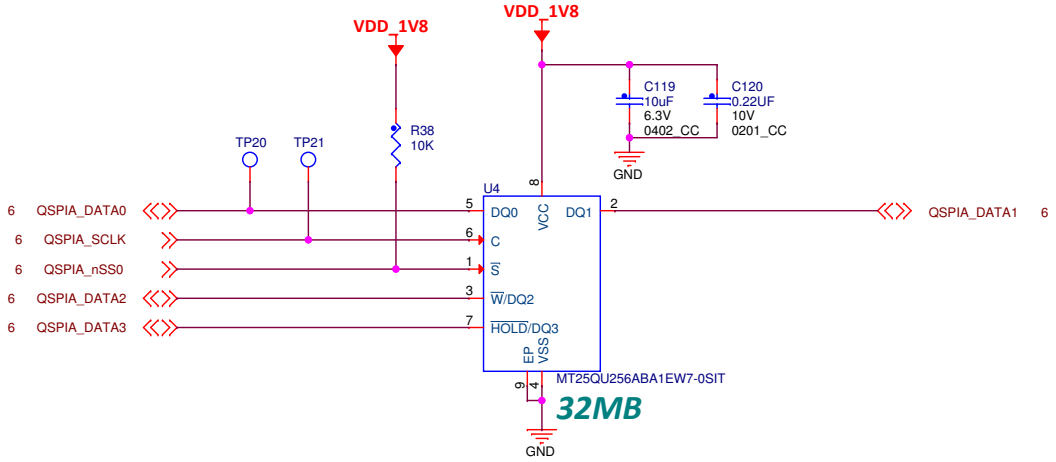


Alternative Part:

SDINBDA6-32G-I	Western Digital
EMMC32G-TB29-PZ90	Kingston



QSPI Flash



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Approved: <Approver>	Size B	Document Number SCH-46368 PDF: SPF-46368	Rev A3
	Date: Wednesday, November 18, 2020	Sheet 9 of 12	

Boot Mode and CFG Switch

i.MX8M Plus ROM Fuse

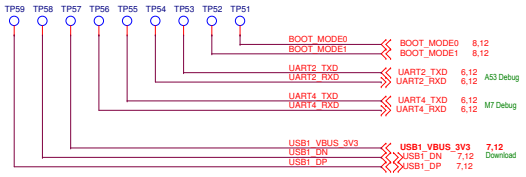
Full Line Address	Physical Address	7	6	5	4	3	2	1	0
0x470[15:0]	0x470[7:0]	OVERRIDE_NAND_PG_PER_BLK_VAL 00 - 32 pages 01 - 64 pages 10 - 128 pages 11 - 32 pages		OVERRIDE_FLEXSPI_BT_SEL 0 - Do not overriude 1 - Override	OVERRIDE_FLEXSPI_BT_SEL_VAL 00 - FlexSPI (Hyperflash 1.8V) 01 - FlexSPI (Flash with 4B READ(1x13 default supported) 10 - Default Octal mode (Micron, supported on 8QXP B0 already) 11 - Default Octal mode (Mxic, Nice to have)	FLEXSPI_AUTO_PROBE_EN 0 - Disable 1 - Enable	FLEXSPI_AUTO_PROBE_TYPE 00 - QuadSPI NOR 01 - MxicOctal 10 - MicronOctal 11 - AdestoOctal	
0x480[15:0]	0x480[7:0]	Reserved	FLEXSPI_DUMMY_CYCLE_SEL				FLEXSPI_FEQ_SEL 000 - 100 MHz 001 - 133 MHz 010 - 166 MHz 011 - 200 MHz 100 - 80 MHz 101 - 20 MHz		
0x480[31:16]	0x480[23:16]	NOC_ID_REMAP_BYPASS	ROM_NO_LOG if blown, ROM will not log event to log buffer	SDP_DISABLE Disable USB serial download	FORCE_BT_FROM_FUSE Boot from programmed fuses, not Boot Mode Pins	FLEXSPI_HOLD_TIME_SEL 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms		WDOG_TIMEOUT_SELECT 00 - 2.0s 01 - 1.5s 10 - 1.0s 11 - 0.5s	
0x490[15:0]	0x490[7:0]	USDHC_PWR_EN 0 - No power cycle 1 - Enabled via	EMMC_FAST_BT 0 - Regular 1 - Fast Boot	SDMMC_BUS_WIDTH 00 - 8-bit 01 - 4-bit 10 - 8-bit DDR (MMC 4.4) 11 - 4-bit DDR (MMC 4.4)	SD_SPEED: 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104	EMMC_SPEED: 00 - Normal 01 - High		USDHC_VOL_SEL For Normal Boot Mode IO Voltage 0 - 3.3V 1 - 1.8V	USDHC_MFG_VOL_SEL For Mfg Mode IO Voltage 0 - 3.3V 1 - 1.8V
0x490[31:16]	0x490[23:16]	RECOVERY_SDMMC_BOOT_DIS 0 - Enable 1 - Disable	IMG_CNTN_SET1_OFFSET				USDHC_PAD_SION_EN 0 - Disable 1 - Enable	BT_RDC_DISABLE	USDHC_DLL_EN 0 - Disable DLL for SD/eMMC 1 - Enable DLL for SD/eMMC
0x4A0[15:0]	0x4A0[7:0]	SD_CALI_STEP '00' - 1 TBD	USDHC_PWR_INTERVAL 00 - 20ms 01 - 10ms 10 - 5ms 11 - 2.5ms		USDHC_PWR_DELAY 0 - 5ms 1 - 2.5ms		USDHC_PWR_POLARITY 0 - Low 1 - High	USDHC_OVRD_PAD_SETTING_UP1	EMMC_FAST_BT_ACK 0 - Boot Ack Disabled 1 - Boot Ack Enabled
0x4A0[31:16]	0x4A0[23:16]	Reserved							
0x4B0[15:0]	0x4B0[7:0]	Reserved	NAND_GPMI_DDR_DLL_VAL (GPMI Read DDR DLL Target Value) 0000 - 7 0001 - 1 0111 - 0 1111 - 15					USB_SS_ENABLE	NAND_CS_NUM (Nand Number Of Devices) 00 - 1 01 - 2 10 - 4 11 - Reserved
0x4B0[31:16]	0x4B0[23:16]	Reserved	FlexSPI NAND Busy Bit Offset Override			FlexSPI NAND CS Interval 00-100ns 01-200ns 10-400ns 11-50ns		FlexSPI NAND Column Address Width 00-12 01-13 10-14 11-15	

Full Line Address	Physical Address	7	6	5	4	3	2	1	0
0x470[15:0]	0x470[15:8]	BOOT_MODE_FUSES BootRom will retrieve boot mode from these fuses instead of BOOT_MODE pins if * BOOT_MODE_PINS=0x0 or * BT_FUSE_SEL blown				OVERRIDE_USDHC_BT_SEL 0 - Do not override 1 - Override	OVERRIDE_USDHC_BT_SEL_VAL 00 - uSDHC1 SD 01 - uSDHC1 eMMC 10 - uSDHC2 eMMC 11 - uSDHC3 SD		OVERRIDE_NAND_PG_PER_BLK 0 - Do not override 1 - Override
0x480[15:0]	0x480[15:8]	BT_LPB (Core/DDR/Bus) '00'/'01' - LPB Disable '10' - Div by 2 '11' - Div by 4		BT_LPB_POLARITY (GPIO polarity)	ICACHE_DIS L1 I-Cache DISABLE	TZASC_EN	WDOG_EN '0' - Disabled '1' - Enabled	BT_FREQ_SEL (ARM/DDR) 0 - 800 / 800 MHz 1 - 400 / 400 MHz	DCACHE_DIS Disable L1 and L2 D-Cache
0x480[31:16]	0x480[31:24]	ECSPI_PORT_SEL 000 - eCSPI1 001 - eCSPI2 010 - eCSPI3		ECSPI_ADDR_SEL 0 - 3-bytes (24-bit) 1 - 2-bytes (16-bit)	ECSPI_CS_SEL(SPI only) 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3		RECOVER_ECSPI_BOOT_EN '0' - Disabled '1' - Enabled		DCACHE_BYPASS_DIS
0x490[15:0]	0x490[15:8]	USDHC_DLL_SEL 0 - DLL Slave Mode for 1 - DLL Override Mode	SDMMC_DLL_DLY[6:0] Delay target for USDHC DLL, it is applied to slave mode target delay or override mode target delay depends on DLL Override fuse bit value.						
0x490[31:16]	0x490[31:24]	USDHC_OVRD_PAD_SETTING_LOW8[7:0]							
0x4A0[15:0]	0x4A0[15:8]	BT_TOGGLE_MODE	NAND_FCB_SERCH_COUNT 00 - 2 01 - 2 10 - 4 11 - 8	NAND_TG_PREAMBLE_RD_LATENCY (Toggle Mode 33MHz Preamble Delay, Read Latency) '000' - 16 GPMICLK cycles. '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 3 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles. '1111' - 15 GPMICLK cycles				NAND_RST_TIME
0x4A0[31:16]	0x4A0[31:24]	NAND_OVERRIDE_PAD_SETTING[7:0]							
0x4B0[15:0]	0x4B0[15:8]	NAND_READ_RETRY_SEQ_ID[3:0] 0000 - don't use read retry(RR) sequence embedded in ROM 0001 - Micron 20nm RR sequence 0010 - Toshiba A19nm RR sequence 0011 - Toshiba 19nm RR sequence 0100 - SanDisk 19nm RR sequence 0101 - SanDisk 1ynmRR sequence 0110 - Hynix 20nm A Die RR sequence 0111 - Hynix 26nm RR sequence 1000 - Hynix 20nm B Die RR sequence 1001 - Hynix 20nm C Die RR sequence Others - Reserved				NAND_ROW_ADDR_BYTES 00 - 3 01 - 2 10 - 4 11 - 5		Reserved	Reserved
0x4B0[31:16]	0x4B0[31:24]	RNG_TRIM[7:0]							

i.MX8M Plus Boot Mode

BOOT_MODE3	BOOT_MODE2	BOOT_MODE1	BOOT_MODE0	Boot Modes
0	0	0	0	Boot From Internal Fuses
0	0	0	1	USB Serial Download
0	***0***	***1***	***0***	***USDHC3 (eMMC boot only, SD3 8-bit) Default***
0	0	1	1	USDHC2 (SD boot only, SD2)
0	1	0	0	NAND 8-bit single device 256 page
0	1	0	1	NAND 8-bit single device 512 page
0	1	1	0	QSPI 3B Read
0	1	1	1	QSPI Hyperflash 3.3V
1	0	0	0	ecSPI Boot
1	0	0	1	Reserved
1	0	1	0	FLEXSPI Serial NAND 2k page
1	0	1	1	FLEXSPI Serial NAND 4k page
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Manufacturing Test



BOOT_MODE1	BOOT_MODE0	Boot Modes
1	***0***	***USDHC3 (eMMC boot only, SD3 8-bit)***
0	1	USB Serial Download

Microcontroller Product Group
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ICAP Classification: CP: IUO: X PUBI:

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Drawn by: Frank Liu	Page Title: BOOT_CFG		
Approved: <Approver>	Size A2	Document Number SCH-46368 PDF: SPF-46368	Rev A3
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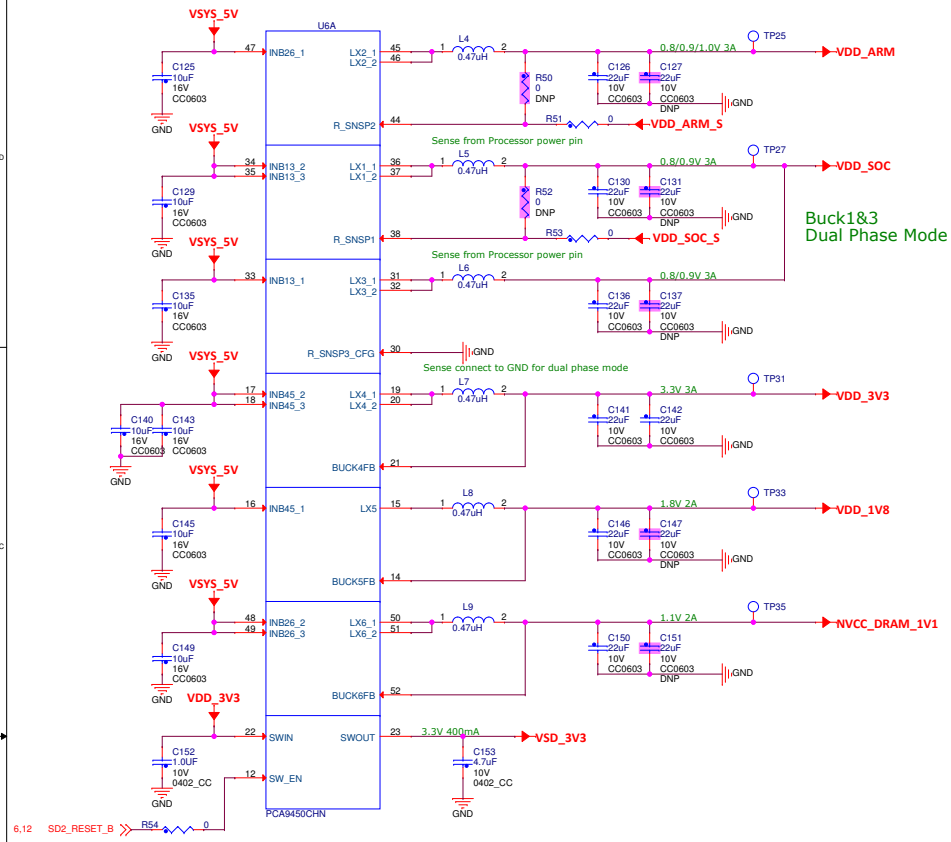
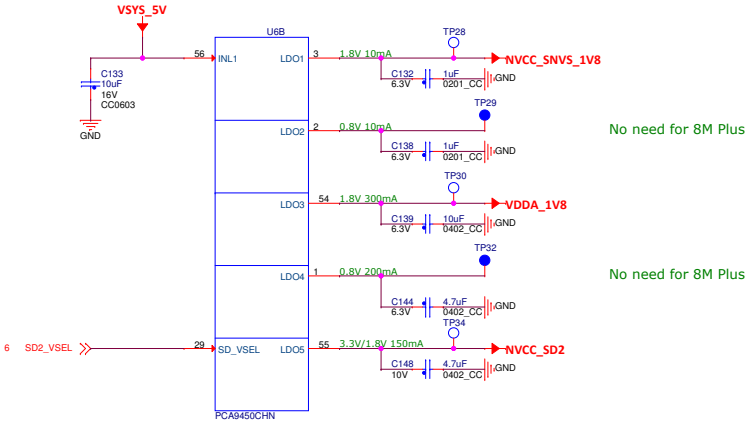
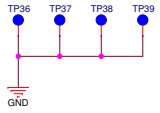
SYS PMIC

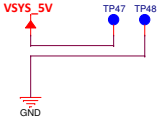


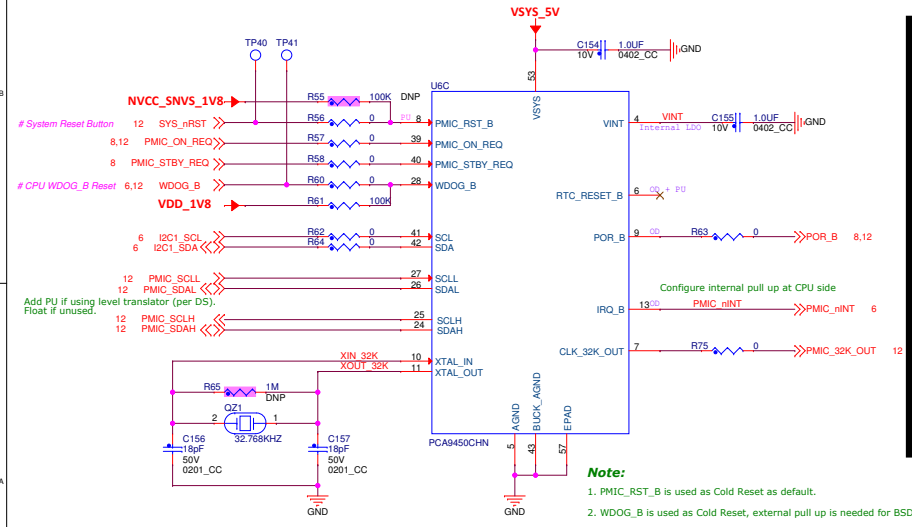


GND Testpoints



Backup PWR Supply





Note:

1. PMIC_RST_B is used as Cold Reset as default.
2. WDOG_B is used as Cold Reset, external pull up is needed for BSDL mode.

i.MX8M Plus LPDDR4 EVK Power Sequence and Operating Range

SEQ	PWR/Signal	REG	MIN	TYP	MAX	Max Current(mA)
1	NVCC_SNVS_1V8	LDO1	1.71	1.8	1.95	10
2	32K_INTERNAL	RTC_CLK	--	--	--	--
3	VDD_SOC	BUCK1/3	0.805/0.9	0.85/0.95	0.9/1.0	6000
4	VDD_ARM	BUCK2	0.805/0.9/0.95	0.85/0.95/1.0	0.9/1.0/1.05	3000
5	VDDA_1V8	LDO3	1.71	1.8	1.89	300
6	VDD_1V8/NVCC_xxx	BUCK5	1.65	1.8	1.95	2000
7	NVCC_DRAM_1V1	BUCK6	1.045	1.1	1.155	2000
8	VDD_3V3/NVCC_xxx	BUCK4	3	3.3	3.6	3000
8	VSD_3V3	MUXSW	3	3.3	3.6	400
9	NVCC_SD2	LDO5	3.0/1.65	3.3/1.8	3.6/1.95	150
10	POR_B	POR_B	--	--	--	--

ICAP Classification: CP: IUO: X PUBI:

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Drawn by: Frank Liu	Page Title: PMIC		
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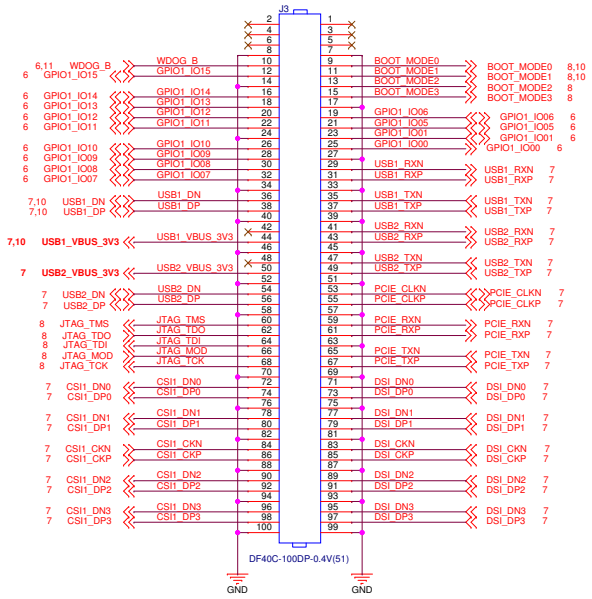
B2B Connector for CPU Board

Header



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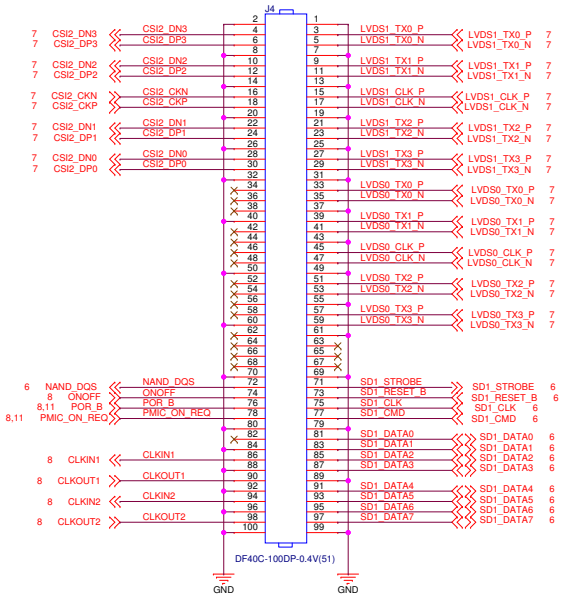

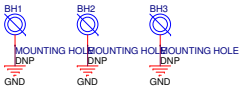

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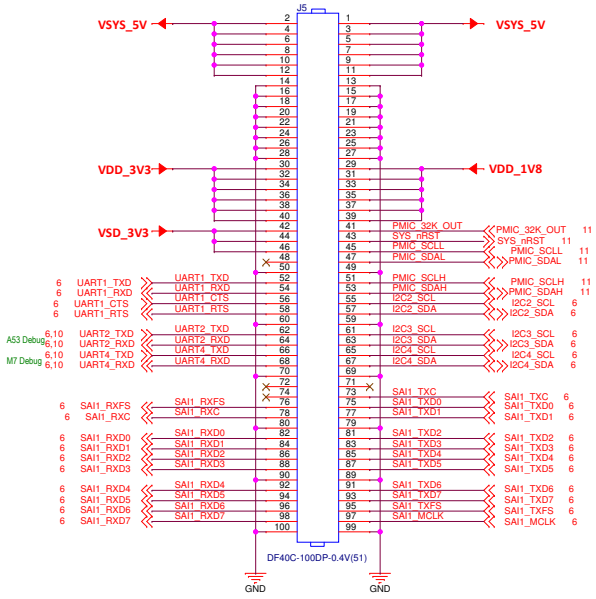

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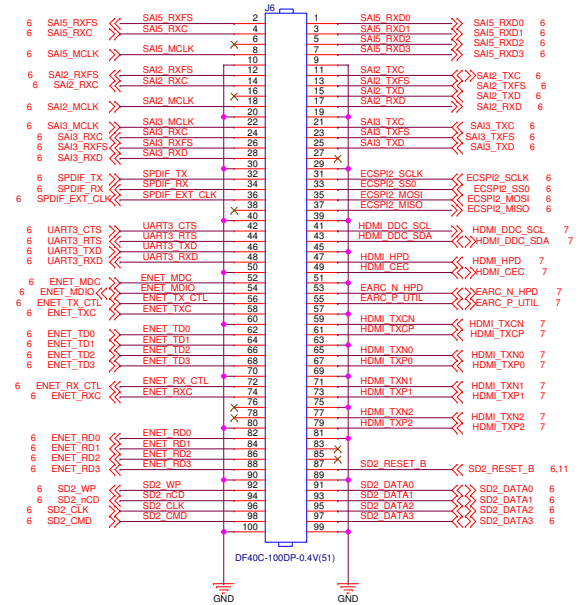

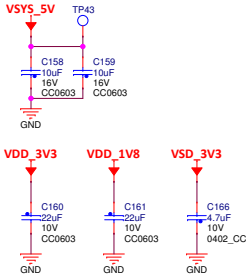

ICAP Classification: CP: IUO: A PUBI:

Designer: Frank Liu	Drawing Title: **8MPLUSLPD4-CPU**	
Drawn by: Frank Liu	Page Title: **SOM Interface**	
Approved: <Approver>	Size: C	Document Number: SCH-46368 PDF: SPF-46368 — Rev: A3
	Date: Wednesday, November 18, 2020	Sheet 12 of 12