C290PCIe-RDB

Version Control

Version	Date	Modifications
V0.1	2012/09	First release of Schematics
V0.2	2012/10	update C293 symbol, change GE phy to VSC8641, add I2C boot EEPROM
V0.3	2012/10	update POR strappings
V0.4	2012/10	1. Change DDR3 to 3 x16 chips. Page 4-6 2. Add FBANK_SEL2 to NOR Flash, change NOR Flash MPN to S29GL512P11TFI0. Page 8 3. Add pull-up resistor to PIN10 of NAND Flash. Page 8 4. Add pull-up resistor to TSEC1_GTX_CLK for cfg_60x in P1010 interposer. Page 8 5. Correct net name errors of "GE2_CMODEx". Page 13 6. Remove UART1 signals and RJ45 connector. Page 15/16 7. Change POR-ON strappings with connect to switchs and CPLD. Page 18/22 8. Connect MGN signal to CPLD and switch to change VCORE voltage. Page 24 9. Change heatsink to S06QZZ0B. Page 28
V0.5	2012/11	1. Swap DDR3 data bus order for layout. Page 4/5/6 2. Change switch pull-up pull-down resistors to same side. Page 18 3. Add sw_cfg_rom_loc[0:3] from switch to CPLD. Page 18/22
V0.6	2012/11	1. Swap CPLD pins for layout. Page 22 2. Reduce power decoupling caps of C293. Page 20
V0.7	2012/11	1. Generate SOC MVREF use voltage divider. Page 3 2. Delete 4.7pF cap on DDR3 clock pair. Page 3 3. Delete optional pull down resistor for TMP_DETECT_B. Page 15
V0.8	2012/11	1. Add a 0603 cap to 1V0_CB. Page 20 2. Add several caps acrossing plane splits. Page 28
V0.9	2012/12	1. Add a 1000pF cap between ZL_VSEN_P and ZL_VSEN_N. Page 24 2. Change U34 to SOT23-5 footprint and connect NC pin to GND. Page 25
V1.0	2013/02	update BOM
V1.1	2013/02	1. Change NAND Flash R/B to CPLD, then CPLD to C293 R/B0 and R/B1. Page 7/8/22 2. Add a 0.01uF cap to PEX_RST_N. Page 10 3. Change panel LED to single color. Page 22
V2.0	2013/08	Add 6pin ATX 6pin power connector, remove PTC and common mode chock Page 25
V2.1	2013/10	Add notes for serdes power and nand flash stuff R248, R275, R299,
V3.0	2013/12	Add 1.0V LDO for SVDD

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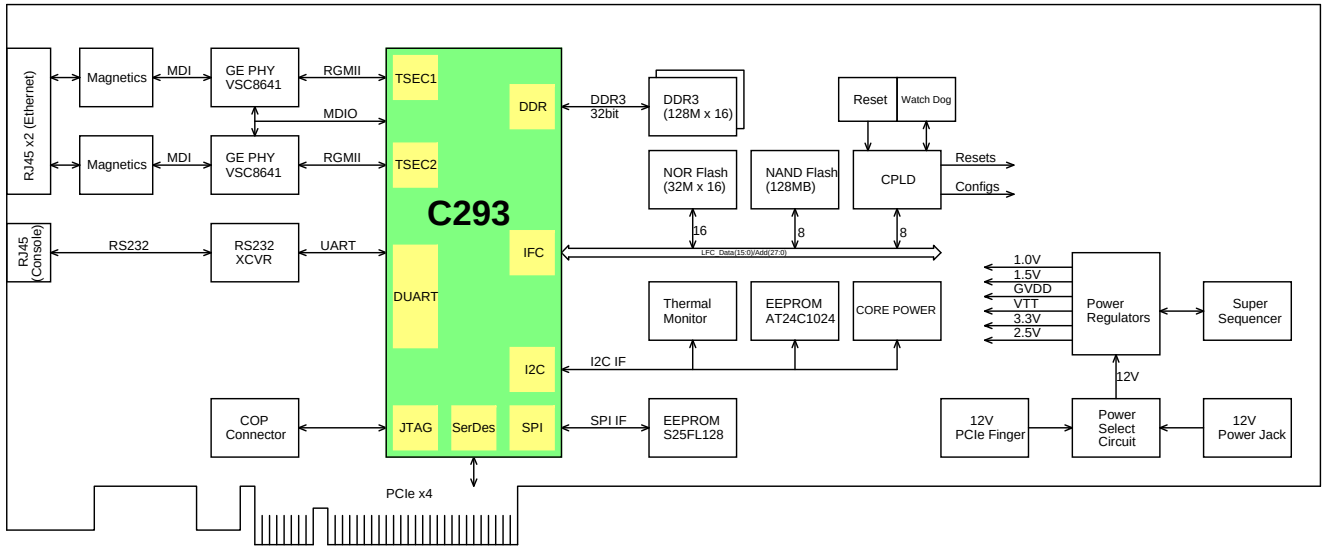
Size: B	Document Number: <Doc>	Design Engineer: *MICETEK*	Rev: A
Date: Tuesday, January 07, 2014		Sheet 1 of 28	

SYSTEM BLOCK DIAGRAM



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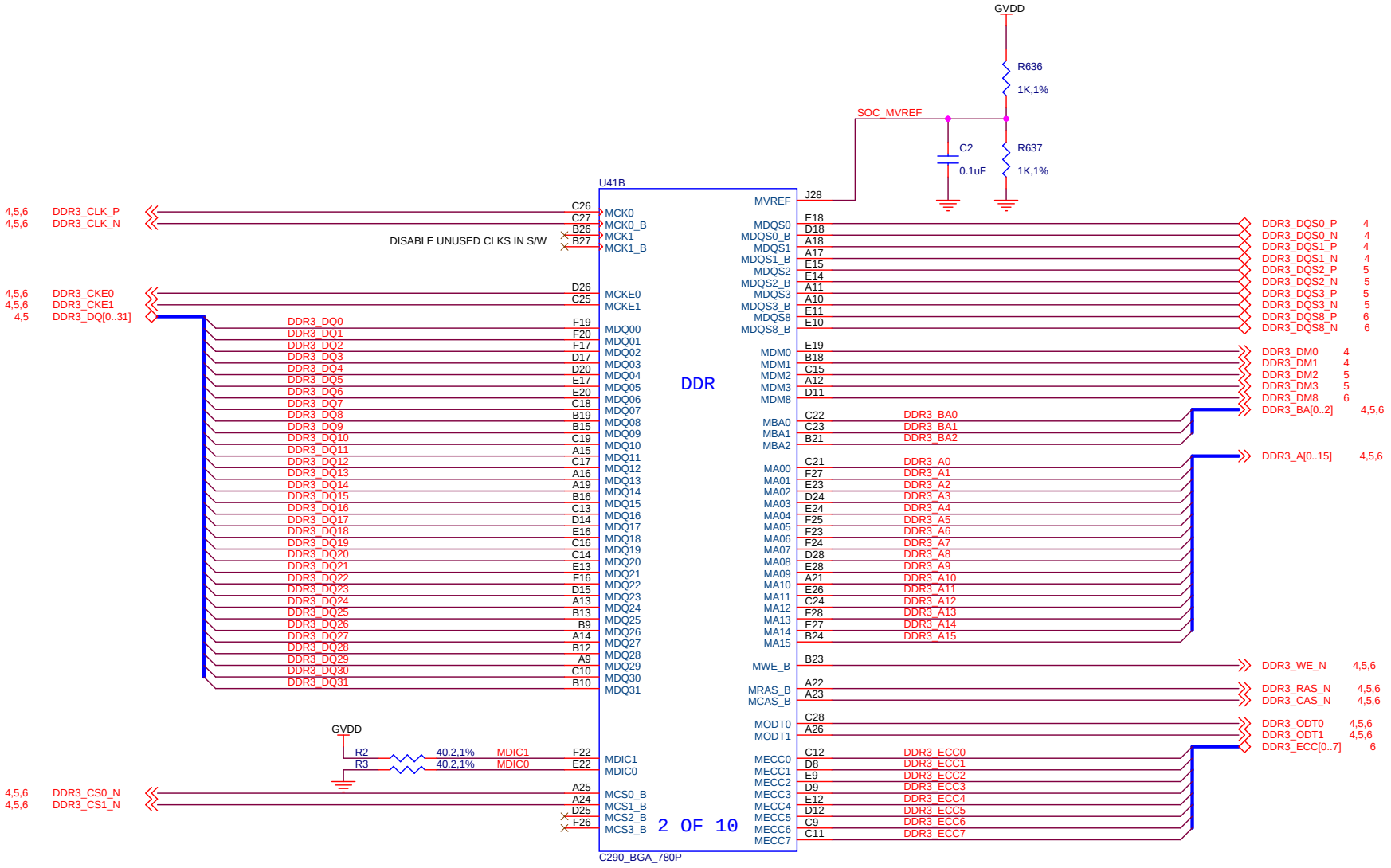
Date: Tuesday, January 07, 2014		Sheet 2 of 28	

C293 DDR3/DDR3L MEMORY INTERFACE



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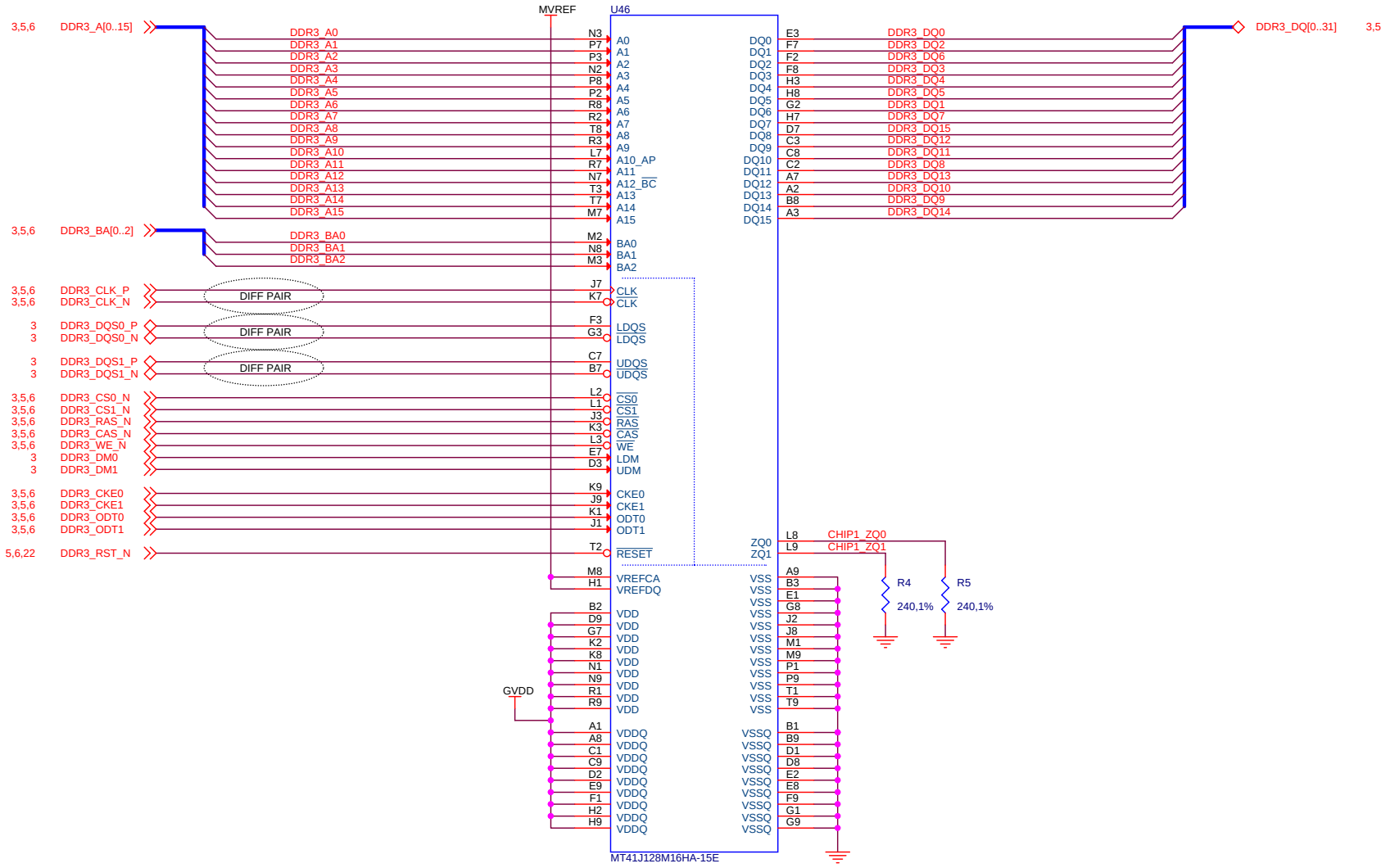
Date: Tuesday, January 07, 2014		Sheet 3 of 28	

DDR3/DDR3L MEMORY CHIP 1



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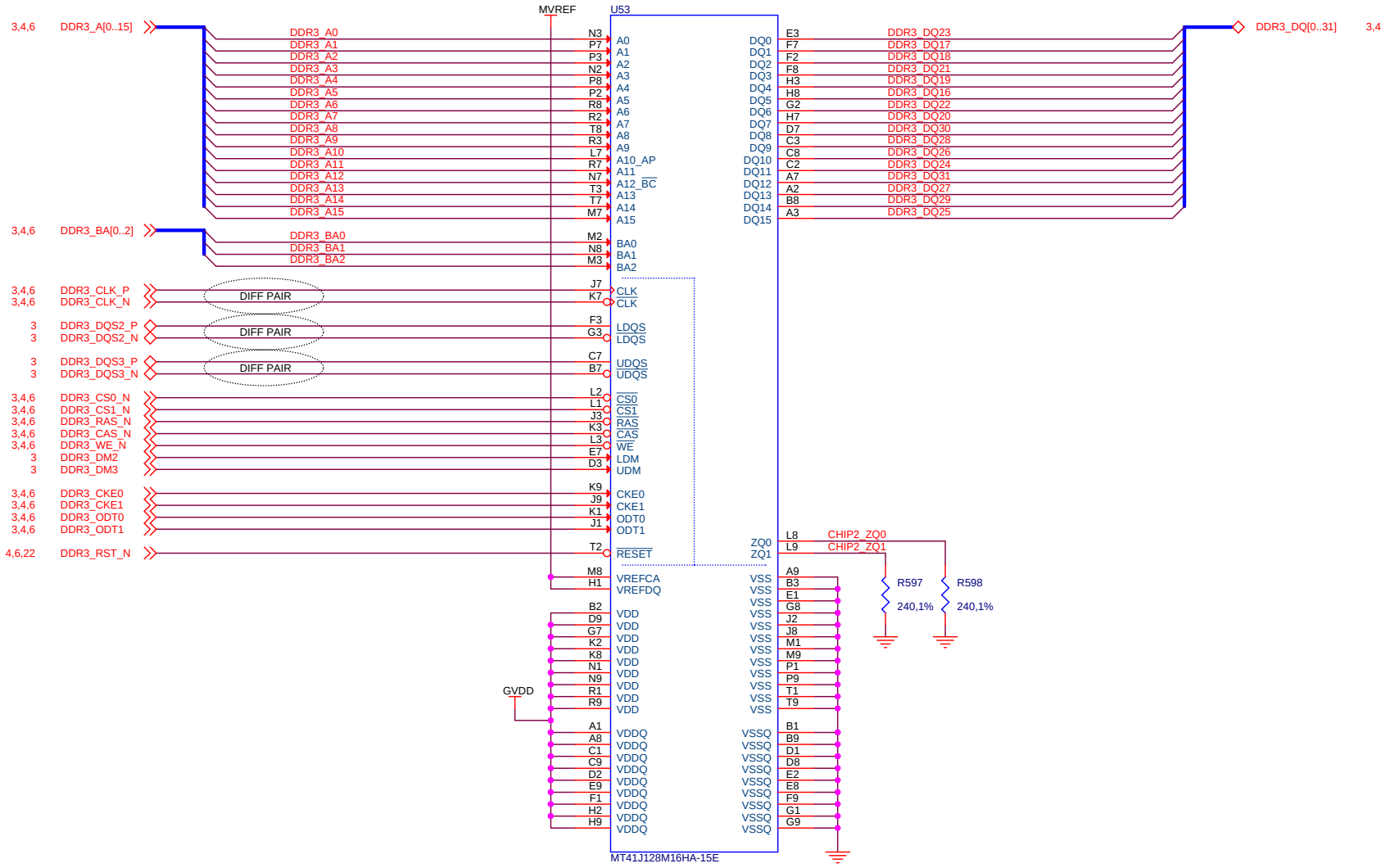
Date: Tuesday, January 07, 2014		Sheet 4 of 28	

DDR3/DDR3L MEMORY CHIP 2



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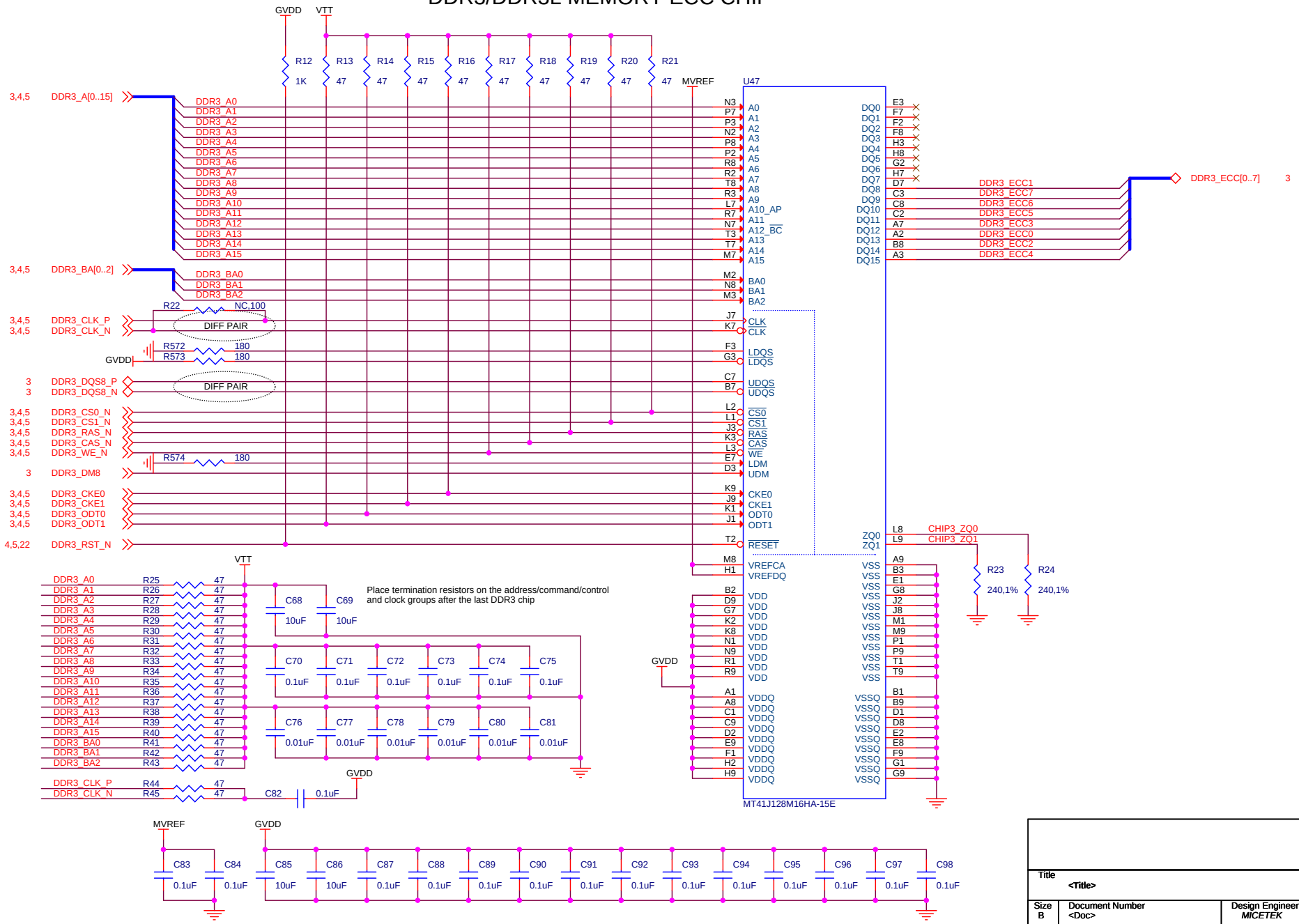
Date: Tuesday, January 07, 2014		Sheet 5 of 28	

DDR3/DDR3L MEMORY ECC CHIP



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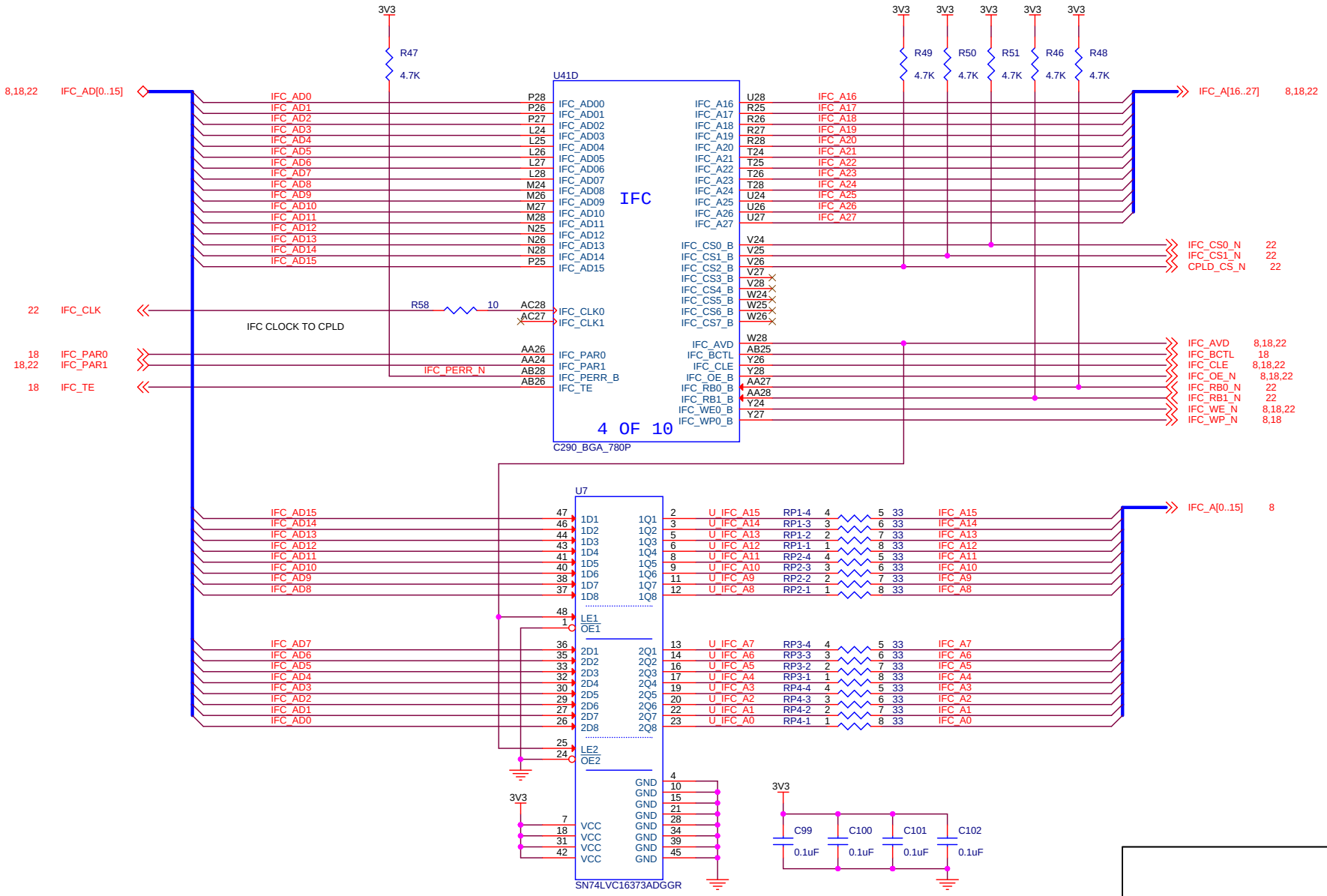
C293 IFC INTERFACE



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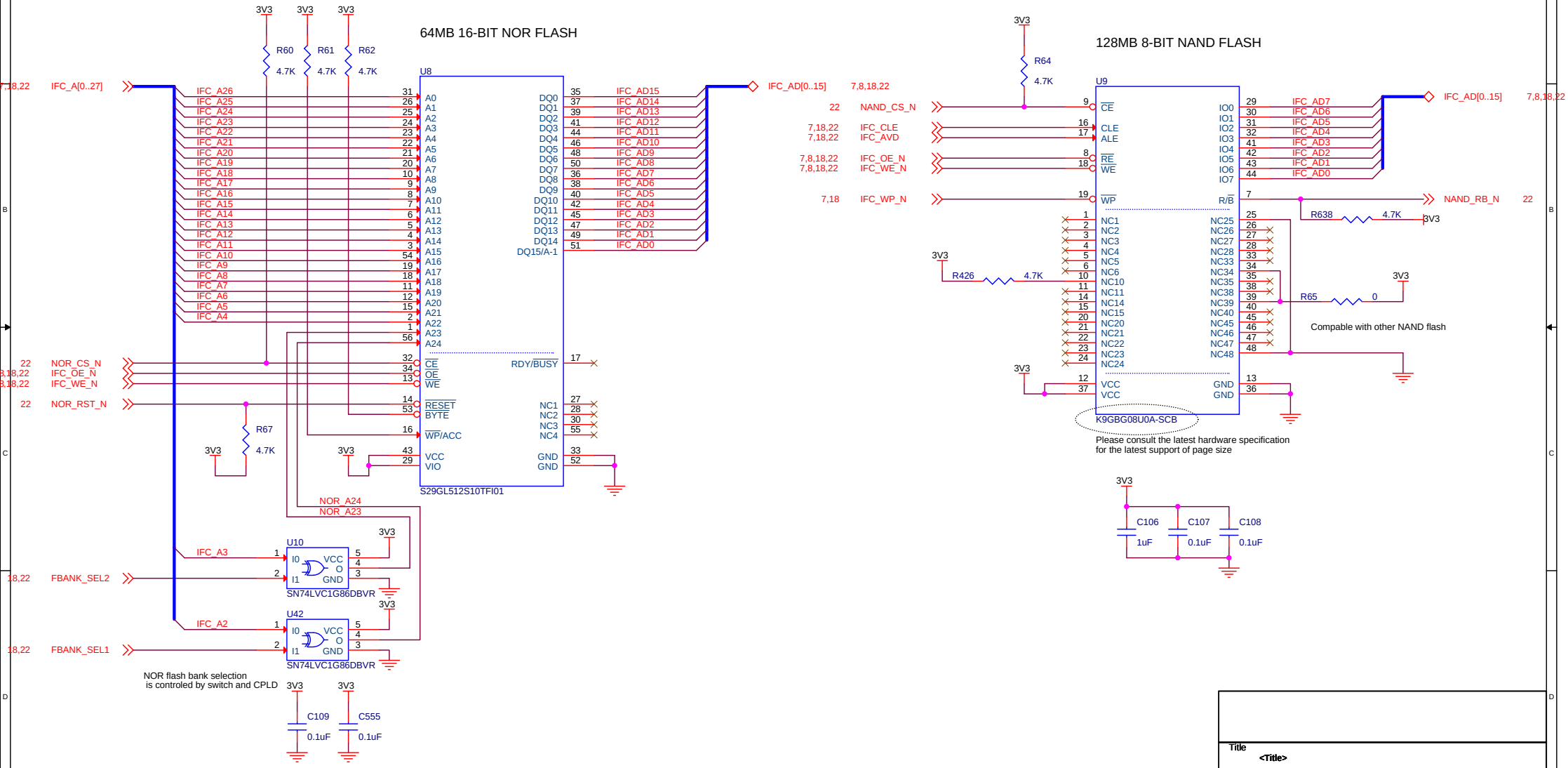
NOR FLASH and NAND FLASH MEMORY



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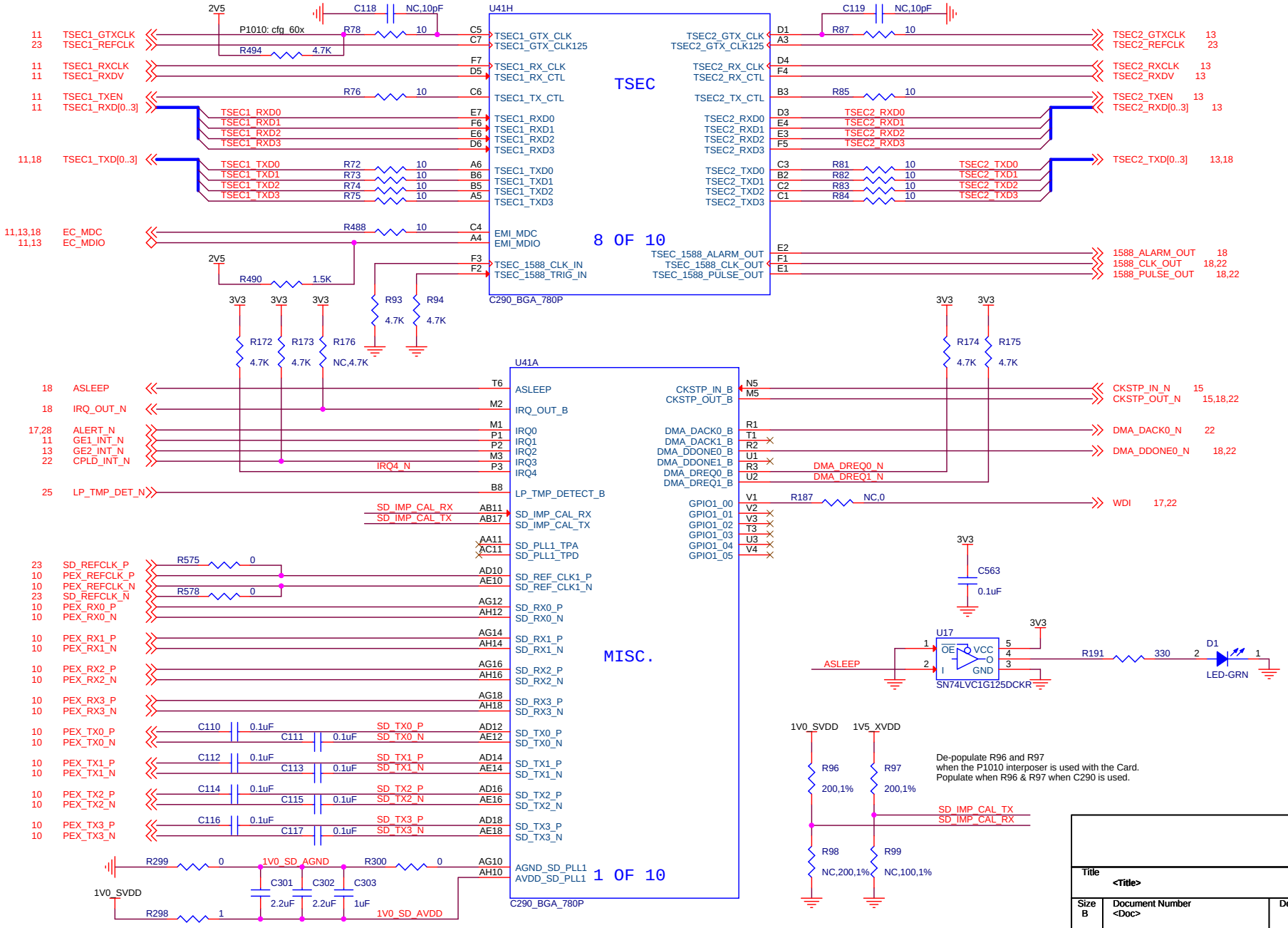
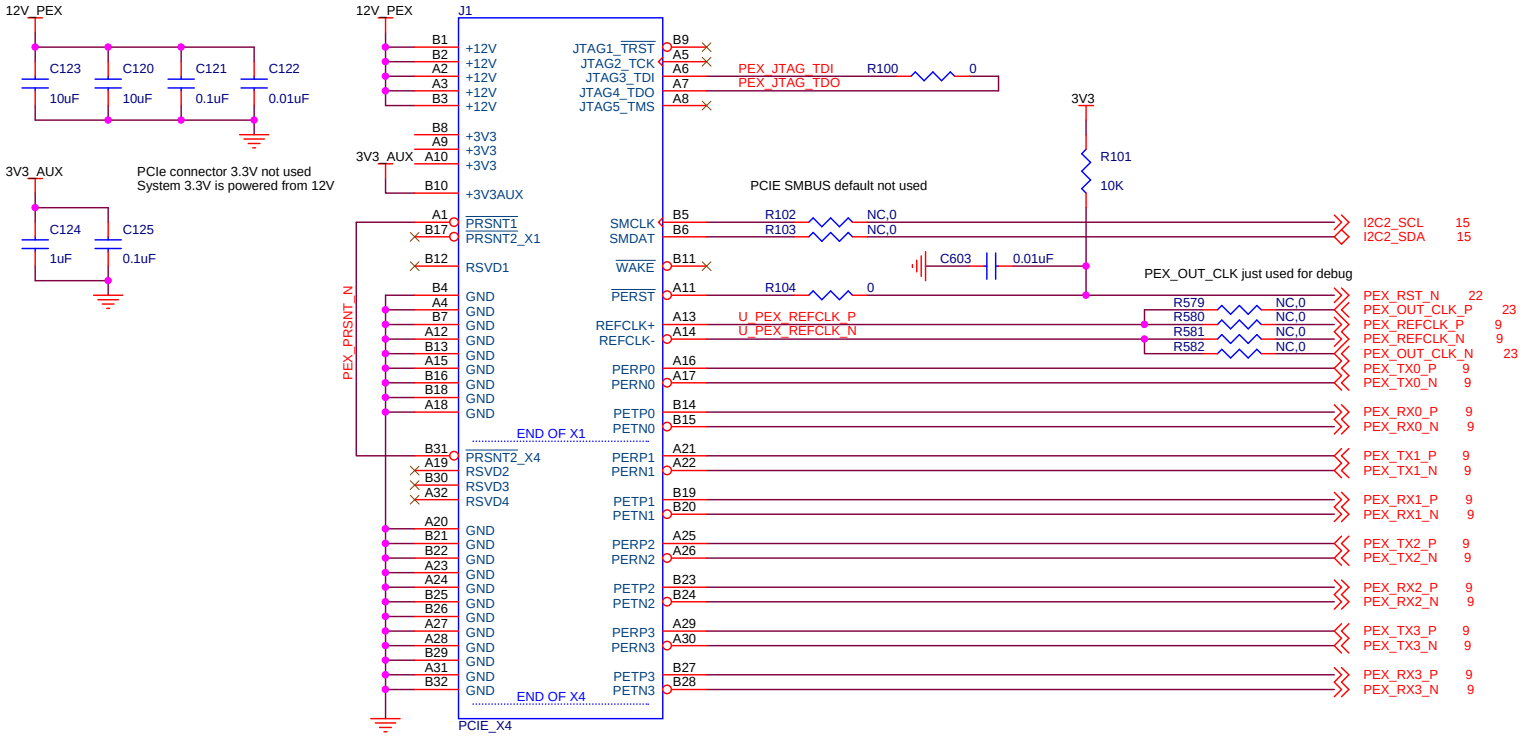
Date: Tuesday, January 07, 2014		Sheet 8 of 28	

C293 SERDES and TSEC 1&2 INTERFACE



PCI EXPRESS X4 INTERFACE



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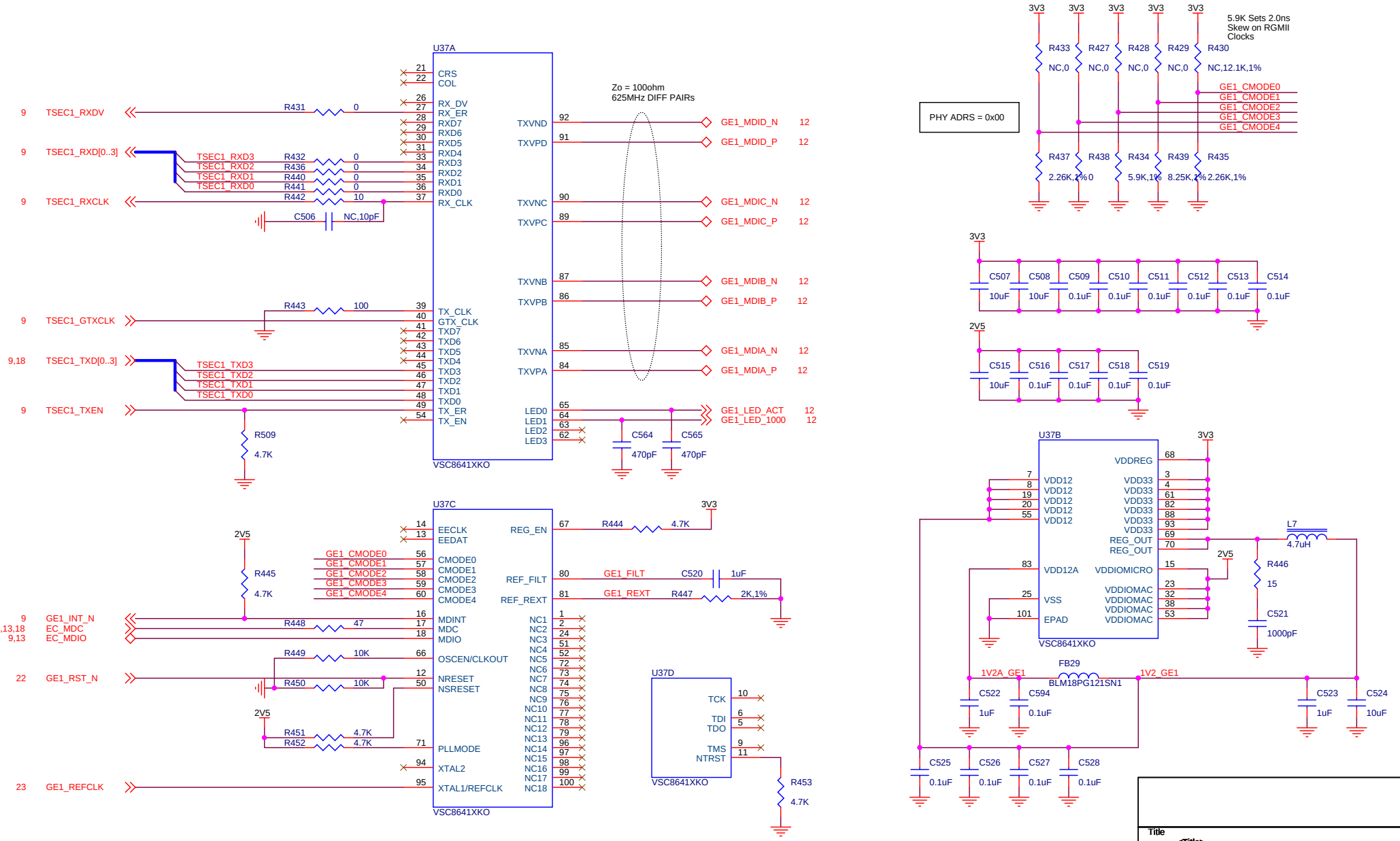
10/100/1000 ETHERNET PHY (PORT 1)



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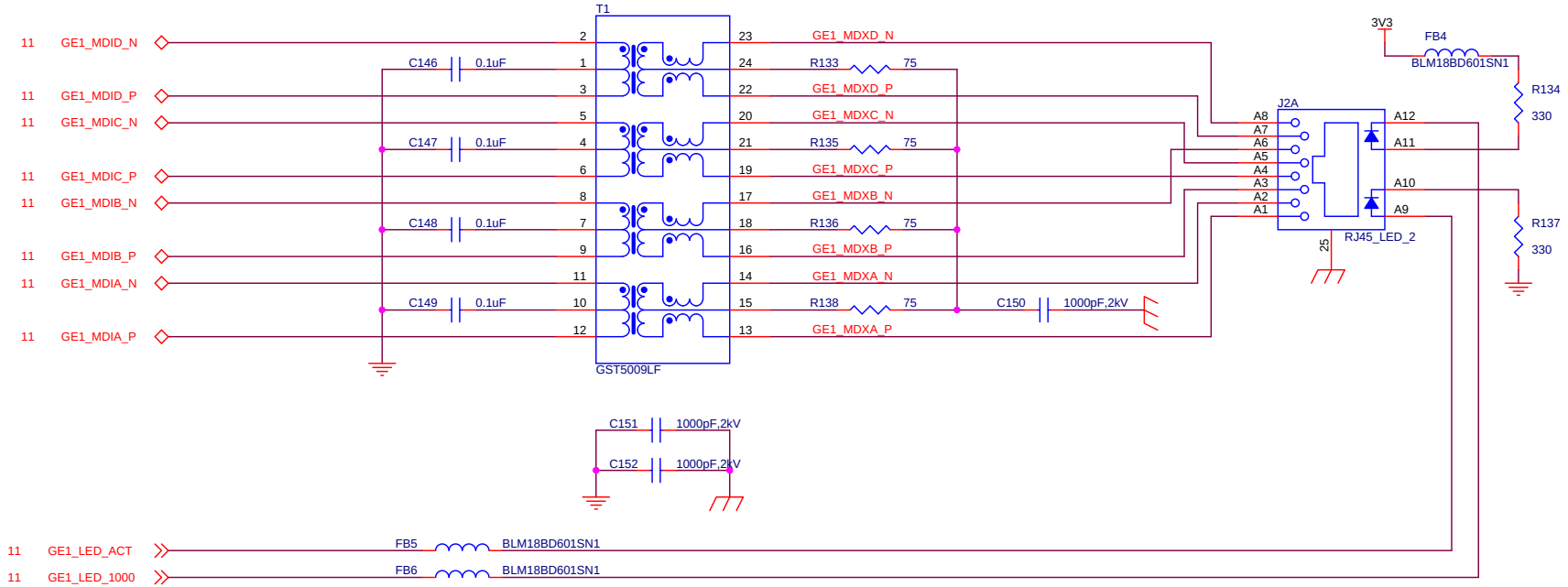
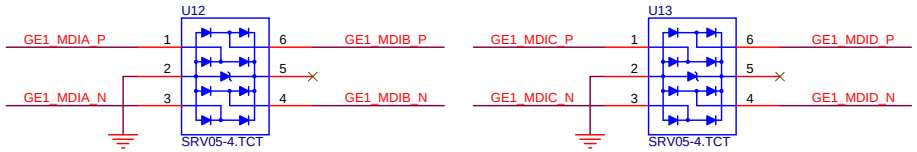
Date: Tuesday, January 07, 2014		Sheet 11 of 28	

10/100/1000 ETHERNET MAGNETICS and RJ45 CONNECTOR (PORT 1)



For Gigabit Ethernet protection, place close to magnetics



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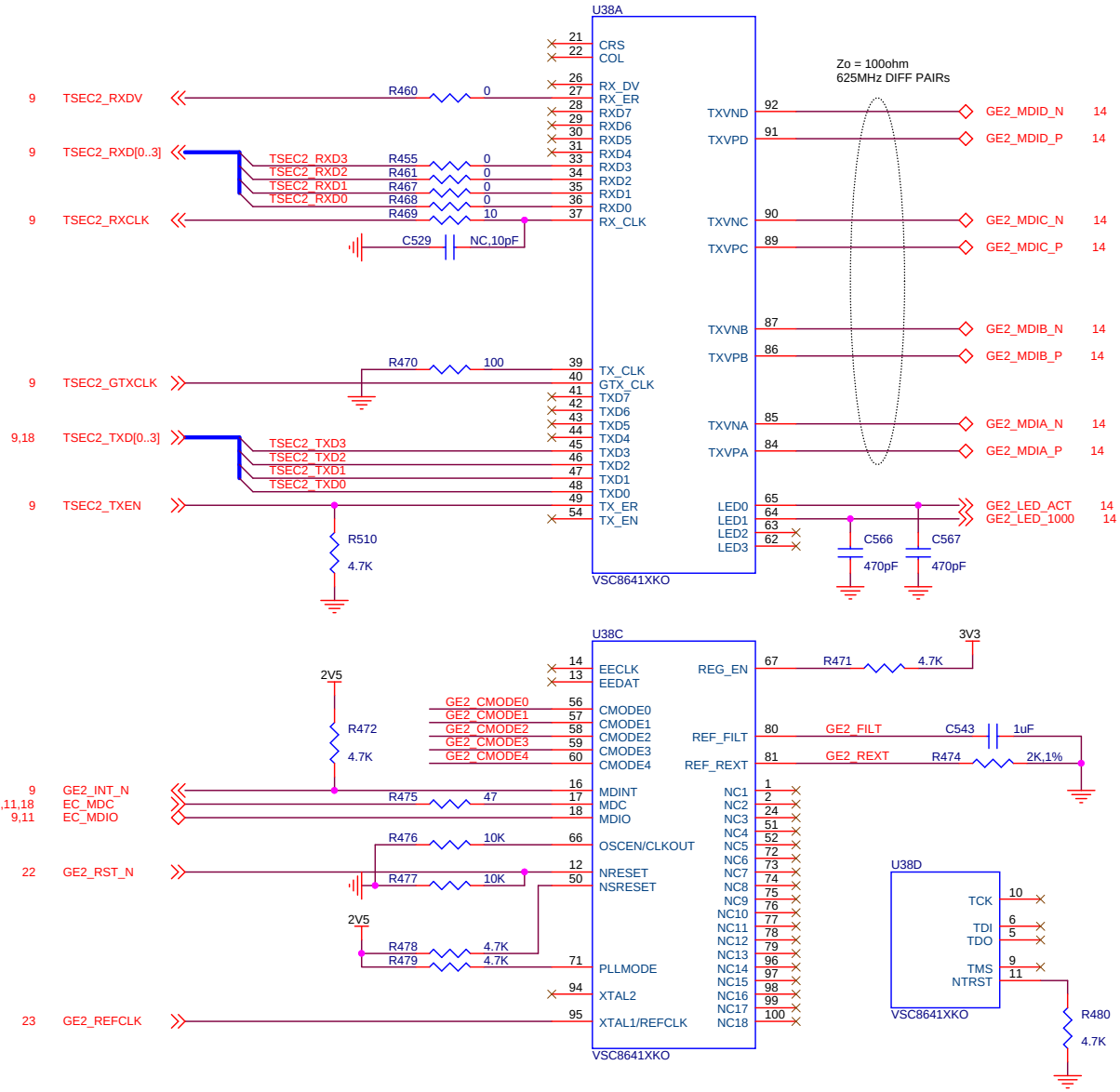
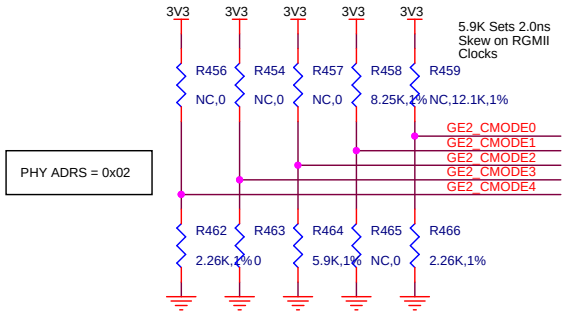
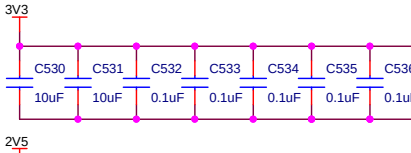
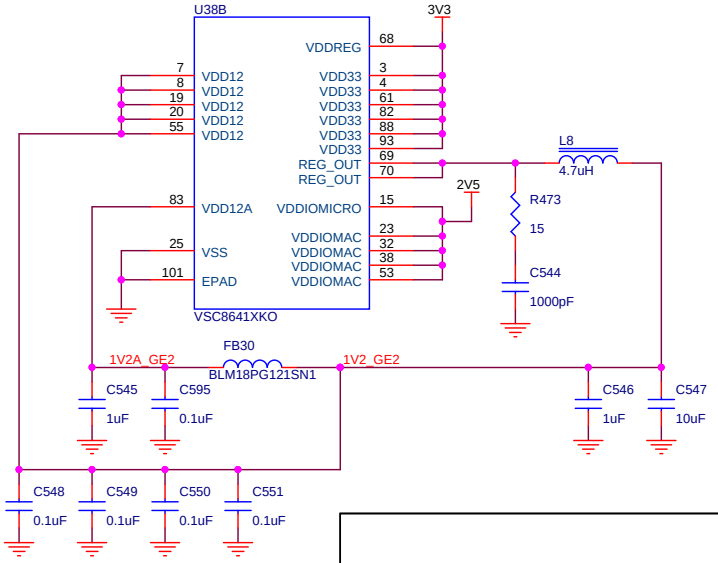
Date: Tuesday, January 07, 2014		Sheet 12 of 28	

10/100/1000 ETHERNET PHY (PORT 2)









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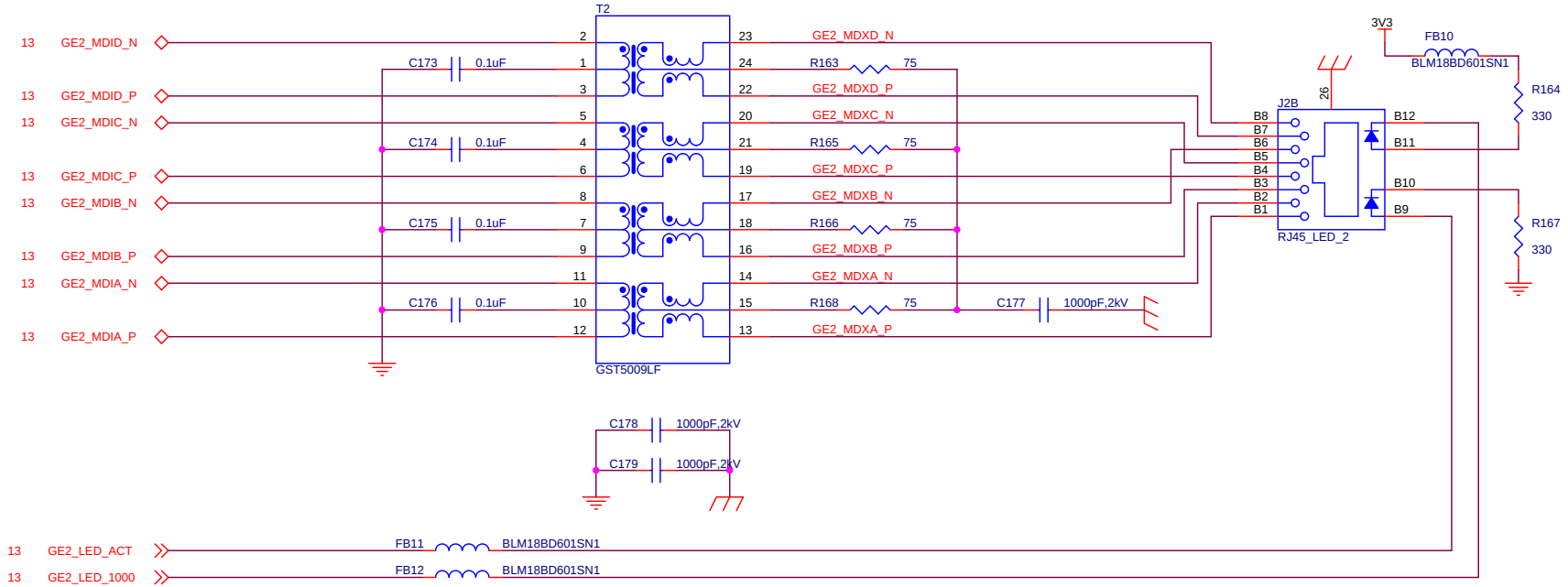
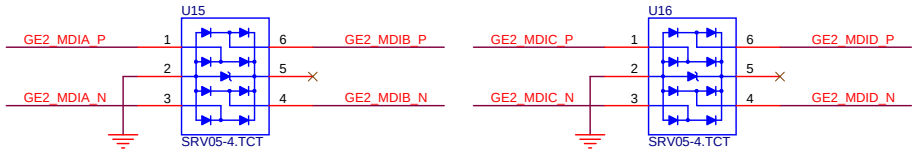
10/100/1000 ETHERNET MAGNETICS and RJ45 CONNECTOR (PORT 2)



For Gigabit Ethernet protection, place close to magnetics



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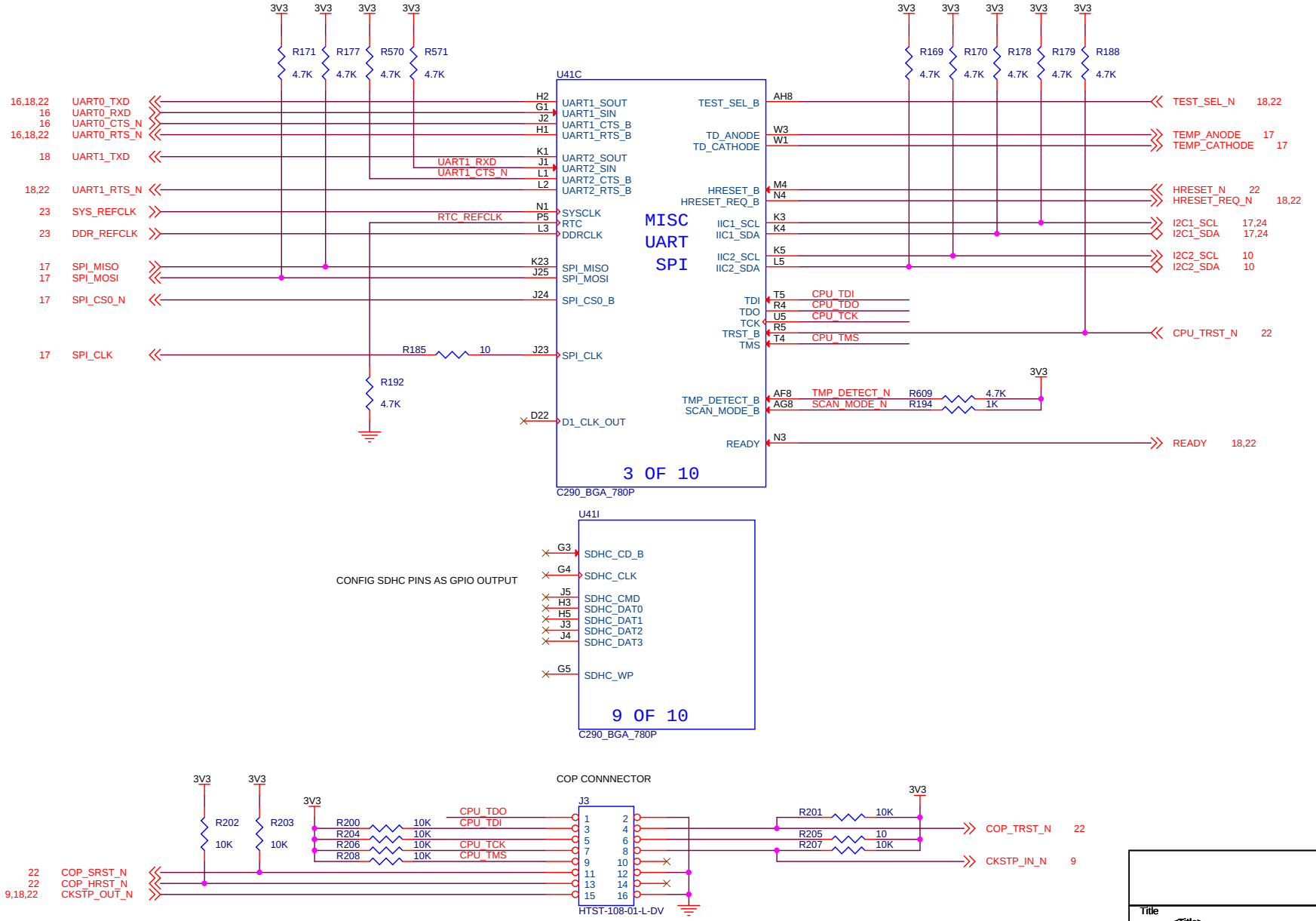
Date: Tuesday, January 07, 2014		Sheet 14 of 28	

C293 MISC



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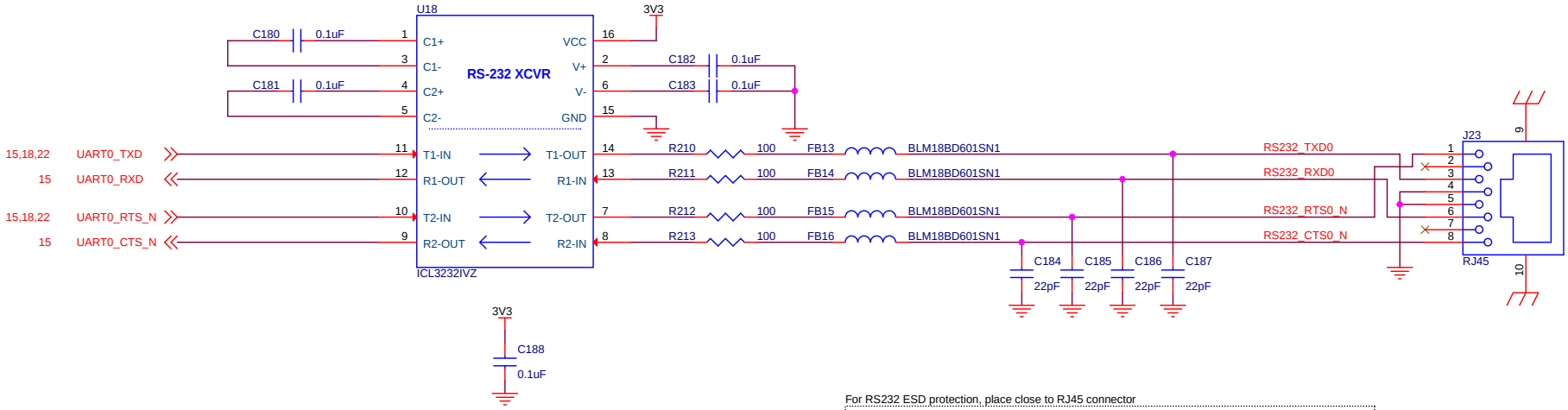
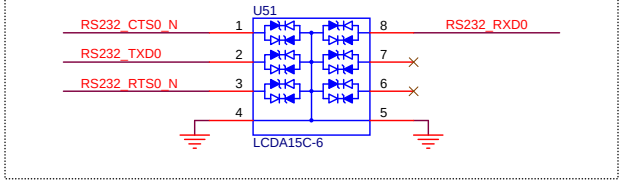
Date: Tuesday, January 07, 2014		Sheet 15 of 28	

DUART INTERFACE



For RS232 ESD protection, place close to RJ45 connector



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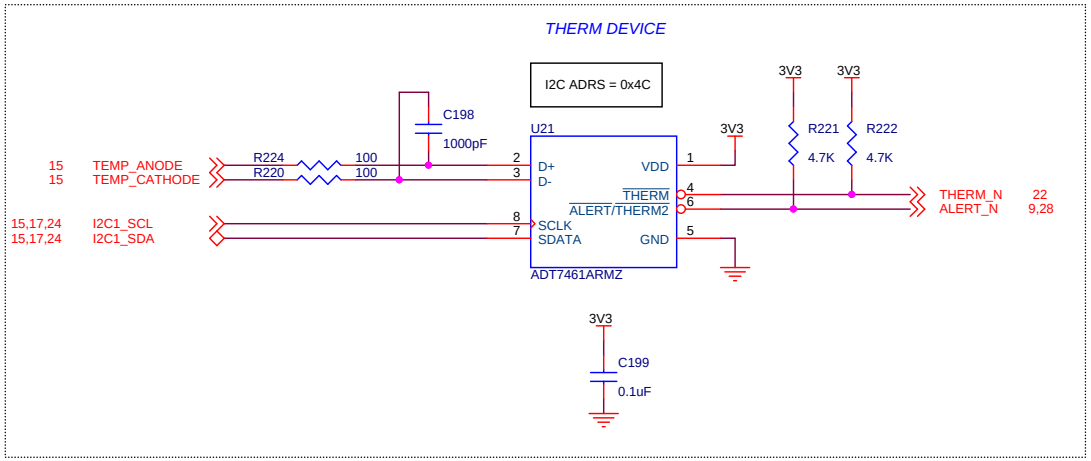
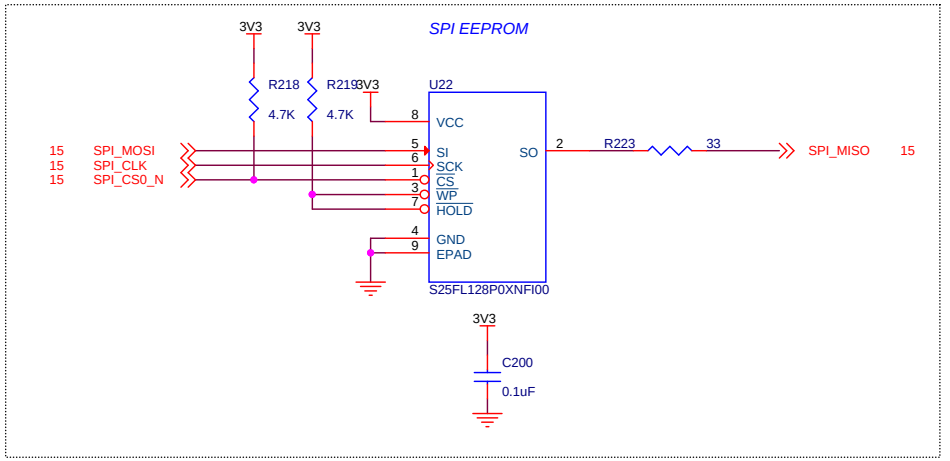
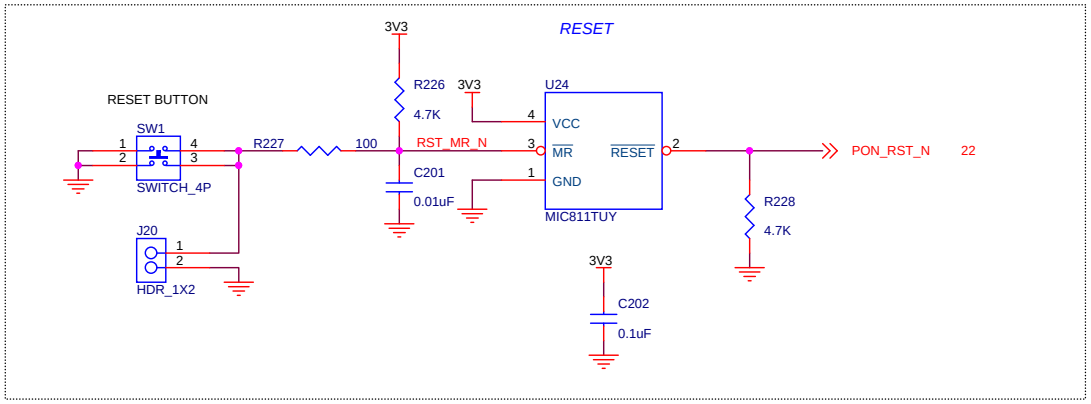
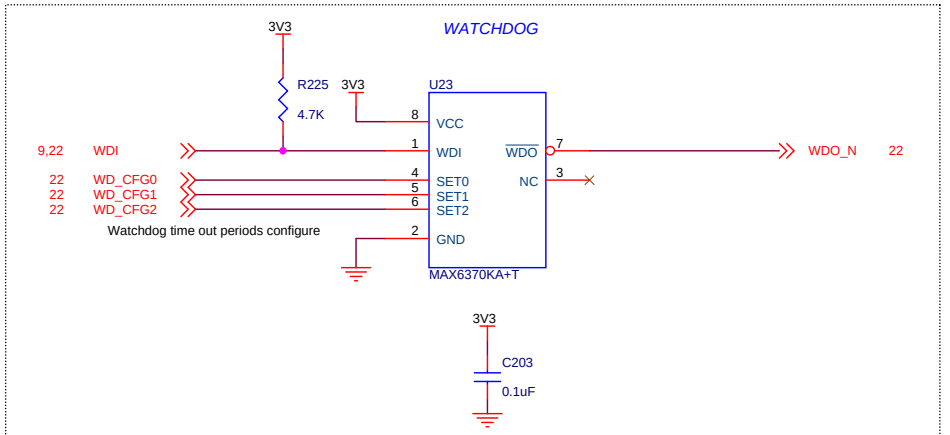
Date: Tuesday, January 07, 2014		Sheet 16 of 28	

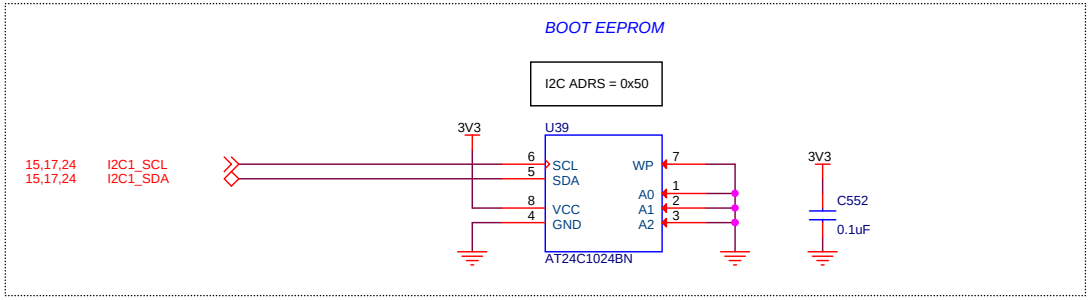
I2C&SPI DEVICE, RESET and WATCHDOG











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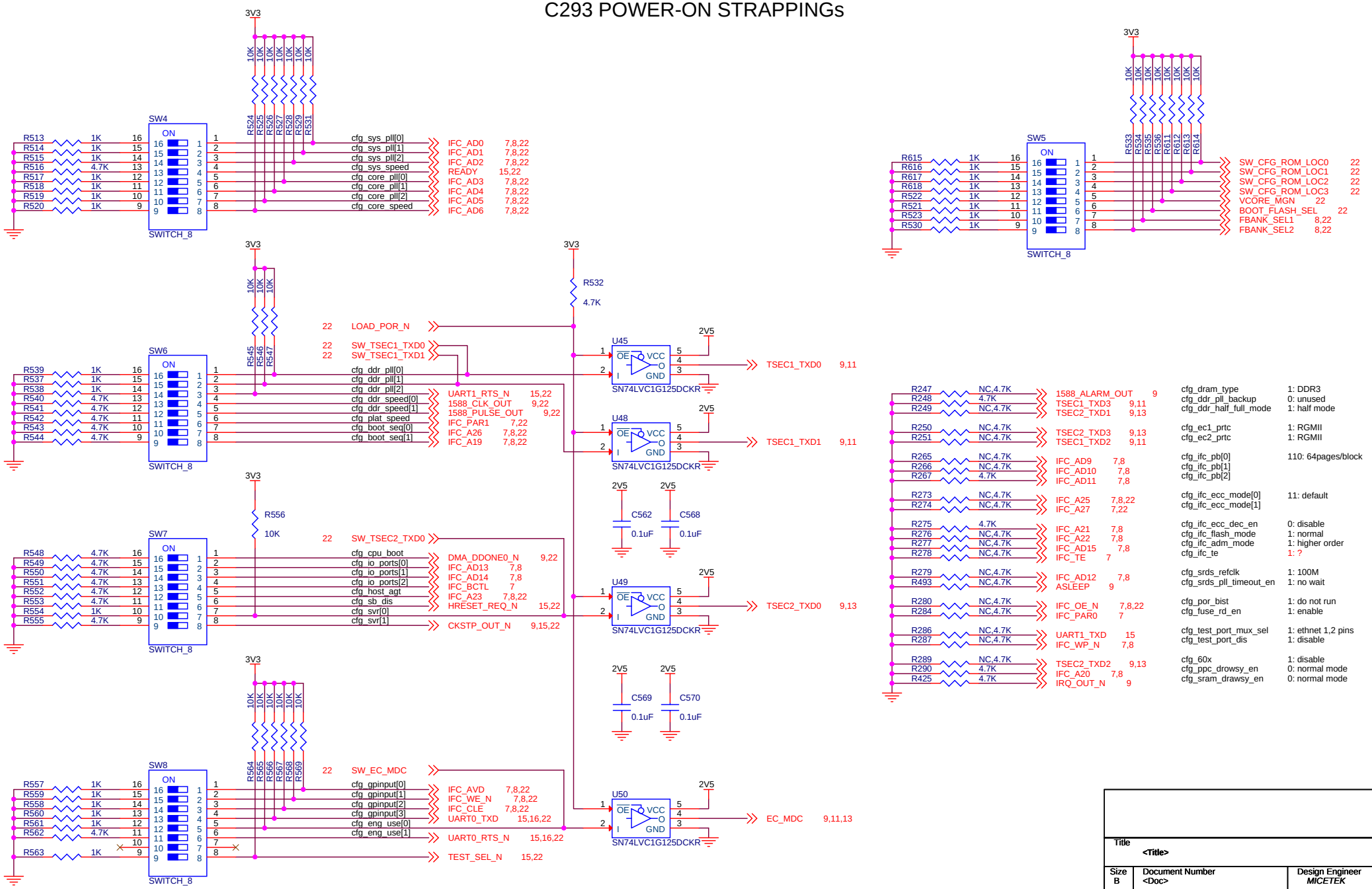
Date: Tuesday, January 07, 2014		Sheet 17 of 28	

C293 POWER-ON STRAPPINGs



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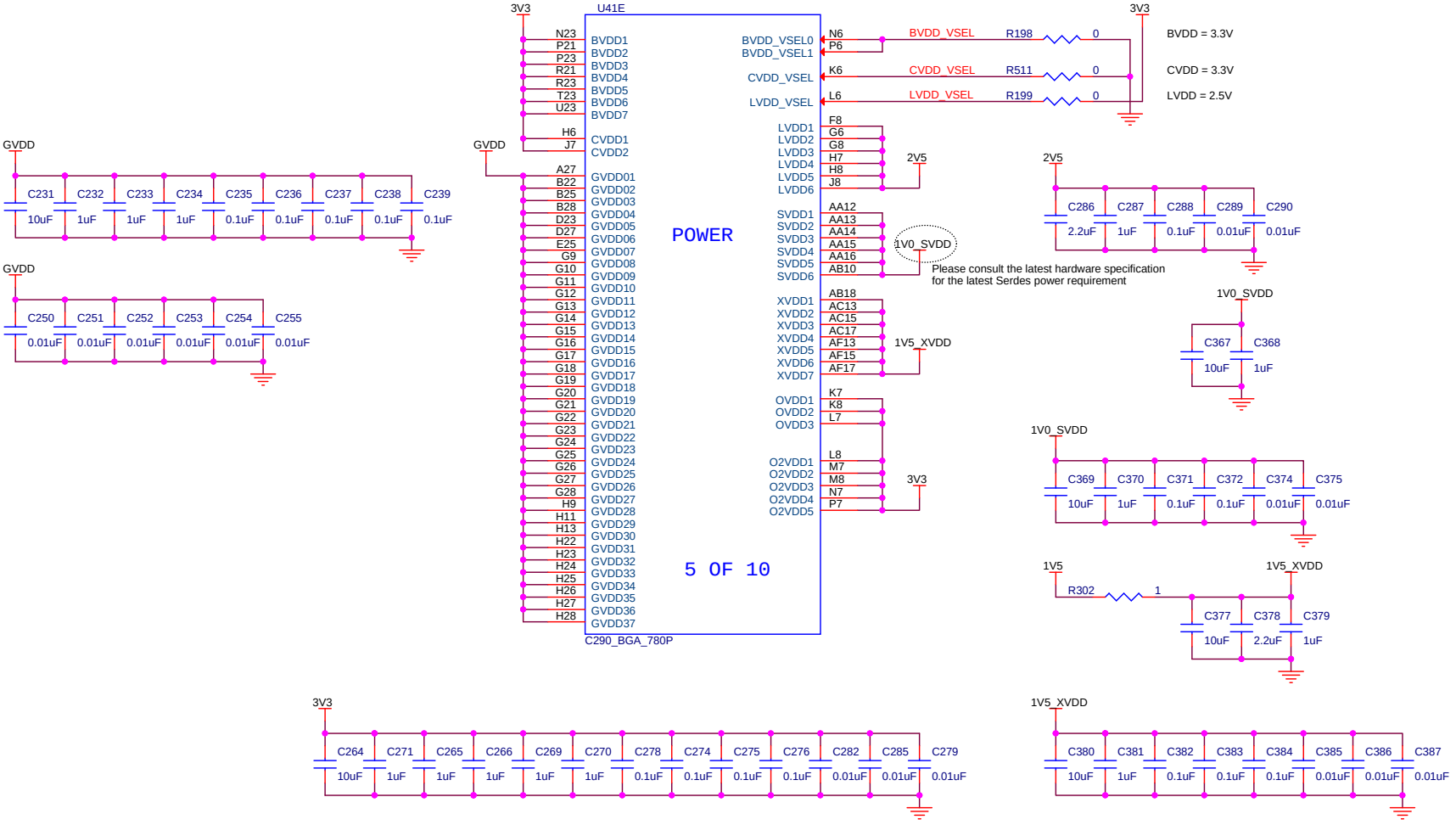
Date: Tuesday, January 07, 2014		Sheet 18 of 28	

C293 POWER SUPPLY



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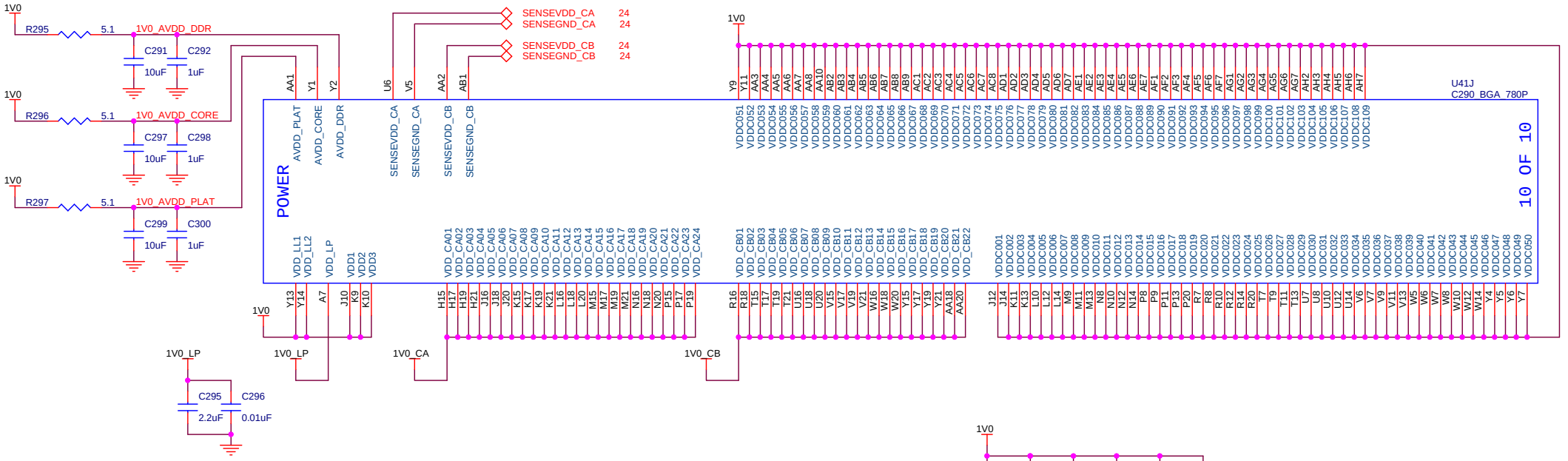
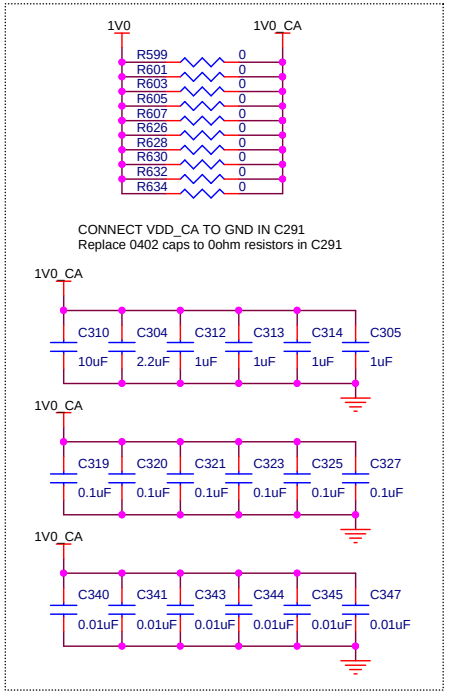
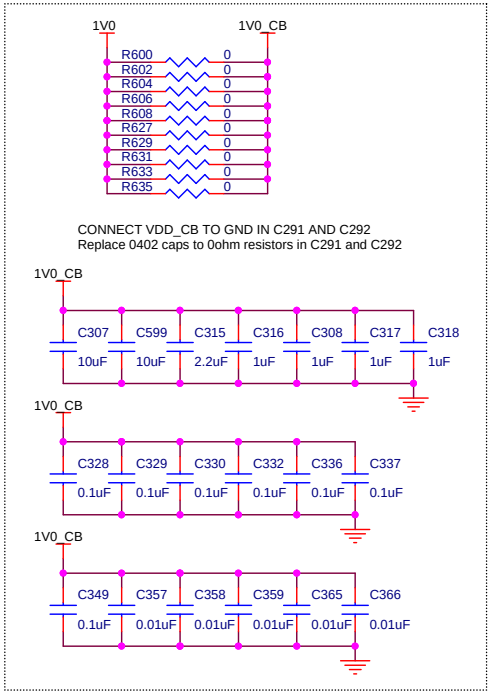
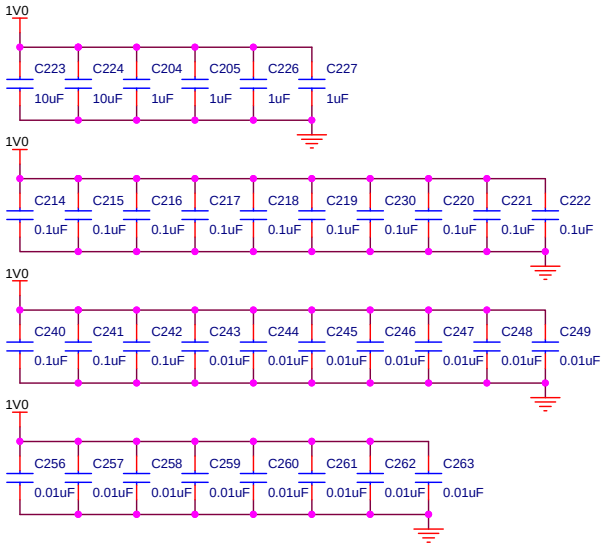
Date: Tuesday, January 07, 2014		Sheet 19 of 28	

C293 POWER SUPPLY (cont.)









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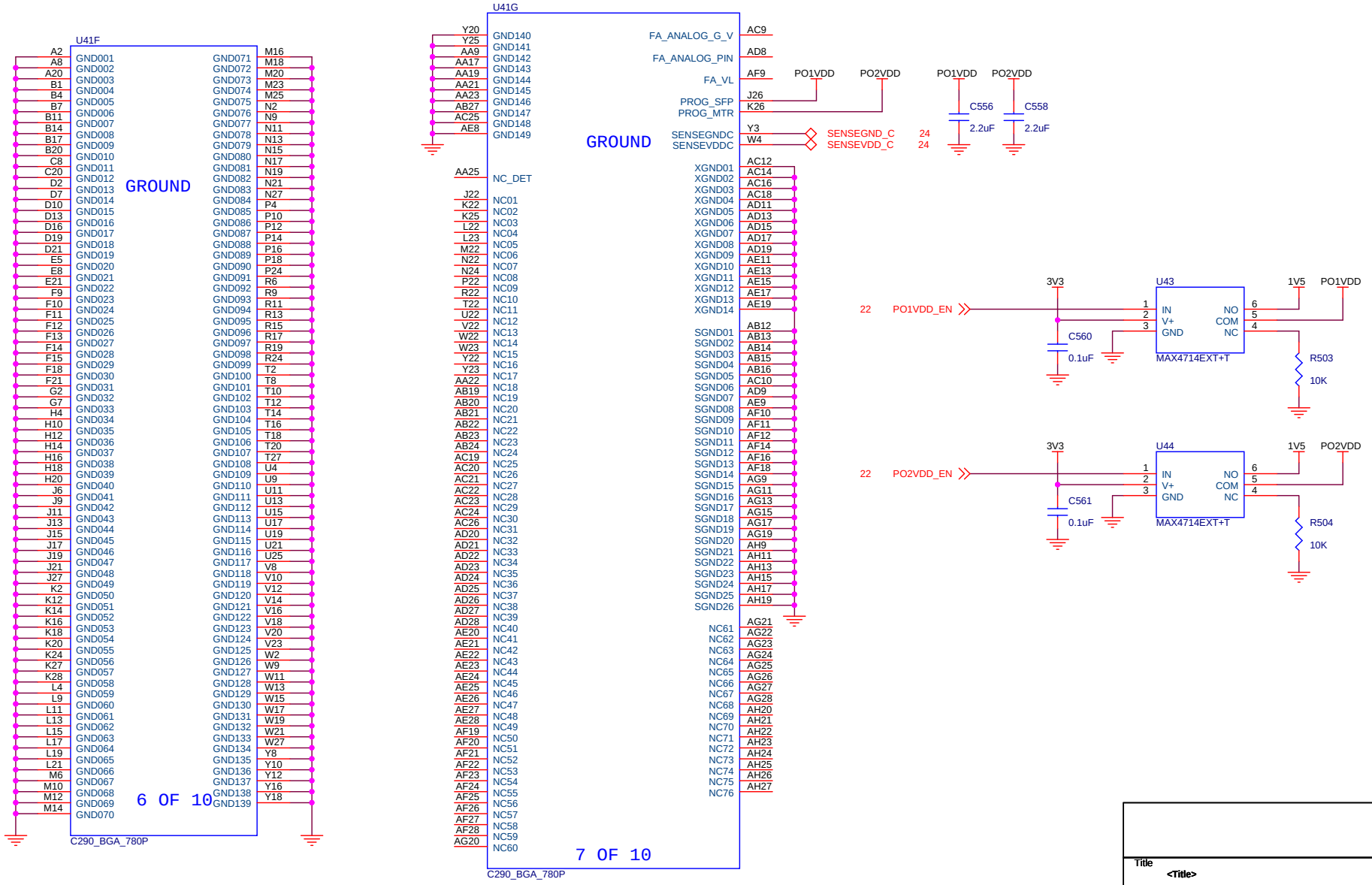
Date: Tuesday, January 07, 2014		Sheet 20 of 28	

C293 GROUND



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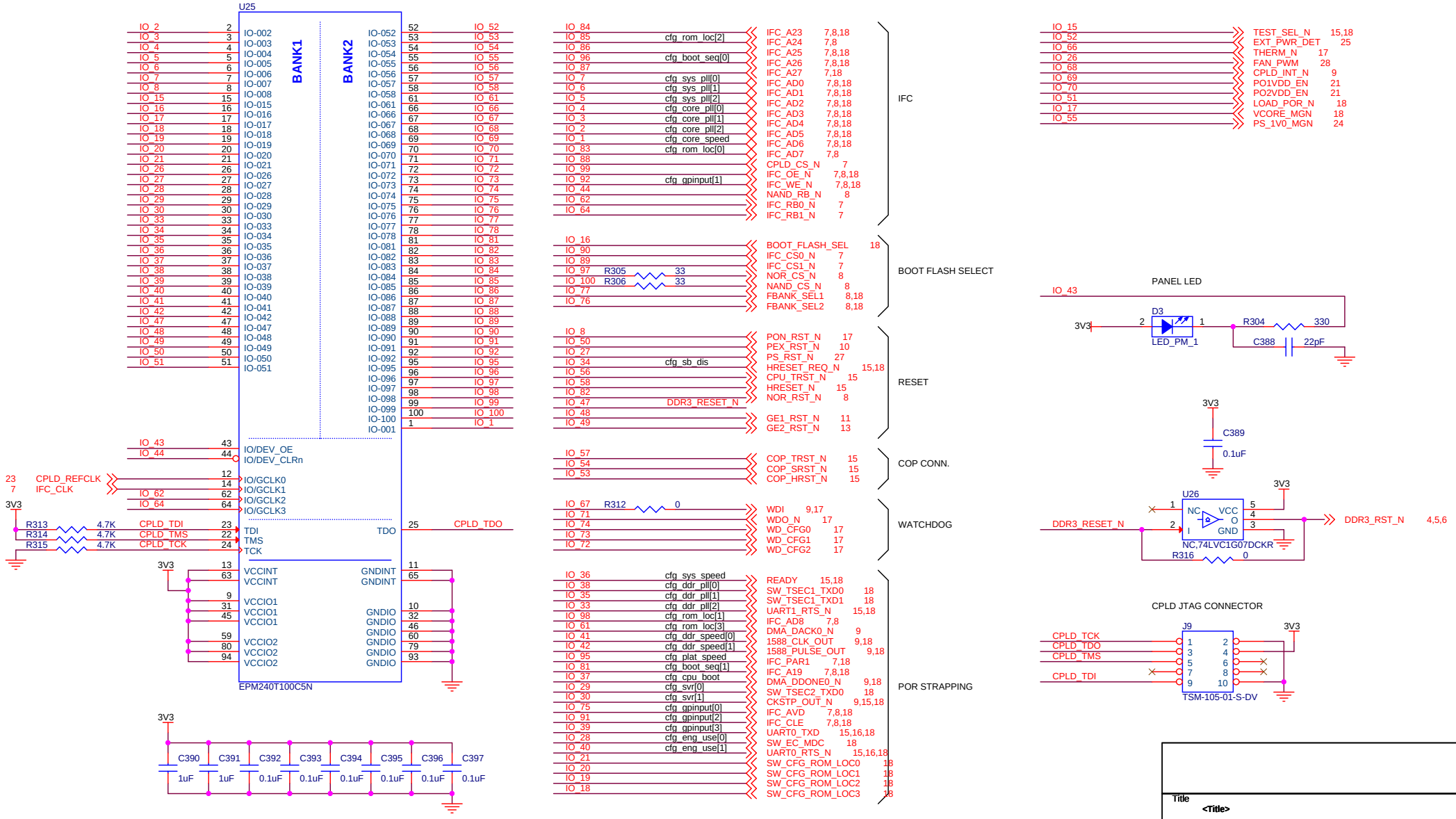
Date: Tuesday, January 07, 2014		Sheet 21 of 28	

CPLD



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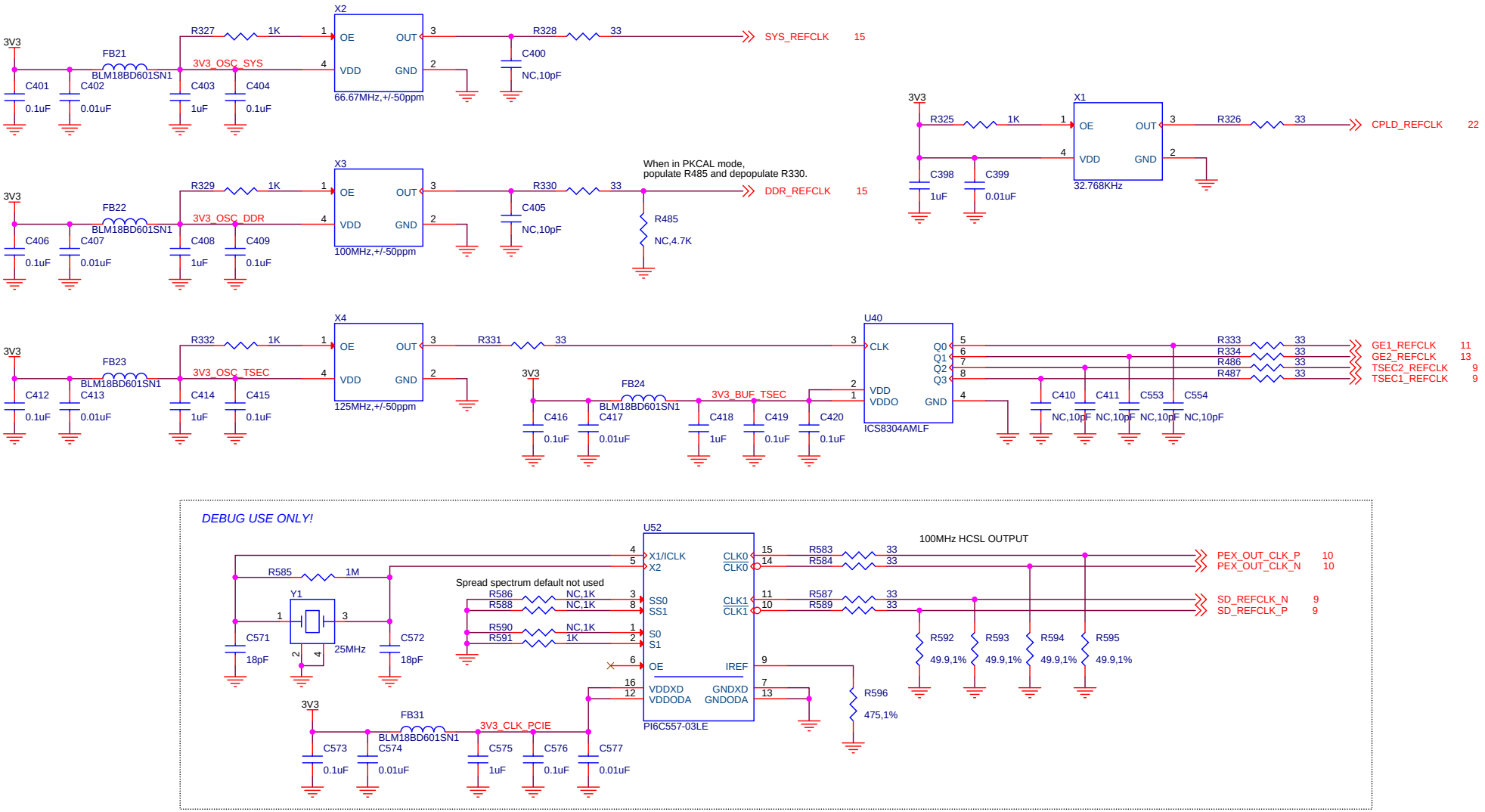
Date: Tuesday, January 07, 2014		Sheet 22 of 28	

SYSTEM CLOCK GENERATORs



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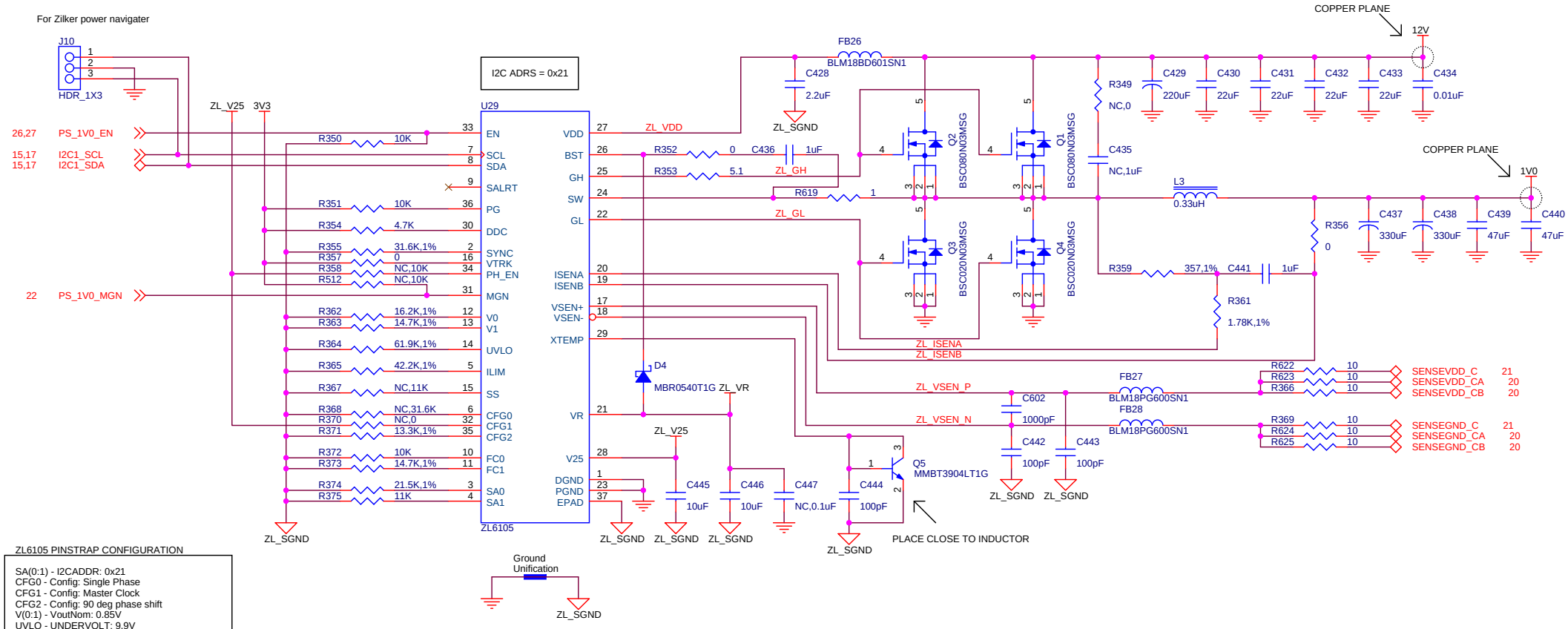
Date: Tuesday, January 07, 2014		Sheet 23 of 28	

C293 CORE POWER CONVERTOR



ZL6105 PINSTRAP CONFIGURATION

SA(0:1) - I2CADDR: 0x21
CFG0 - Config: Single Phase
CFG1 - Config: Master Clock
CFG2 - Config: 90 deg phase shift
V(0:1) - VoutNom: 0.85V
UVLO - UNDERVOLT: 9.9V
FC0 - Single Auto Comp Not Stored
FC1 - 50% Auto Comp Gain
ILIM -37.5mv/DCR for 40A
SS - SoftStart: 5ms ramp 5ms delay
FSW - Switching Freq. 615 KHZ
Shutdown if IOUT >= 45A
Inductor DCR current sensing method.
If the 50-ohm output load is populated, it will draw static current of
20 MA @ 1.0V to 22MA @ 1.1V
SGND and PGND/GND grounds are tied together at the low side of the FET Source pins.

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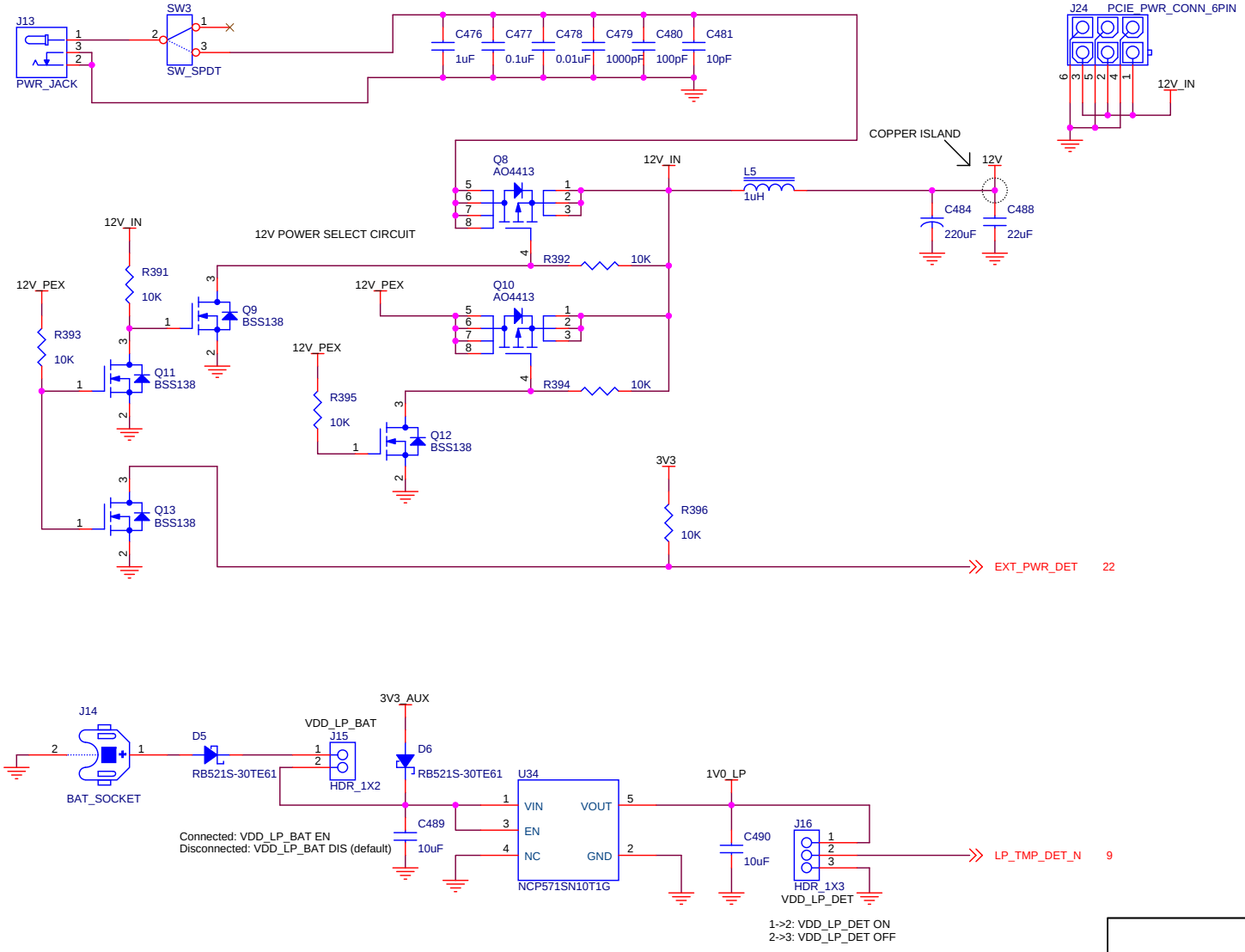
Size: B	Document Number: <Doc>	Design Engineer: MICETEK	Rev: A
Date: Tuesday, January 07, 2014		Sheet 24 of 28	

SYSTEM POWER INPUT



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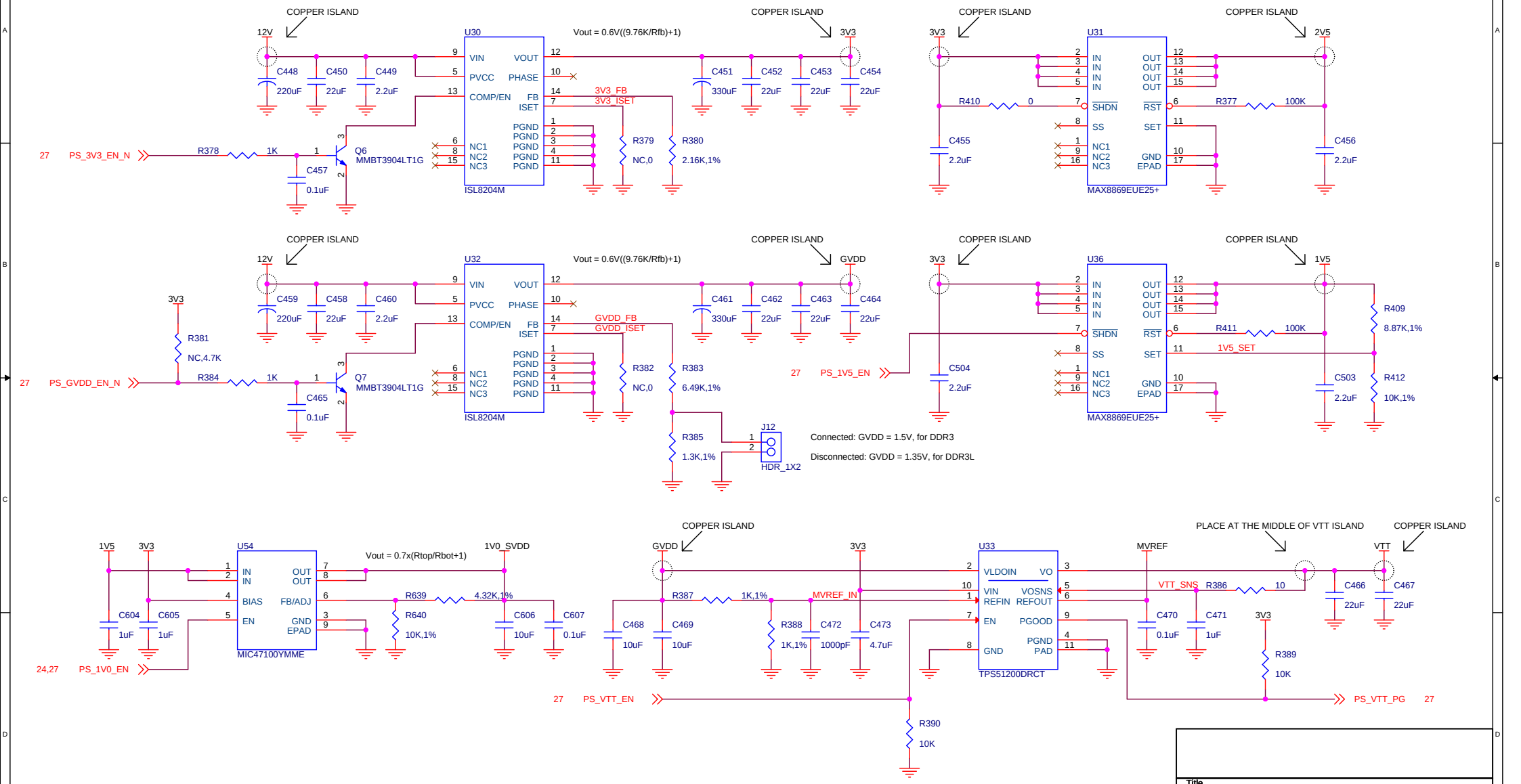
Date: Tuesday, January 07, 2014		Sheet 25 of 28	

SYSTEM POWER CONVERTORs



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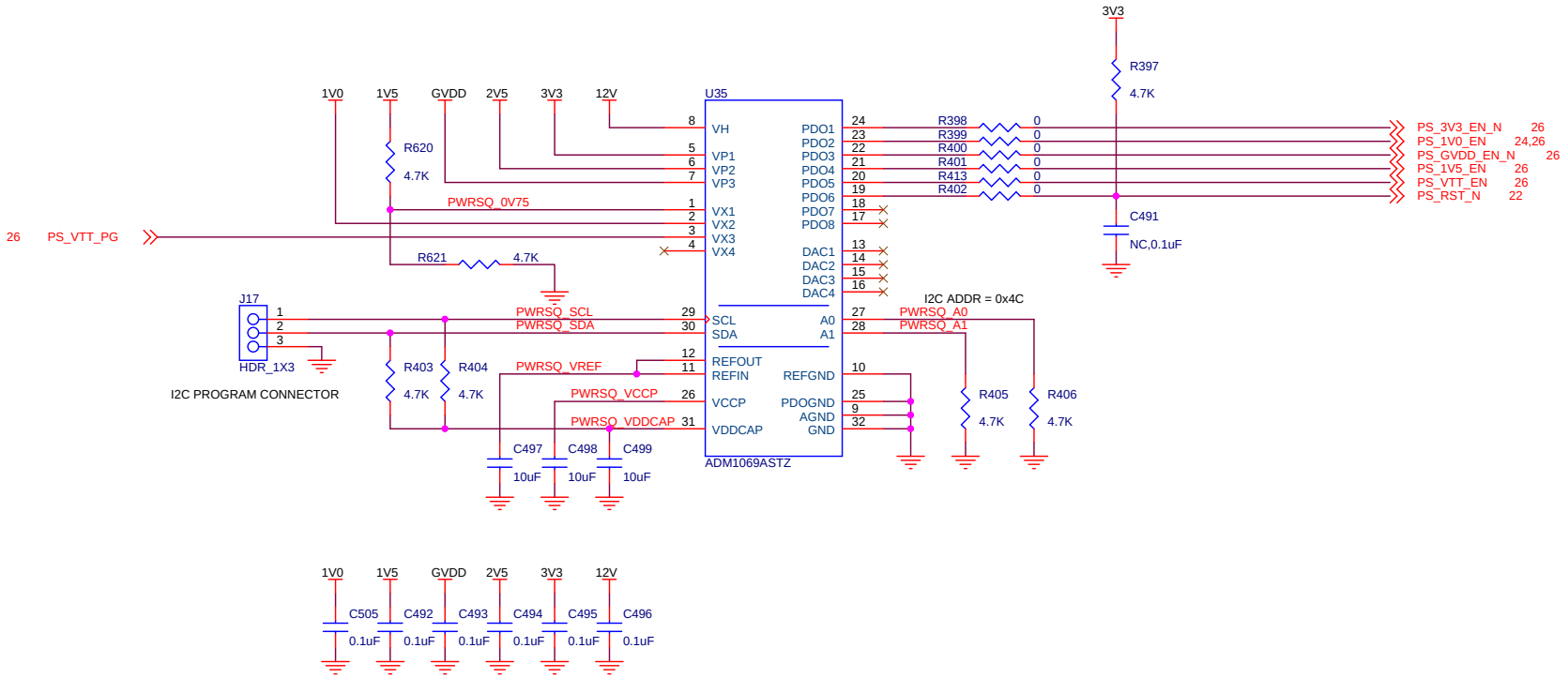
Date: Tuesday, January 07, 2014		Sheet 26 of 28	

SYSTEM POWER ON SEQUENCING



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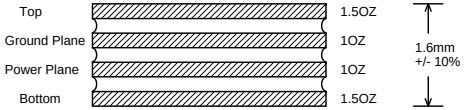
Date: Tuesday, January 07, 2014		Sheet 27 of 28	

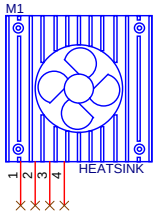
MECHANICALs

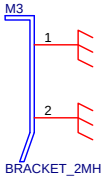
Fiducial Marks

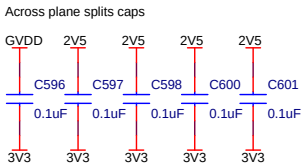
Layer Detail

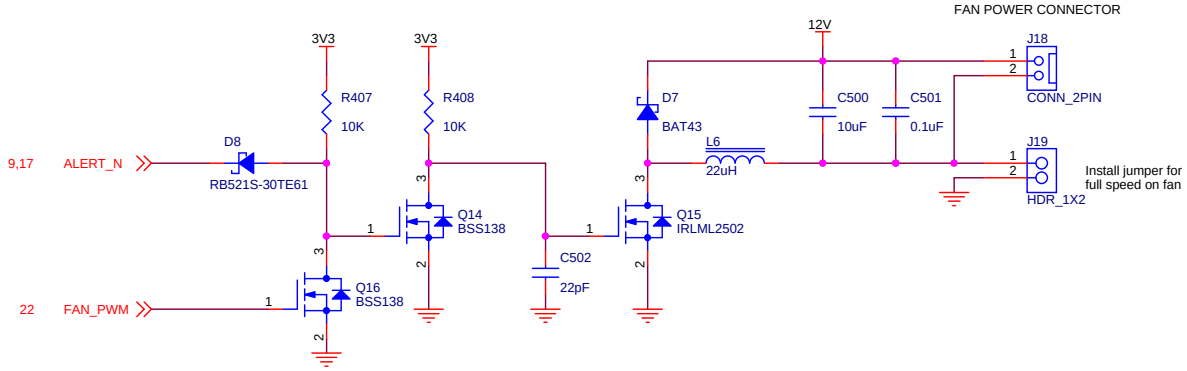


Mouting Holes









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Date: Tuesday, January 07, 2014		Sheet 28 of 28	