# Vybrid Automotive Customer Evaluation Board

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## Revision Information

<table>
<thead>
<tr>
<th>Rev</th>
<th>Date</th>
<th>Designer</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>B</td>
<td>24 April 2013</td>
<td>G. Ron</td>
<td>SCH change: - New 24 MHz crystal. - L1 TOP: remove GND plane in between USB and USB1 diff pairs. - Correct Fab note 22 to match netname changes on board. - Change Fab note 6 to 0.0035&quot;/0.0035&quot;. - Change Fab note 7 to (2-8 microinches).</td>
</tr>
</tbody>
</table>

## Notes:

- All components and board processes are to be ROHS compliant.
- All small capacitors are 0402 unless otherwise stated.
- All zero ohm links are 0603.
- All connectors and headers are denoted Px and are 2.54mm pitch, unless otherwise stated.
- All jumpers are denoted Jx. Vast majority of them are 2-mm pitch.
- Jumper default positions are shown. 2-way jumpers have *source* as pin 1.
- All Switches denoted SWx.
- All Test Points denoted TPx.
- All Test Point Vias denoted TPVx.
- User notes given throughout schematic.
- Specific PCB LAYOUT notes detailed in P&L.
- Jumper settings given throughout schematic.
- Modifications from previous major board revision given throughout schematic.

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**Note:** These schematics are provided for reference purposes only. As such, Freescale does not make any warranty, implied or otherwise, as to the suitability of circuit design or component selection (type or value) used in these schematics for hardware design using the Freescale Vybrid family of microprocessors. Customers using any part of these schematics as a basis for hardware design, do so at their own risk and Freescale does not assume any liability for such a hardware design.

This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with Vybrid processors. Although best design practices have been applied, some areas may not be suitable for a mass-production design. System evaluation was not performed over process fluctuations, voltage changes, and temperature variations.

For an added resource, refer to Vybrid Hardware Development Guide document.
Main Input and Linear Voltage Regulators (1.2V / 1.8V / 3.3V)

**Power Supply Input, Polarity Protection, and Filter**

**Label "12V, 2A"**

- **12V-POL-PROT**
- **12V-IN**

*Layout note: provide copper for good cooling.*

**1.2V Linear Regulator (150mA Max)**

- **3V3_SR**
- **5V0_SR**
- **3V3_SR**
- **5V0_SR**

- **1.2VL**
- **1.8VL**
- **3.3VL**

- **Backup supply for analog circuits**

**1.8V Linear Regulator (350mA Max)**

- **3V3_SR**
- **1V8_LR_PWRGD**
- **1V8_LR_PWRGD**
- **1V8_LR_PWRGD**

*Layout note: provide copper for good cooling.*

**3.3V Linear Regulator (500mA Max)**

- **3V3_SR**
- **3V3_SR**
- **3V3_SR**

*Layout note: provide copper for good cooling.*

**Test and Reference Points**

- **TP02**
- **TP09**
- **TP26**
- **TP10**
- **TP42**
- **TP20**

*Layout note: GND Test Points, Top Side*

- **TP51**
- **TP500**
- **TP44**
- **TP43**

*Layout note: GND Test Points, Bottom Side*

**Label each TP "GND"**

**Note:** Modifications from Rev D 27419:

- 12V input circuitry simplified.
- D500 (wrong polarity protection) connection changed.
- Optional 1.2V Linear Regulator circuitry added and DNP-ed.
- LED indication for VCC_1V2_AFE rail added.
- LED indication transistors from FET to bipolar.
Switch-Mode Voltage Regulator (5V, 3.3V, 1.5V)

Part must be 'Option E' per Selector output voltage guide.

Layout note: provide copper for good cooling.
Reset (incl I2C reset Mux) and Clocks

**Crystals**

- **MCU-XTAL**
  - C18: 0.1UF
  - C19: 0.1UF
  - R17: 10K
  - R18: 10K
  - R56: 1.5K

**I2C ADDRESS = 0x30**

- **U2**: MAX7310
  - SCL: 1
  - SDA: 2
  - AD0: 3
  - AD1: 4
  - AD2: 5
  - I/O0_OD: 6
  - I/O1: 7
  - I/O2: 8
  - I/O3: 9
  - I/O4: 10
  - I/O5: 11
  - I/O6: 12
  - I/O7: 13
  - VCC: 4
  - GND: 16

**I2C RESET Control**

- **U4**: STM6315RDW13F
  - VCC: 4
  - RST: 2
  - VSS: 1
  - MR: 3
  - R56: 1.5K

**I2C ADDRESS = 0x30**

- **All ICs**: Microchip PIC32MX270EX
  - VCC: 4
  - GND: 2
  - AD0: 3
  - AD1: 4
  - AD2: 5
  - I/O0_OD: 6
  - I/O1: 7
  - I/O2: 8
  - I/O3: 9
  - I/O4: 10
  - I/O5: 11
  - I/O6: 12
  - I/O7: 13
  - VCC: 4
  - GND: 16

**Note:** Modifications from Rev.D 27419:
- Reset circuit copied from i.MX6 design + simplified.
- R640 (2.2M resistor) added as per Erratum e5880.
- I2C RESET Control IO0 disconnected.
- I2C RESET Control IO7 re-assigned to 3.3V I2C Daughtercard.
All 0603 CC can be removed if not needed

BOOTMOD[1:0]  Boot Description
00       Boot from Fuses
01       Serial Download
10       From RCON sw.
11       Reserved

Boot Mode / RCON Configuration

Factory use only

Layout note: place J14 and J15 side by side.
CANx Physical Interface

- **VCC**: Supply voltage from 4.5V to 5.5V (with undervoltage detection kicking in between 3.5V and 4.5V).
- **VI/O**: Determines the signal level on MCU TX and RX pins and can range from 2.8V to 5.5V.
- **S**: Enables Silent mode (Listen Only) when high.

LINx Physical Interface

- **Label "LIN"**: Place J16 and J17 side by side.
- **Label "SCI"**: Default: Removed
- **Label "LIN"**: Default: 1-2

SCI Physical Interface

Note: Modifications from Rev. D 27419:
- SCI_0 is now used for Bluetooth and SCI_2 for RS-232.
MAC (Ethernet) Connections

- 8-bit I2C address: - 0xD1 for Read, - 0xD0 for Write.
- PHY reset pulled low to hold PHY in reset and its TX pins into Hi-Z until actively released by MCU via GPIO (DNP since main option is having it on ENET card).
- Critical for RCON operation.

Note: Modifications from Rev.D 27419:
- On-board PHY replaced with standard ENET board-to-board connector.
- PHY reset changed from SCI0_RST (now used by Bluetooth) to FB_AD[21] (SCI2_RST).
- Hybrid’s TRACED2 pin now used as IO for ENET_CARD_DET_B (after ARM ETM connector got removed).

Layout note: all bus and clock traces 50-ohm.
USB Interfaces

Default state: 5V OFF --> on OTG micro-AB connector

Default state: 5V ON on Type A Host connector

Layout note:
Use wide traces for:
- USB power (5V0_SR, USB_SW_OUTA, USB_SW_OUTB, USB0_OUT, and USB1_OUT),
- ESD protection.

Place USB-signal ferrite beads adjacent to their USB connectors.

Note: Modifications from Rev.D 27419:
- P9 and P1 swapped to make USB0 used for serial boot mode (OTG Micro AB connector needed)
- configuration made similar to standardized one
- 1000pF replaced with 1500pF for unification
- ESD protection scheme modified,
- - ESD_3.3V
- - ferrite bead added into USB signal lines
- - ferrite bead types optimized.

USB OTG Micro AB

Standard Type A (Host) connector

ESD Protection

Connections and Memory

**Layout note:** Place as close as possible to DDR power pins.

**Clock Termination**

DDR_CLK termination resistor close to DDR3 chip.

**0.75V Reference**

0.75V Reference circuit 240 1% instead of 470 5%.

**DDR3 MCU Connections and Memory**

Note: Modifications from Rev.D 27419:
- In 0.75V Reference circuit 240 1% instead of 470 5% (precision improvement and BOM consolidation),
- pull-up added on DDR_RST line to support DDR3
- Self-Refresh when Hybrid in LPSTOP modes.
Flash size 32MB, Sector size 64KB.

DQSx signal not used on SPANSION Flash, so may be used for GPIO in this instance.

Flash devices have internal pull-up on CS line, so no need for external pull resistors.
Note: Modifications from Rev. D 27419:
- SD socket changed to type with card detection switch, routed to pin FB_AD[20],
- Series 20-Ohm in SDHC1_CLK line deleted.
Note: Modifications from Rev.D 27419:
- for 75-Ohm impedance matching, changed to series "Short" (was 36R resistor) with 75R pull-down (was 39R),
- 3.3V unidirectional TVSs instead of 30V bidir. ones,
- series 0.1uF instead of 47nF (value unification).
24-bit DCU Daughtercard Connector (Standard)

Compatible graphic devices / daughtercards:
- HDMI (FSL # MCIMXHDMICARD / # 26673),
- Display (FSL # LCD-WVGA-7IN-1 / # 28239).

External reset:
- Valid for HDMI card,
- Invalid for MSS1 LCD panel.

Reset pulled low to hold connected device in reset and its TX pins (if relevant) into Hi-Z until actively released by MSS via GPIO. Critical for RCON operation of shared DCU lines.

Prevent resistive touch panel from being touched while booting up. Critical for RCON operation (I/Os shared).

To read resistive touch panel:
1. Set 0 & 2 to input ADC input plus ability to drive HIGH
2. Set 1 & 3 to need ability to drive HIGH or LOW

Note: Modifications from Rev D 27419:
- Universal DCU daughter-card connector used,
- Hybrid's TRACED4 pin used as optional RESET_B.
B) Daughtercard Connections

Compatible with Physical Interface Board 'OS81050 / 2+0' by SMSC.

Compatible with Physical Interface Board 'OS81050 / 2+0' by SMSC.

Note: Modifications from Rev.D 27419:
- INT line pull-up added,
- Series resistor into RST line added.

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Compatible with Physical Interface Board 'OS81050 / 2+0' by SMSC.

Note: Modifications from Rev.D 27419:
- INT line pull-up added,
- Series resistor into RST line added.
User Peripherals, Audio Controls, and GPIOs

**ADC Input Potentiometer and Test Point**
(Ideally run from linear 3.3V regulator to provide stable input voltage).

**Incremental Encoders (Volume and Tuning)**

**Push Buttons for Presets**

Caution: SW3 is also an RCON pin controlled via switches on page 4. If Pulled high for RCON, this switch will have no effect.

**Header for Digital Accessible GPIOs**

**Header for Analog Accessible GPIOs**

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*User Peripherals, Audio Controls, and GPIOs*
Audio 1: Line and Microphone Inputs

**Microphone Input (Left)**

- Label "LINE IN"
- Attenuation factor of 0.5. 0.5*Vpeak < 1.914V.

**Microphone Input (Right)**

- Label "MICROPHONE IN"
- Timing inputs from ESAI.

**Layout note:** Should have clean GNDs - tips in Datasheet.

**Output to Vybrid or DSP**

- Note: Modifications from Rev.D 27419:
  - Separate AUX_IN_GND created.
Note: Modifications from Rev.D 27419:
- In FILTER circuit 560 and 2700pF instead of 470 and 3300pF (BOM consolidation).
Compatible with "Si476x LNA-Balun Rev4.0"
RF tuner daughtercard by Silicon Labs.
I2C, CD, and Bluetooth Headers

**4-Pin Header (I2C3)**

(5V power)

**Generic CD Header**

Layout note: Place connector close to board edge.

**Bluetooth Daughtercard Header**

(compatible with Freescale part number FD-B-TOOTH-DC)

**I2C (Authentication) Daughtercard Header**

(3.3V power)

Note: Modifications from Rev.D 27419:
- SCI0_CTS (TRACE_CTL) now used for Bluetooth SCI.
- Bluetooth is now connected to SCI0 rather than SCI2.
- Added LCD 4-pin header (I2C3 interface).
- Connector for different Bluetooth daughtercard type.
Appendix 1: Customer EVB Block Diagram

I2C address of MCIMXHDIMICARD/ Agile # 26673, SiI9022A-based HDMI card:

<table>
<thead>
<tr>
<th>I2C Branch</th>
<th>Device</th>
<th>Write</th>
<th>Read</th>
<th>Speed</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Tuner</td>
<td>0xC4</td>
<td>0xC5</td>
<td>400kHz</td>
</tr>
<tr>
<td>1</td>
<td>Touch Screen</td>
<td>0x30</td>
<td>0x2E</td>
<td>400kHz</td>
</tr>
<tr>
<td>2</td>
<td>IOmux (Reset)</td>
<td>0x31</td>
<td></td>
<td>400kHz</td>
</tr>
<tr>
<td>2</td>
<td>I2C card (3.3V, 8-pin)</td>
<td>0x32</td>
<td></td>
<td>400kHz</td>
</tr>
<tr>
<td>3</td>
<td>Generic CD</td>
<td></td>
<td></td>
<td>400kHz</td>
</tr>
<tr>
<td>1</td>
<td>MLB</td>
<td>0x40</td>
<td>0x41</td>
<td>400kHz</td>
</tr>
<tr>
<td>3</td>
<td>Ethernet Card</td>
<td>0xD1</td>
<td>0xD2</td>
<td>400kHz</td>
</tr>
<tr>
<td>1</td>
<td>Most = MLB</td>
<td></td>
<td></td>
<td>400kHz</td>
</tr>
<tr>
<td>1</td>
<td>DCU</td>
<td></td>
<td></td>
<td>400kHz</td>
</tr>
</tbody>
</table>

Transmitter Programming Interface (TPI) device address: 0x72
CEC Programming Interface (CPI) device address: 0xC0
SiI9020-compatible internal registers: first device address: 0x72
SiI9020-compatible internal registers: second device address: 0x7A

Note: Modifications from Rev.D 27419:
- I2C1 also used for DCU daughtercard connector.
- I2C3 also used for Ethernet daughtercard connector.
2: Audio Routing Diagram