

FRDM-IMX8MPLUS

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(FRDM-IMX8MPLUS Development Board)

Revision History

Rev. Code	Date	By	Description
A1	2024-11-30	Polyhex	Initial version
A2	2025-01-15	Polyhex	ENET2_AVDDL to ENET2_DVDDL 3.3V volage level for RST and INT HDMI_DDC_SCL, HDMI_DDC_SDA, HDMI_CEC, HDMI_HPD are 3.3V signals W2_UART_CTS and W2_UART_CTS are crossed Delete U7/U8, Change power supply DCDC solution U105/U106/U107 Delete U39, VCC_EXT_3V3 supply DSI&CAM_3V3 The 40-pin EXP_CN (J18) is the same as 8MP EVK TCPC_nINT and TCPC1_nINT are connected to SAI1_TXD6/TXD7 Add Power Switch Fan connector (J29) to a 2-pin 2mm connector Add Net DEB_UART4_TX/DEB_UART4_RX Add U104/74AVC4TD245GU
B1	2025-04-21	Polyhex	Update U4 MFG_PN01 from "W25Q64JWSSIQ" to "W25Q256JWPIQ" Update U51 Value/MFG_PN01 from "TJA1051T/3" to "TJA1051T/3/2Z" Update U6 Value/MFG_PN01 from "PCA9450CHN" to "PCA9450CHNY" Update U58,U61 Value/MFG_PN01 from "NTS0104GU12" to "NTS0104GU12,115" Update U11,U20 Value/MFG_PN01 from "NX20P0407" to "NX20P0407UKAZ" Update U14 Value/MFG_PN01 from "NX20P3483UK" to "NX20P3483UKAZ" Update J3 Value/MFG_PN01 from "HY-TC-101" to "5001-UPC079B-24R1-01" Update SW6,SW7,SW8 Value/MFG_PN01 from "TS-A016_H3P5" to "TS-A016_H2P5" Update U9 Value from "NX20P5090UK" to "NX20P5090UKAZ" Update U10,U15 Value from "PTN5110" to "PTN5110NHQZ" Update FB2,FB3,FB4,FB5,FB6,FB7,FB8,FB9,FB10,FB13,FB14,FB17,FB18 Value from "PZ3216D600" to "BLM15PX121SN1D" Update U13 Value from "SGM8709YN5G" to "SGM8709YN5G/TR" Update U63 Value from "74AVC4T3144GU12" to "74AVC4T3144GU12X" Update U62 Value from "74AVC8T245BQ" to "74AVC8T245BQ,118" Update D4,D5,D10,D15,D17,D18,D19,D21,D23,D29,D31 Value from "BAT54HT1" to "BAT54HT1G" Update U18 Value from "CBTL02043ABQ" to "CBTL02043ABQ,115" Add Test Point TP185 Change J21 Pin3 Net to HP_J_R, Pin4 Net to HP_J_L Add R631, Q25, R632

1. Interrupted lines coded with the same letter or letter combinations are electrically connected.
2. Device type number is for reference only. The number varies with the manufacturer.
3. Special signal usage:


_B Denotes - Active-Low Signal

<> or [] Denotes - Vectored Signals
4. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

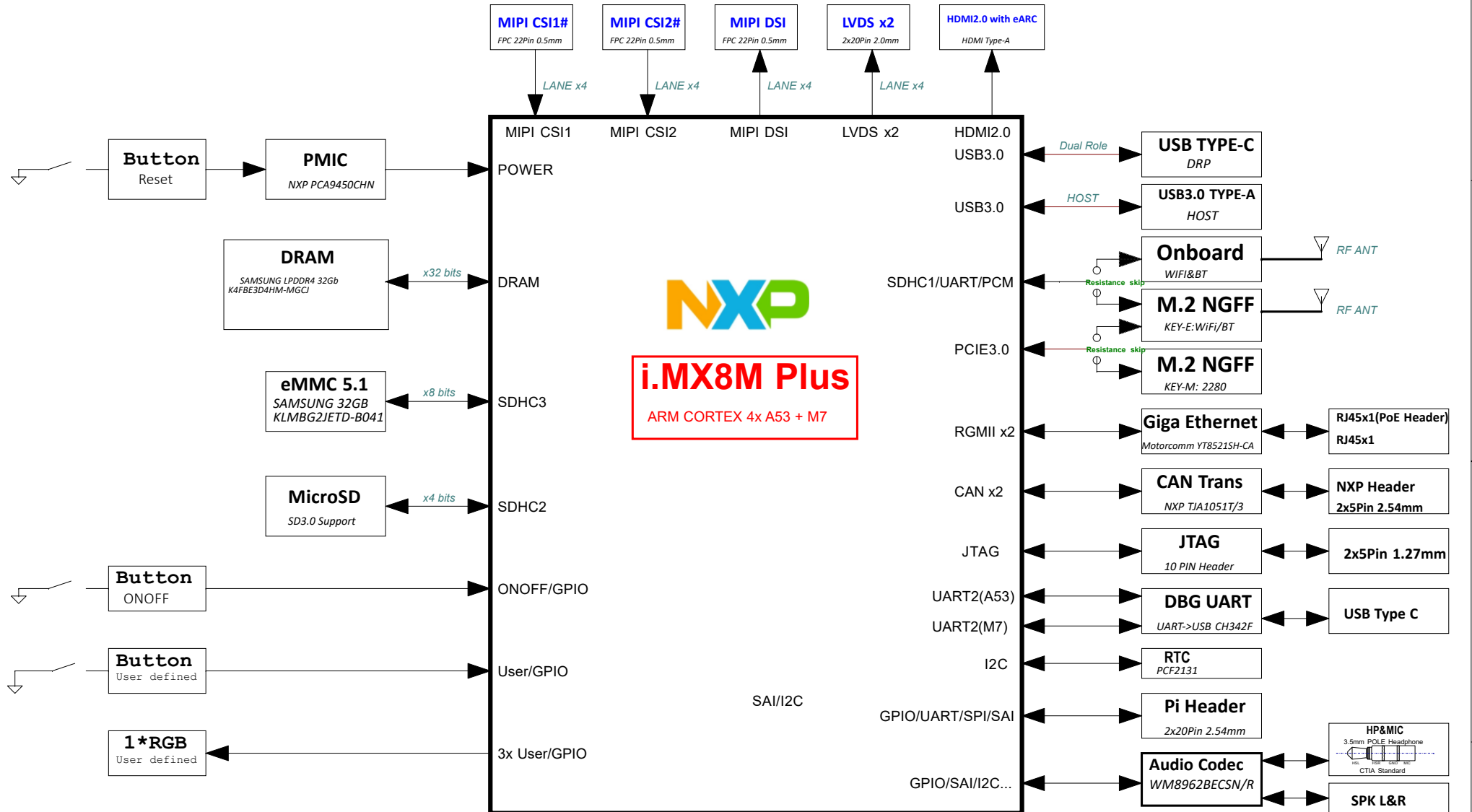
Preliminary - Subject to Change without Notice!


This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with i.MX processors. Although best design practices have been applied, some areas may not be suitable for a mass-production design.

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FRDM-IMX8MPLUS Block Diagram



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USB C SNK PD

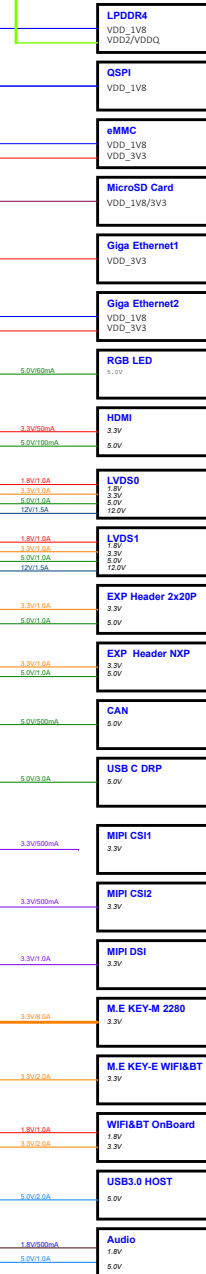
VBUS

12-20V

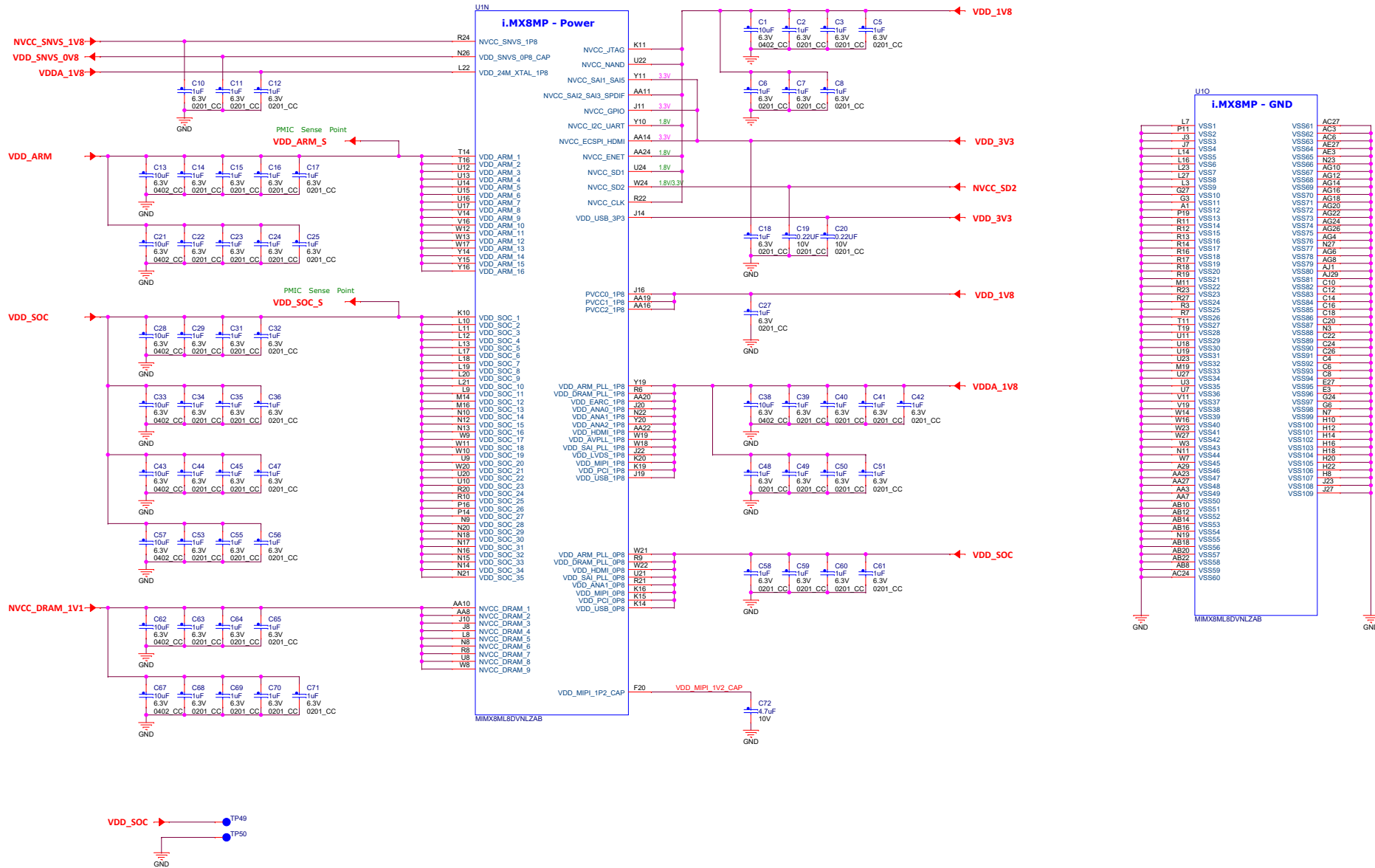


PMIC: PCA9450C			
SEQ	REG	TYP	Max Capability(mA)
1	LDO1	1.8	10
2	RTC_CLK	--	--
3	BUCK1/3	0.85/0.95	6000
4	BUCK2	0.85/0.95/1.0	3000
5	LDO3	1.8	300
6	BUCK5	1.8	2000
7	BUCK6	1.1	2000
8	BUCK4	3.3	3000
9	MUXSW	3.3	400
9	LDO5	3.3/1.8	150
10	POR_B	--	--

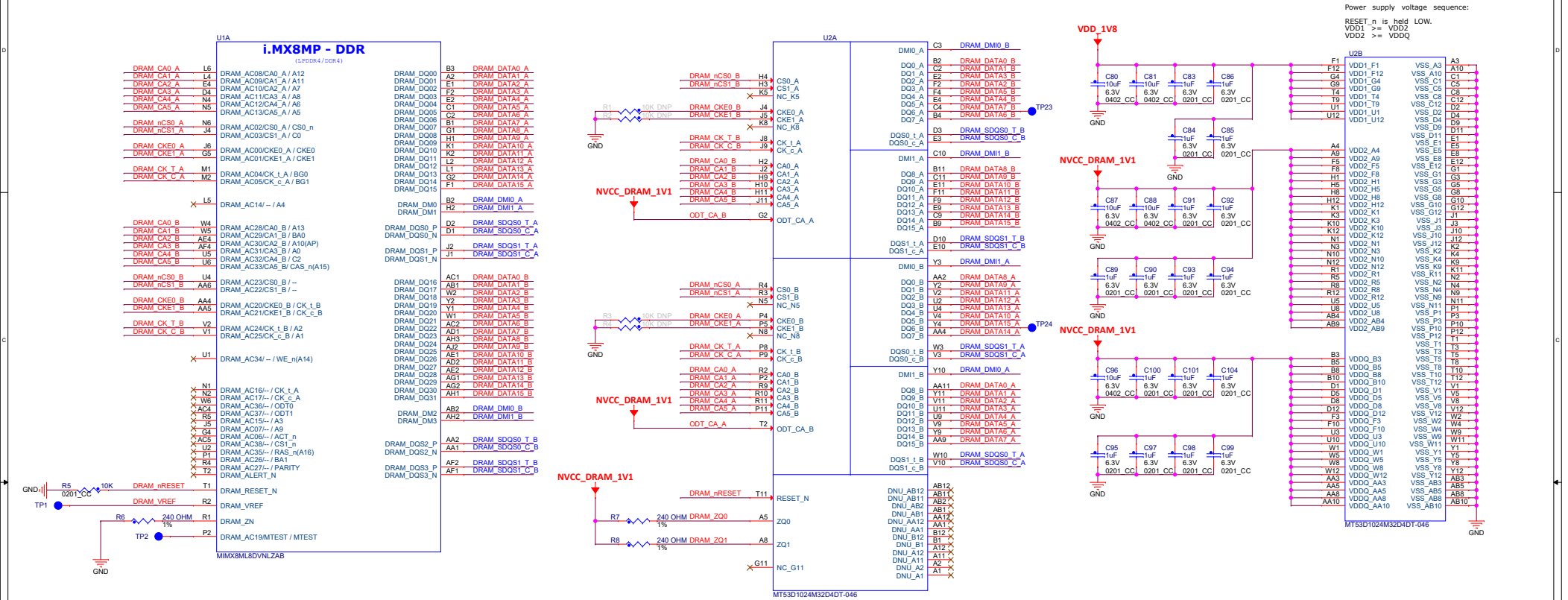
CPU: i.MX8M Plus			
SEQ	PWR/Signal	TYP	Required(mA)
1	NVCC_SNV5_V18	1.8	10
2	32K_INTERNAL	---	---
3	VDD_SOC	0.85/0.95	5000
4	VDD_ARM	0.85/0.95/1.0	21000
5	VDDA_V18	1.8	300
6	VDD_V18/NVCC_xxxx	NvccVx(0.5x)	---
7	NVCC_DRAM_V11	NvccVx(0.5x)	---
8	VDD_V3V3/NVCC_xxxx	NvccVx(0.5x)	---
9	VSD_V3V3	3.3/1.8	10
10	NVCC_SD2	---	---
	PODR_B	---	---



i.MX8M Plus PWR

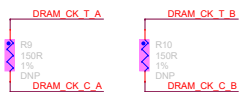


LPDDR4 4GB



Note:
LPDDR4 ODT on i.MX 8M Plus is command-based, ODT_CA/A/B of LPDDR4 part should be connected directly to VDD2.

Data Bus

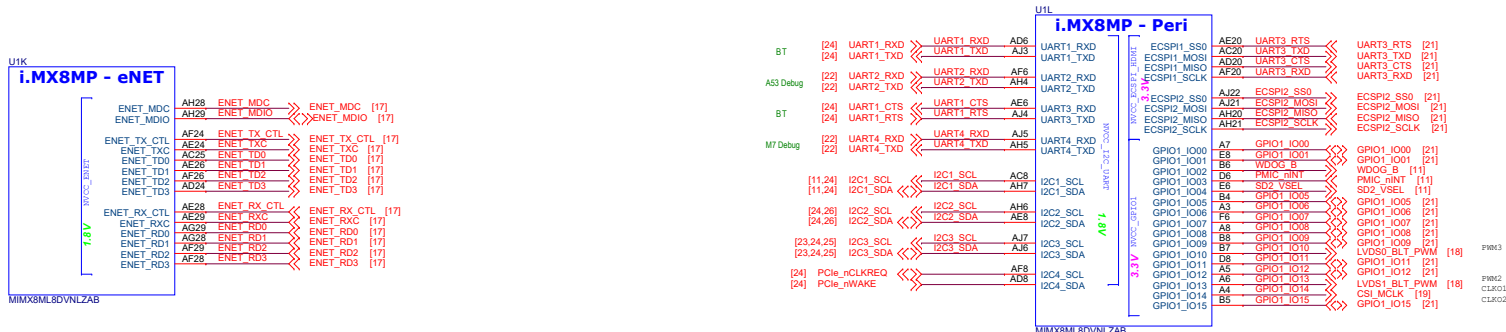
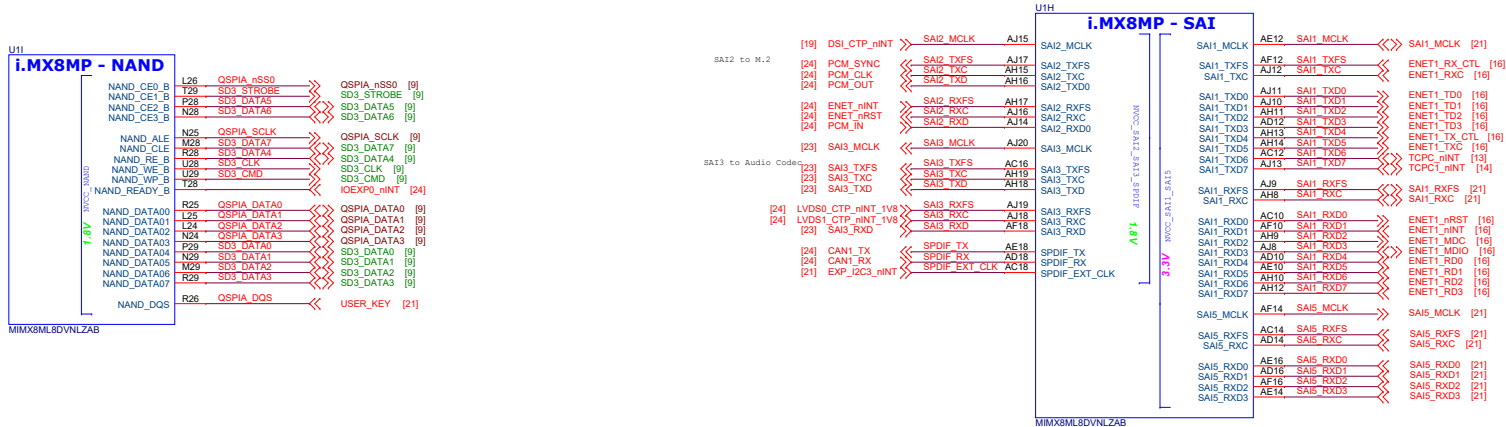


Command/Address

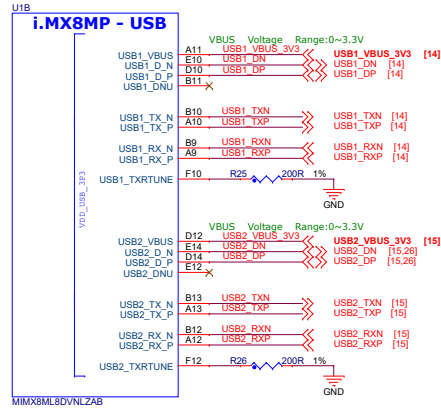
Pin Name	LPDDR4	DDR4
DRAM_DQ00_P	DQ00_L	DQ00_L
DRAM_DQ00_N	DQ00_C	DQ00_C
DRAM_DQ01	DQ01_A	DQ01_A
DRAM_DQ02	DQ02_A	DQ02_A
DRAM_DQ03	DQ03_A	DQ03_A
DRAM_DQ04	DQ04_A	DQ04_A
DRAM_DQ05	DQ05_A	DQ05_A
DRAM_DQ06	DQ06_A	DQ06_A
DRAM_DQ07	DQ07_A	DQ07_A
DRAM_DQ08	DQ08_A	DQ08_A
DRAM_DQ09	DQ09_A	DQ09_A
DRAM_DQ10	DQ10_A	DQ10_A
DRAM_DQ11	DQ11_A	DQ11_A
DRAM_DQ12	DQ12_A	DQ12_A
DRAM_DQ13	DQ13_A	DQ13_A
DRAM_DQ14	DQ14_A	DQ14_A
DRAM_DQ15	DQ15_A	DQ15_A
DRAM_DQ16	DQ16_A	DQ16_A
DRAM_DQ17	DQ17_A	DQ17_A
DRAM_DQ18	DQ18_A	DQ18_A
DRAM_DQ19	DQ19_A	DQ19_A
DRAM_DQ20	DQ20_A	DQ20_A
DRAM_DQ21	DQ21_A	DQ21_A
DRAM_DQ22	DQ22_A	DQ22_A
DRAM_DQ23	DQ23_A	DQ23_A
DRAM_DQ24	DQ24_A	DQ24_A
DRAM_DQ25	DQ25_A	DQ25_A
DRAM_DQ26	DQ26_A	DQ26_A
DRAM_DQ27	DQ27_A	DQ27_A
DRAM_DQ28	DQ28_A	DQ28_A
DRAM_DQ29	DQ29_A	DQ29_A
DRAM_DQ30	DQ30_A	DQ30_A
DRAM_DQ31	DQ31_A	DQ31_A

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NXP SE	C	SCH-95022 PDF: SPF-95022	
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i.MX8M Plus IO Interface

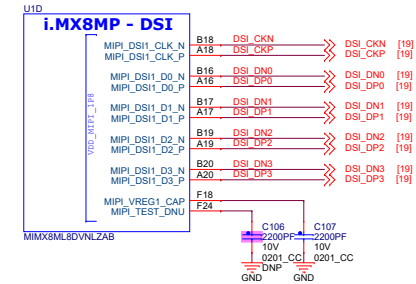
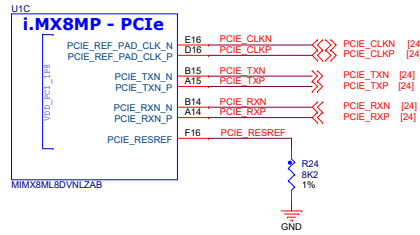


i.MX8M Plus PHYs



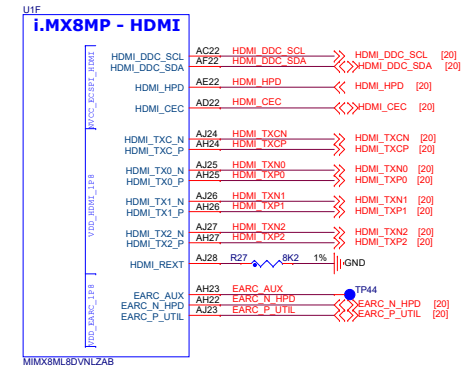
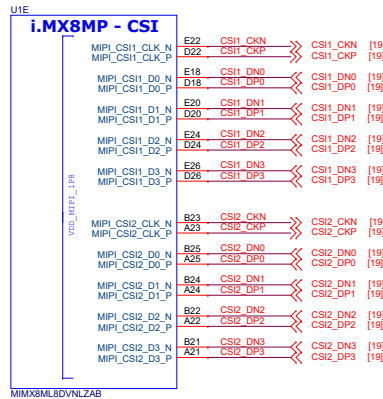
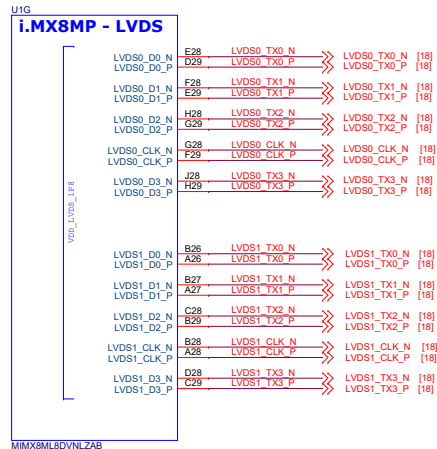
Note:

1. USB1_DNU, USB2_DNU are not functional, if USB ID function is needed, use common GPIO.
2. If USB connector is MicroAB or MicroB, USBx_VBUS MUST not connect directly to the 5V VBUS voltage of connector; instead, this pin must be isolated with an external 30K 1% resistor.



Note:

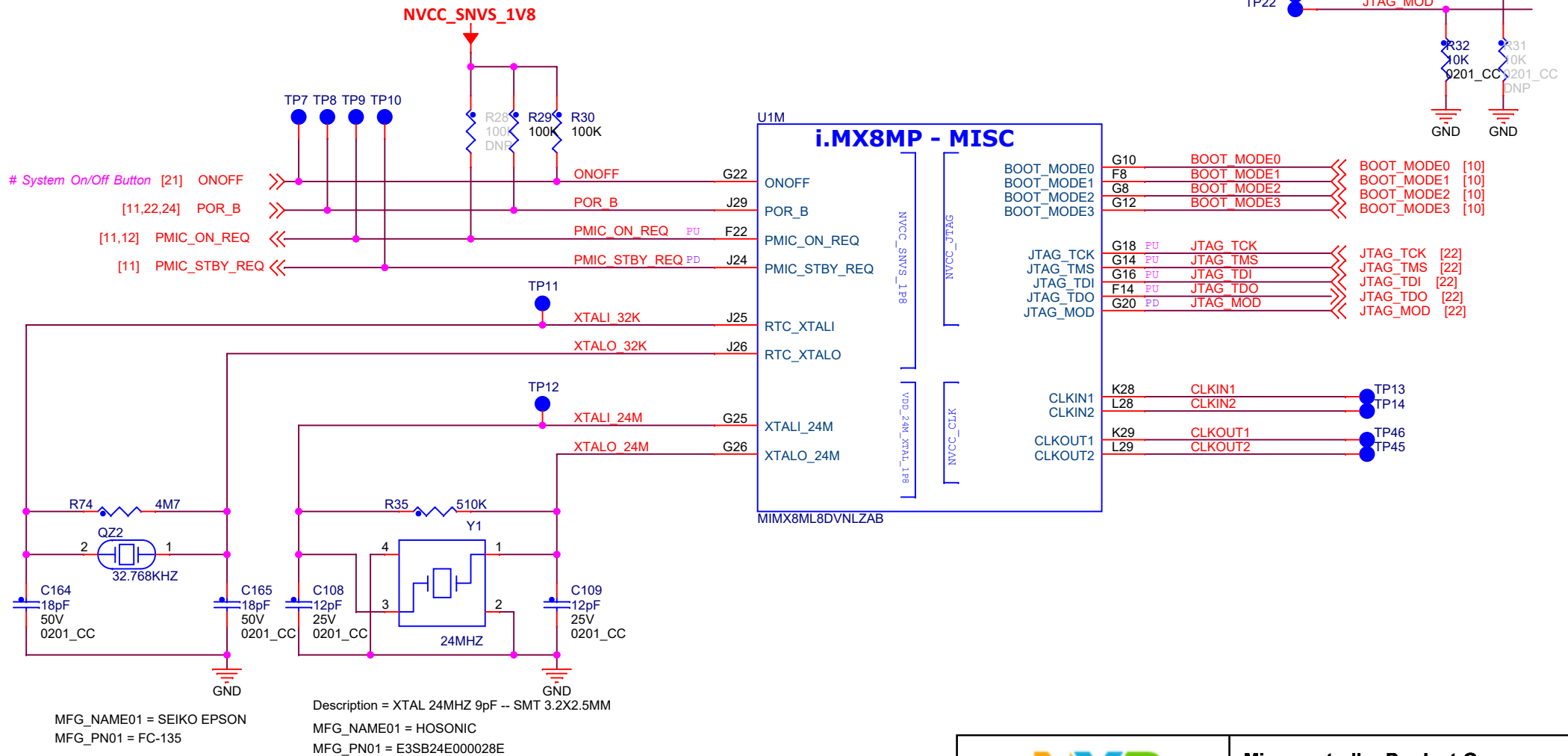
MIPI_TEST_DNU is for internal test, can be floating for normal use.



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i.MX8M Plus MISC

JTAG Debug

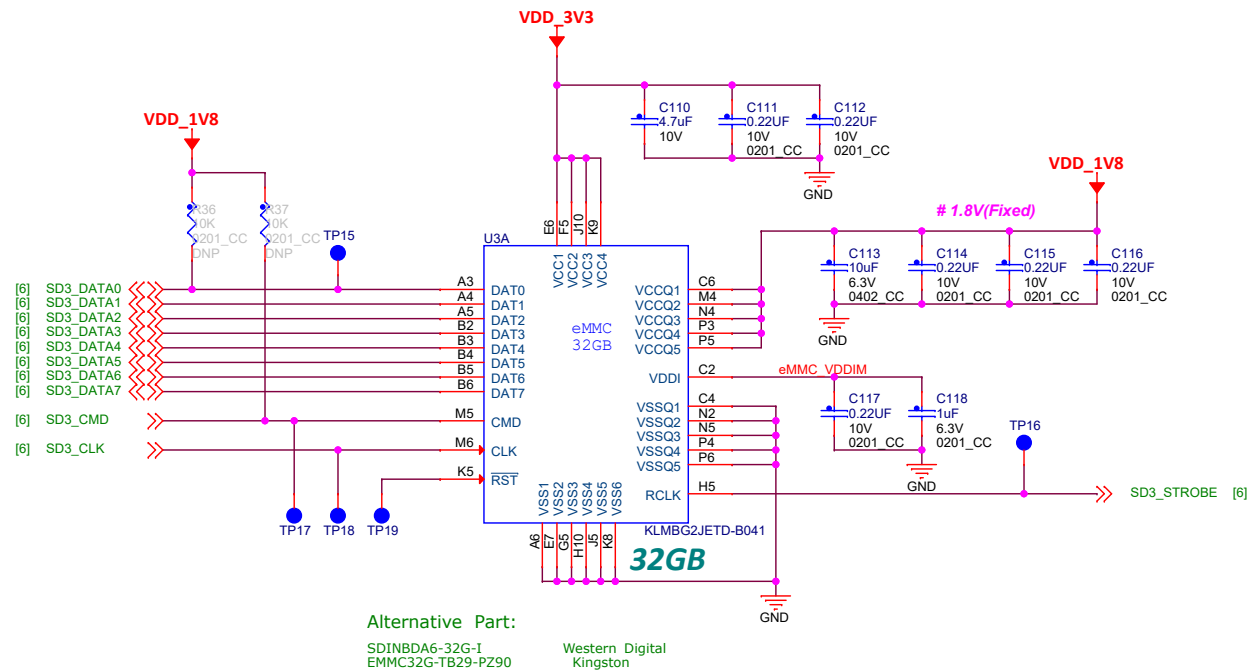


Caution:

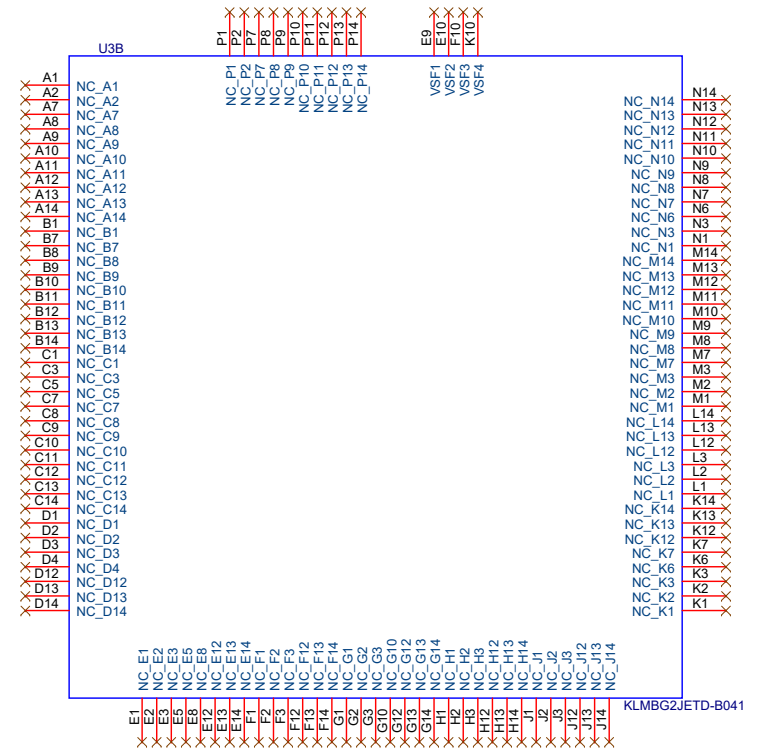
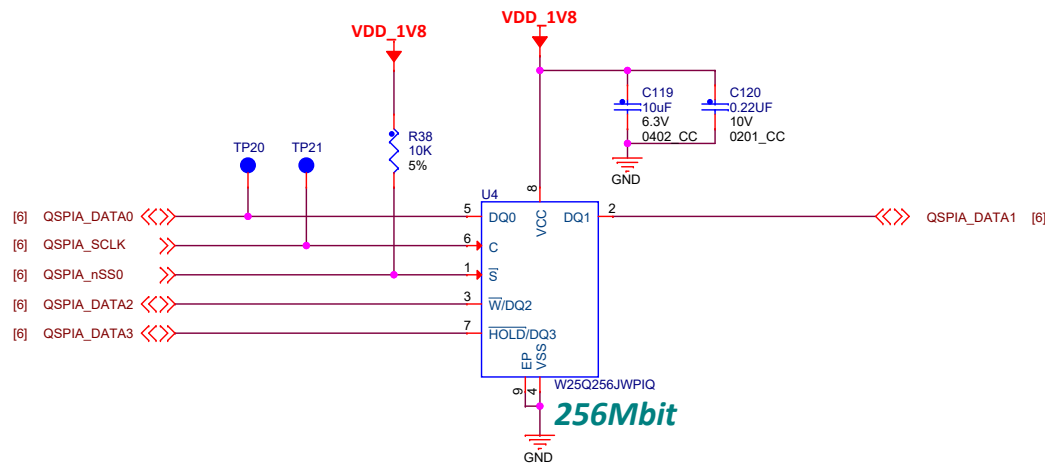
BOOT_MODE0, BOOT_MODE1, BOOT_MODE2, BOOT_MODE3, JTAG_MOD and POR_B must be pulled to "111111" for i.MX8M Plus to enter Boundary Scan mode.


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eMMC5.1



QSPI Flash



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Boot Mode and CFG Switch

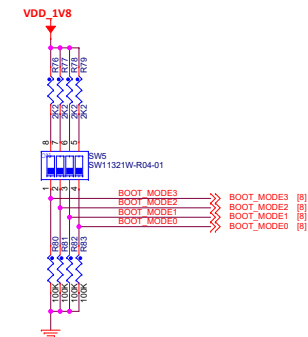
i.MX8M Plus ROM Fuse


Full Line Address	Physical Address	7	6	5	4	3	2	1	0
0x470[15:0]	0x470[7:0]	OVERWRITE_NAND_PG_PER_BLK_VAL 00 - 32 pages 01 - 64 pages 10 - 128 pages 11 - 32 pages		OVERWRITE_FLEXSPI_BT_SEL 0 - Do not override 1 - Override	OVERWRITE_FLEXSPI_BT_SEL_VAL 00 - FlexSPI (HyperFlash 1.8V) 01 - FlexSPI (Flash with 4B READ)(1x13 default supported) 10 - Default Octal mode (Micron, supported on 8QXP B0 already) 11 - Default Octal mode (Mic, Nice to have)		FLEXSPI_AUTO_PROBE_EN 0 - Disable 1 - Enable	FLEXSPI_AUTO_PROBE_TYPE 00 - QuadSPI NOR 01 - MicronOctal 10 - MicronOctal 11 - AdestoOctal	
0x480[15:0]	0x480[7:0]	Reserved			FLEXSPI_DUMMY_CYCLE_SEL			FLEXSPI_FREQ_SEL 000 - 100 MHz 001 - 133 MHz 010 - 166 MHz 011 - 200 MHz 100 - 80 MHz 101 - 20 MHz	
0x480[31:16]	0x480[23:16]	NOC_ID_REMAP_BYPASS	ROM_NO_LOG if blown, ROM will not log event to log buffer	SDP_DISABLE Disable USB serial download	FORCE_BT_FROM_FUSE Boot from programmed fuses, not Boot Mode Pins		FLEXSPI_HOLD_TIME_SEL 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms	WDG_TIMEOUT_SELECT 00 - 2.0s 01 - 1.5s 10 - 1.0s 11 - 0.5s	
0x490[15:0]	0x490[7:0]	USDHC_PWR_EN 0 - No power cycle 1 - Enabled via	EMMC_FAST_BT 0 - Regular 1 - Fast Boot	SDMMC_BUS_WIDTH 00 - 8-bit 01 - 4-bit 10 - 8-bit DDR (MMC 4.4) 11 - 4-bit DDR (MMC 4.4)	SD_SPEED: 00 - Normal/SDR12 01 - High/SDR25 10 - 8-bit DDR (MMC 4.4) 11 - SDR104	EMMC_SPEED: 00 - Normal 01 - High	USDHC_VOL_SEL For Normal Boot Mode IO Voltage 0 - 3.3V 1 - 1.8V	USDHC_MFG_VOL_SEL For Mfg Mode IO Voltage 0 - 3.3V 1 - 1.8V	
0x490[31:16]	0x490[23:16]	RECOVERY_SDMMC_BOOT_DIS 0 - Enable 1 - Disable		IMG_CNTRN_SET1_OFFSET			USDHC_PAD_SION_EN 0 - Disable 1 - Enable	BT_RDC_DISABLE	USDHC_DLL_EN 0 - Disable DLL for SD/eMMC 1 - Enable DLL for SD/eMMC
0x4A0[15:0]	0x4A0[7:0]	SD_CALI_STEP '00' - 1 TBD		USDHC_PWR_INTERVAL 00 - 20ms 01 - 10ms 10 - 5ms 11 - 2.5ms	USDHC_PWR_DELAY 0 - 5ms 1 - 2.5ms	USDHC_PWR_POLARITY 0 - Low 1 - High	USDHC_OVRD_PAD_SETTING_UP1	EMMC_FAST_BT_ACK 0 - Boot Ack Disabled 1 - Boot Ack Enabled	
0x4A0[31:16]	0x4A0[23:16]	Reserved							
0x4B0[15:0]	0x4B0[7:0]	Reserved			NAND_GPMI_DDR_DLL_VAL (GPMI Read DDR DLL Target Value) 0000 - 7 0001 - 1 0111 - 0 1111 - 15		USB_SS_ENABLE	NAND_CS_NUM (Nand Number Of Devices) 00 - 1 01 - 2 10 - 4 11 - Reserved	
0x4B0[31:16]	0x4B0[23:16]	Reserved		FlexSPI NAND Busy Bit Offset Override		FlexSPI NAND CS Interval 00-100ns 01-200ns 10-400ns 11-50ns		FlexSPI NAND Column Address Width 00-12 01-13 10-14 11-15	

i.MX8M Plus Boot Mode

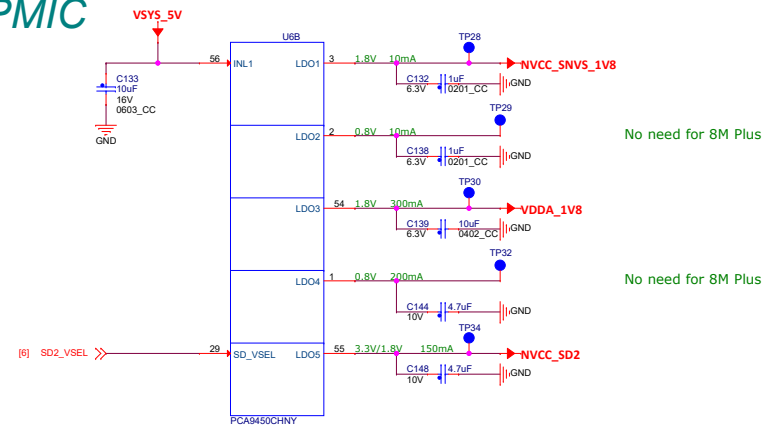
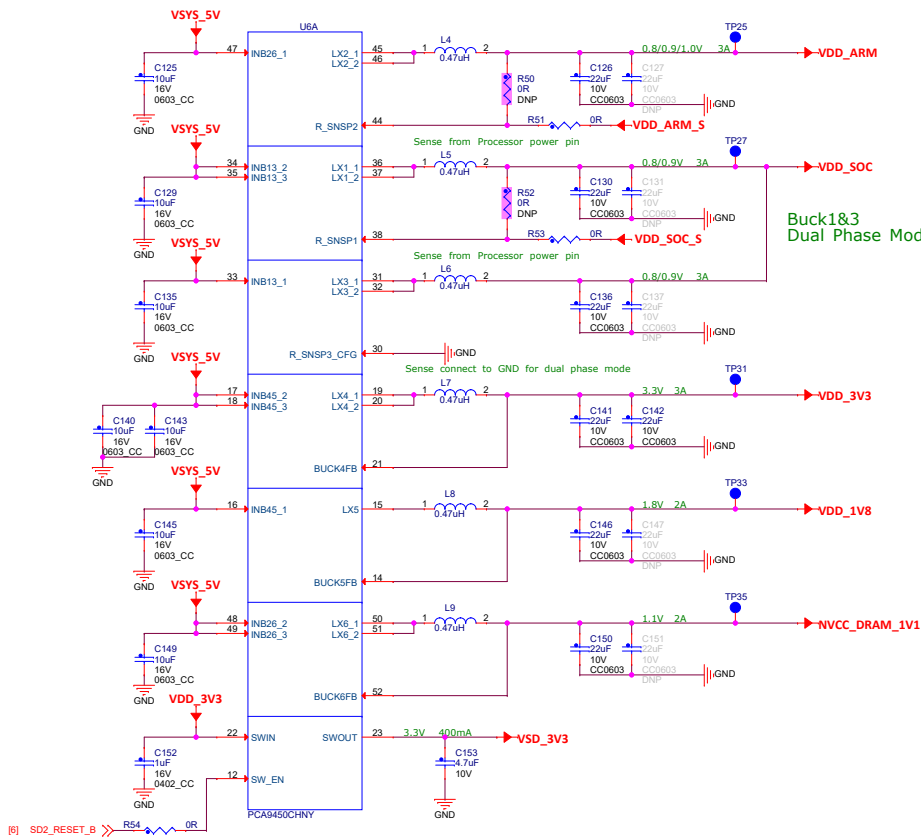
BOOT_MODE3	BOOT_MODE2	BOOT_MODE1	BOOT_MODE0	Boot Modes
0	0	0	0	Boot From Internal Fuses
0	0	0	1	USB Serial Download
0	0	1	0	USDHC3 (eMMC boot only, SD3 8-bit) Default
0	0	1	1	USDHC2 (SD boot only, SD2)
0	1	0	0	NAND 8-bit single device 256 page
0	1	0	1	NAND 8-bit single device 512 page
0	1	1	0	QSPI 3B Read
0	1	1	1	QSPI HyperFlash 3.3V
1	0	0	0	ecSPI Boot
1	0	0	1	Reserved
1	0	1	0	FLEXSPI Serial NAND 2k page
1	0	1	1	FLEXSPI Serial NAND 4k page
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Full Line Address	Physical Address	7	6	5	4	3	2	1	0
0x470[15:0]	0x470[15:8]	BOOT_MODE_FUSES BootRom will retrieve boot mode from these fuses instead of BOOT_MODE pins if * BOOT_MODE_PINS=0x0 or * BT_FUSE_SEL blown				OVERWRITE_USDHC_BT_SEL 0 - Do not override 1 - Override	OVERWRITE_USDHC_BT_SEL_VAL 00 - uSDHC1 SD 01 - uSDHC1 eMMC 10 - uSDHC2 eMMC 11 - uSDHC3 SD		OVERWRITE_NAND_PG_PER_BLK 0 - Do not override 1 - Override
0x480[15:0]	0x480[15:8]	BT_LPB (Core/DDR/Bus) '00'/'01' - LPB Disable '10' - Div by 2 '11' - Div by 4	BT_LPB_POLARITY (GPIO polarity)	ICACHE_DIS L1 I-Cache DISABLE	TZASC_EN	WDG_EN '0' - Disabled '1' - Enabled	BT_FREQ_SEL (ARM/DDR) 0 - 800 / 800 MHz 1 - 400 / 400 MHz	DCACHE_DIS Disable L1 and L2 D-Cache	
0x480[31:16]	0x480[31:24]	ECSPI_PORT_SEL 000 - eCSPI1 001 - eCSPI2 010 - eCSPI3	ECSPI_ADDR_SEL 0 - 3-bytes (24-bit) 1 - 2-bytes (16-bit)	ECSPI_CS_SEL(SPI only) 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3	RECOVER_ECSPI_BOOT_EN '0' - Disabled '1' - Enabled	DCACHE_BYPASS_DIS			
0x490[15:0]	0x490[15:8]	USDHC_DLL_SEL 0 - DLL Slave Mode for 1 - DLL Override Mode	SDMMC_DLL_DLY[6:0] Delay target for USDHC DLL, it is applied to slave mode target delay or override mode target delay depends on DLL Override fuse bit value.						
0x490[31:16]	0x490[31:24]	USDHC_OVRD_PAD_SETTING_LOW[7:0]							
0x4A0[15:0]	0x4A0[15:8]	BT_TOGGLE_MODE	NAND_FCB_SERCH_COUNT 00 - 2 01 - 2 10 - 4 11 - 8	NAND_TG_PREAMBLE_RD_LATENCY (Toggle Mode 33MHz Preamble Delay, Read Latency) '000' - 16 GPMICLK cycles. '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 3 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles. '1111' - 15 GPMICLK cycles				NAND_RST_TIME	
0x4A0[31:16]	0x4A0[31:24]	NAND_OVERRIDE_PAD_SETTING[7:0]							
0x4B0[15:0]	0x4B0[15:8]	NAND_READ_RETRY_SEQ_ID[3:0] 0000 - don't use read retry(RR) sequence embedded in ROM 0001 - Micron 20nm RR sequence 0010 - Toshiba A19nm RR sequence 0011 - Toshiba 19nm RR sequence 0100 - SanDisk 19nm RR sequence 0101 - SanDisk 19nmRR sequence 0110 - Hynix 20nm A Die RR sequence 0111 - Hynix 26nm RR sequence 1000 - Hynix 20nm B Die RR sequence 1001 - Hynix 20nm C Die RR sequence Others - Reserved				NAND_ROW_ADDR_BYTES 00 - 3 01 - 2 10 - 4 11 - 5	Reserved	Reserved	
0x4B0[31:16]	0x4B0[31:24]	RNG_TRIM[7:0]							

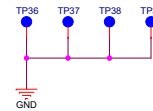


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Date: Monday, April 21, 2025		Sheet 10 of 27	

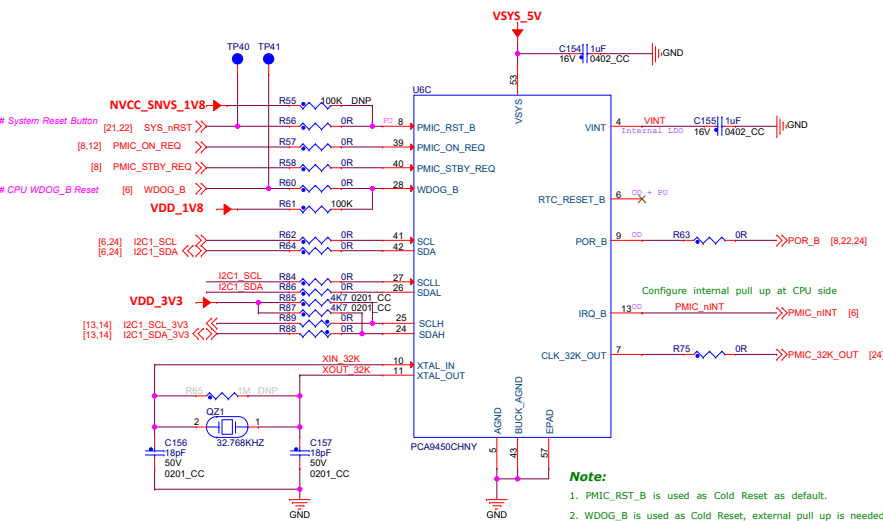
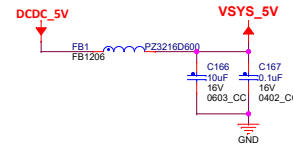
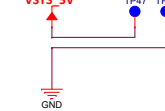
SYS PMIC



GND Testpoints



Backup PWR Supply

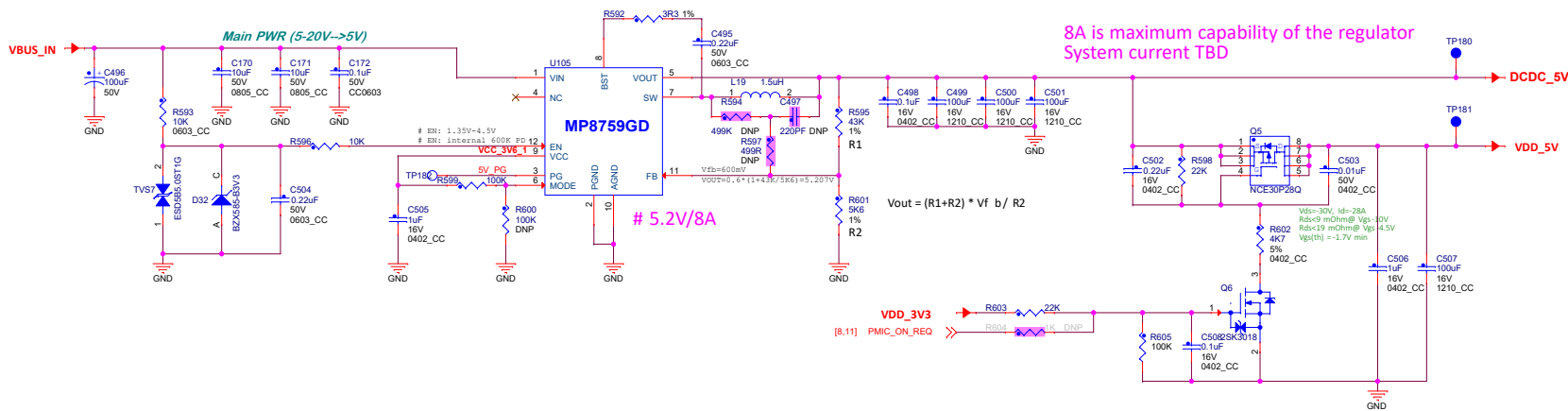


i.MX8M Plus LPDDR4 EVK Power Sequence and Operating Range						
SEQ	PWR/Signal	REG	MIN	TYP	MAX	Max Current(mA)
1	NVCC_SNVS_1V8	LDO1	1.71	1.8	1.95	10
2	32K_INTERNAL	RTC_CLK	--	--	--	--
3	VDD_SOC	BUCK1/3	0.805/0.9	0.85/0.95	0.9/1.0	6000
4	VDD_ARM	BUCK2	0.805/0.9/0.95	0.85/0.95/1.0	0.9/1.0/1.05	3000
5	VDDA_1V8	LDO3	1.71	1.8	1.89	300
6	VDD_1V8/NVCC_XXX	BUCK5	1.65	1.8	1.95	2000
7	NVCC_DRAM_1V1	BUCK6	1.045	1.1	1.155	2000
8	VDD_3V3/NVCC_XXX	BUCK4	3	3.3	3.6	3000
9	VSD_3V3	MUXSW	3	3.3	3.6	400
8	NVCC_SD2	LDO5	3.0/1.65	3.3/1.8	3.6/1.95	150
10	POR_B	POR_B	--	--	--	--

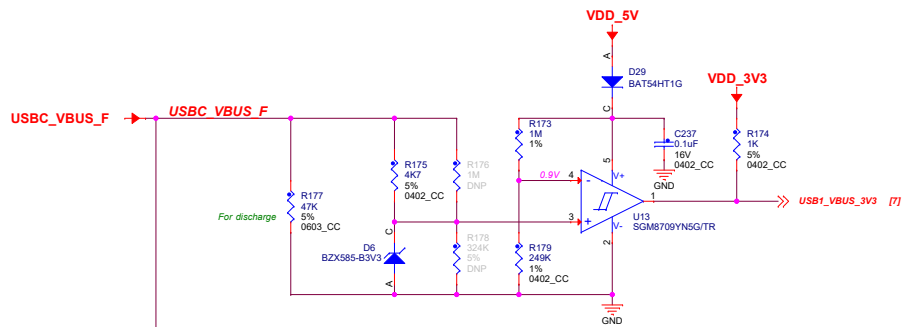
Note:
 1. PMIC_RST_B is used as Cold Reset as default.
 2. WDOG_B is used as Cold Reset, external pull up is needed for BSDL mode.

MFG_NAME01 = SEIKO EPSON
 MFG_PN01 = FC-135

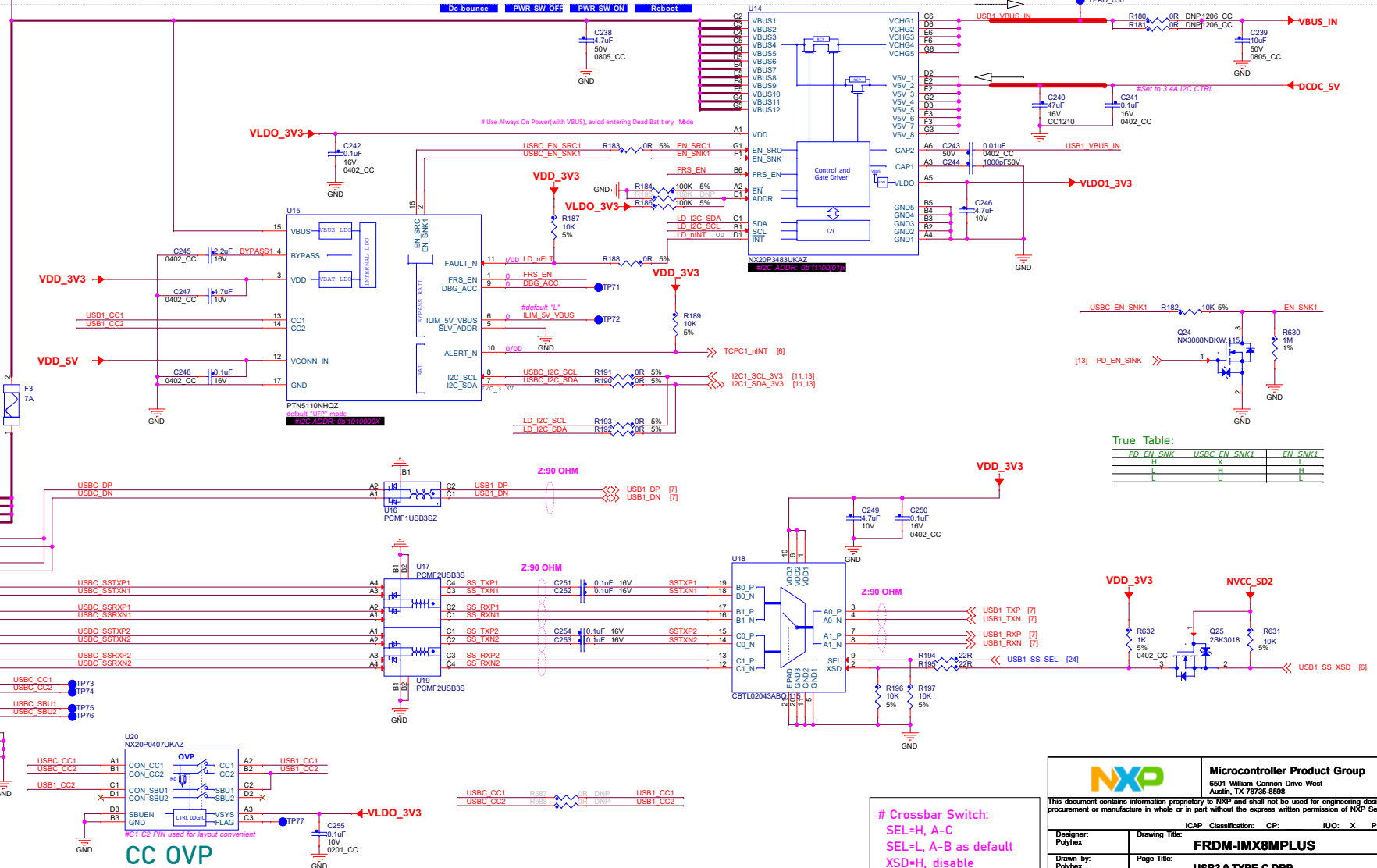
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Designer: Polyhex		Drawing Title: FRDM-IMX8MPLUS	
Drawn by: Polyhex		Page Title: PMIC	
Approved: NXP SE		Size C	Document Number: SCH-95022 PDF: 9PF-95022
Date: Monday, April 21, 2025		Sheet 11 of 27	Rev B1



USB2.0/3.0 C



VBUS DET

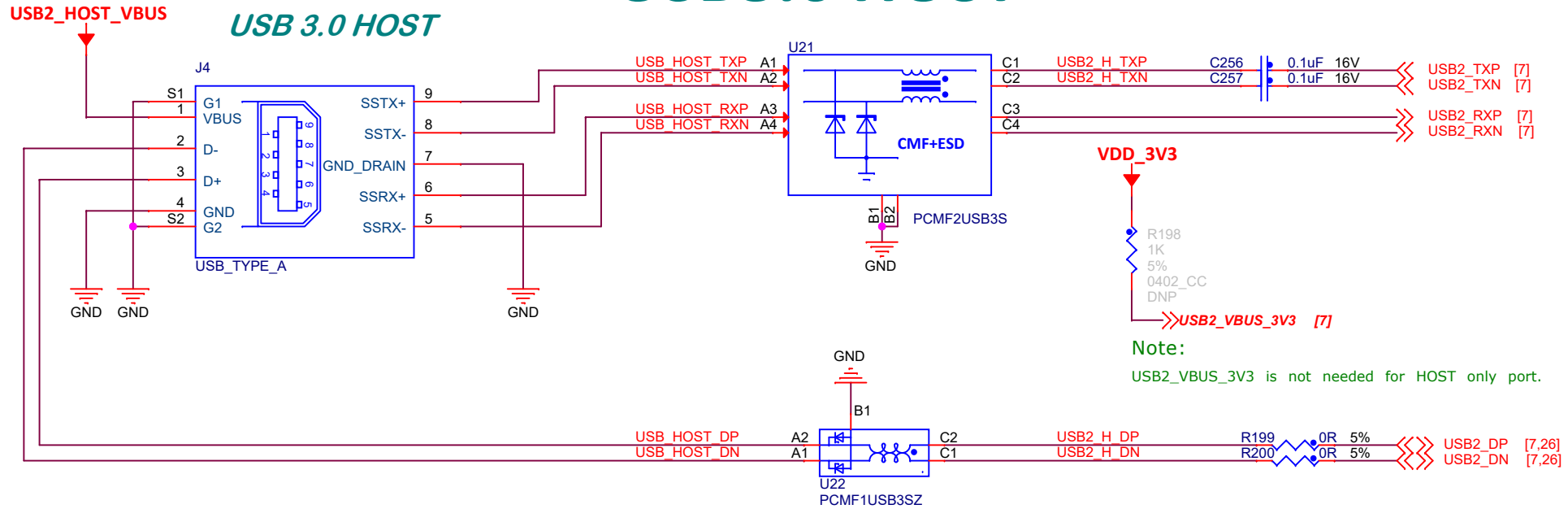


True Table:

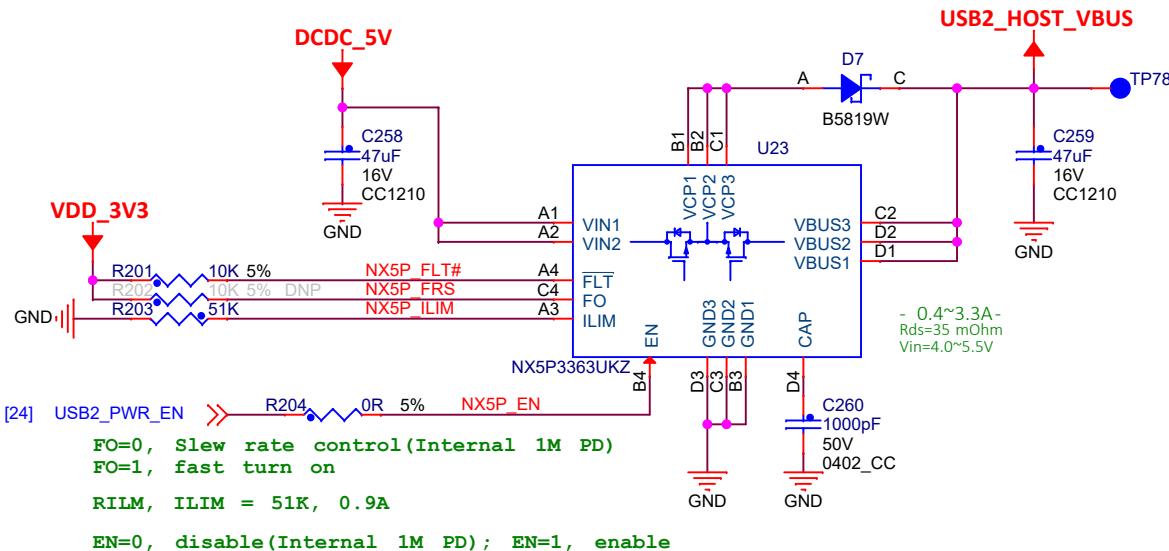
<i>PD_EN_SNK</i>	<i>USBC_EN_SNK1</i>	<i>EN_SNK</i>
H	X	L
L	H	H
L	L	L

- # Crossbar Switch:
 - SEL=H, A-C
 - SEL=L, A-B as default
 - XSD=H, disable
 - XSD=L, enable as default

USB3.0 HOST



5V Source Load Switch



Microcontroller Product Group

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Designer:
Polyhex

Drawing Title:

FRDM-IMX8MPLUS

Drawn by:
Polyhex

Page Title:

USB3.0 HOST

Approved:
NXP SE

Size
A4

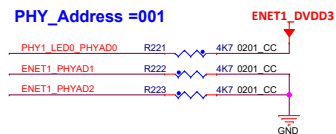
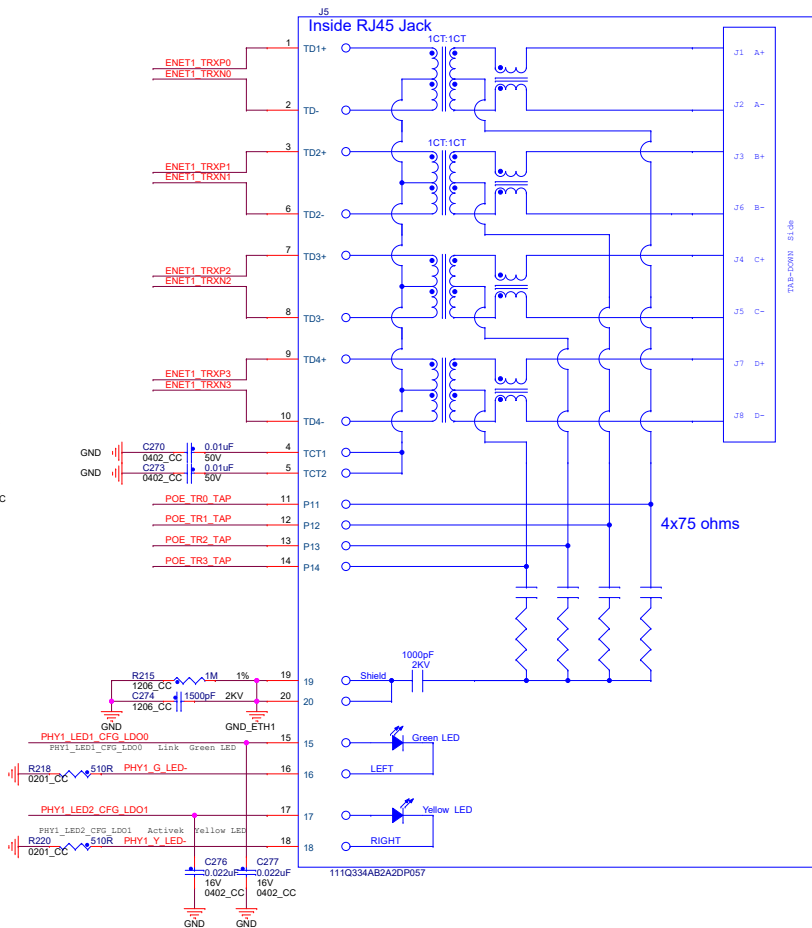
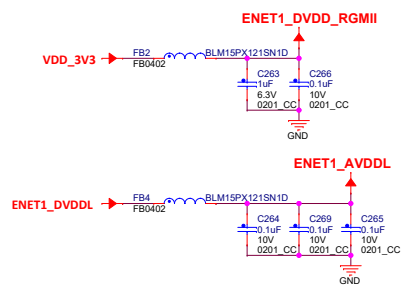
Document Number

SCH-95022 PDF: SPF-95022

Rev
B1

Date: Monday, April 21, 2025

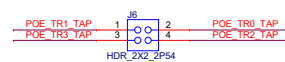
Sheet 15 of 27

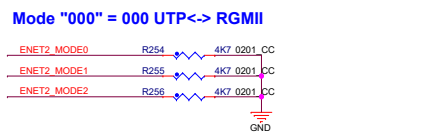
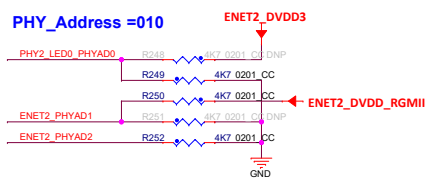
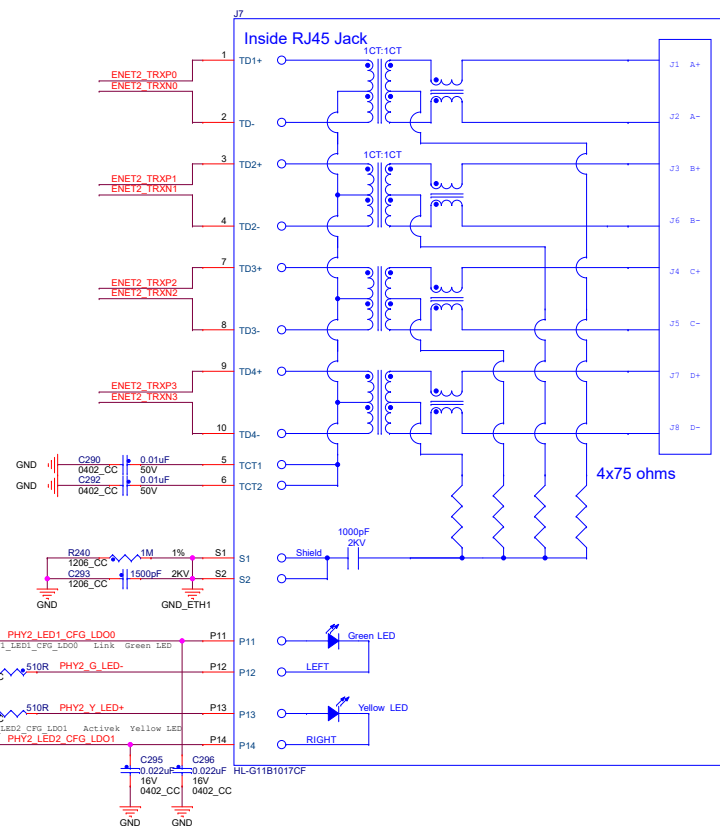


CFG_LDO[1:0] /LED[2:1]	RGMII Voltage
2'b00	1.3V External
2'b01	2.5V Internal
2'b10	1.8V Internal
2'b11	-



	CFG_LDO[1:0]			
YT8521SR-CA	2' b00: 3.3V	2' b01: 2.5V	2' b10: 1.8V	2b'11: 1.8V
RTL8211FSI-CG	2' b00: 3.3V	2' b01: 2.5V	2' b10: 1.8V	2b'11: 1.5V

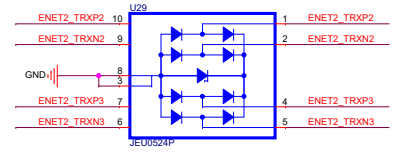





	CFG_LDO[1:0]			
YT8521SH-CA	2' b00: 3.3V	2' b01: 2.5V	2' b10: 1.8V	2b'11: 1.8V
RTL8211FSI-CG	2' b00: 3.3V	2' b01: 2.5V	2' b10: 1.8V	2b'11: 1.5V

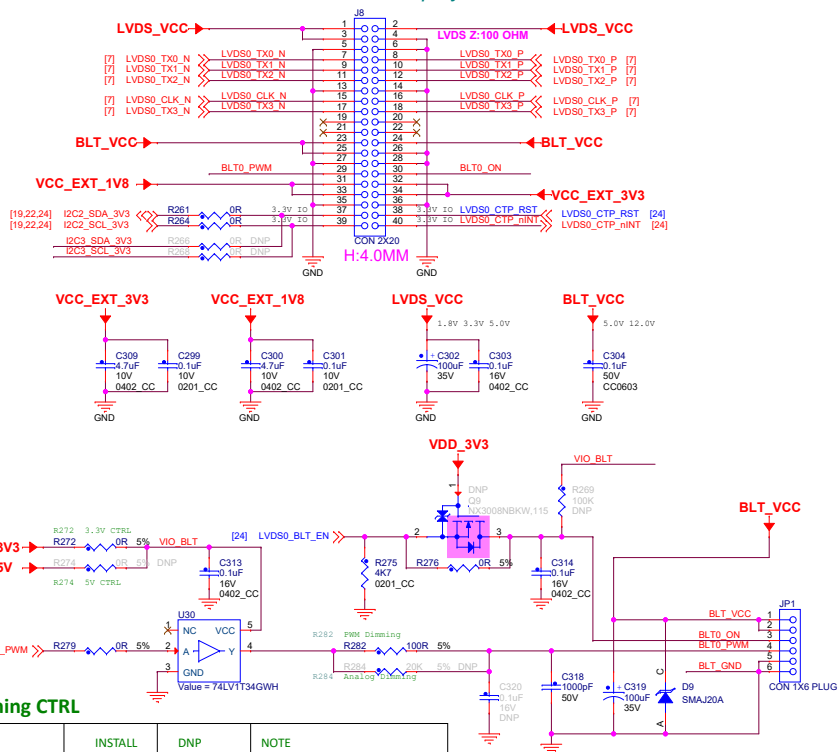
CFG_LED[1:0] /LED[2:1]	RGMIIC Voltage
2'b00	3.3V External
2'b01	2.5V Internal
2'b10	1.8V Internal
2'b11	-

Pin No	Pin Name	Default
23	RXD3/CFG MODE2	0
24	RXD2/CFG MODE1	0
25	RXD1/CFG MODE0	0
26	RXD0/RXDLY	1
27	RX DV/PHYAD2	0
28	RX CLK/PHYAD1	1
35	LED0/PHYAD0	0
36	LED1/CFG LDO0	0
37	LED2/CFG LDO1	1



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Designer: Polytech	Drawing Title: FRDM-IMX8MPLUS				
Drawn by: Polytech	Page Title: Giga Ethernet2 TSN				
Approved: NXD SE	Size C	Document Number SCH-95022 DocID: SPF-95022			Rev B1
Date: Monday, April 21, 2025		Sheet 17	of 27		

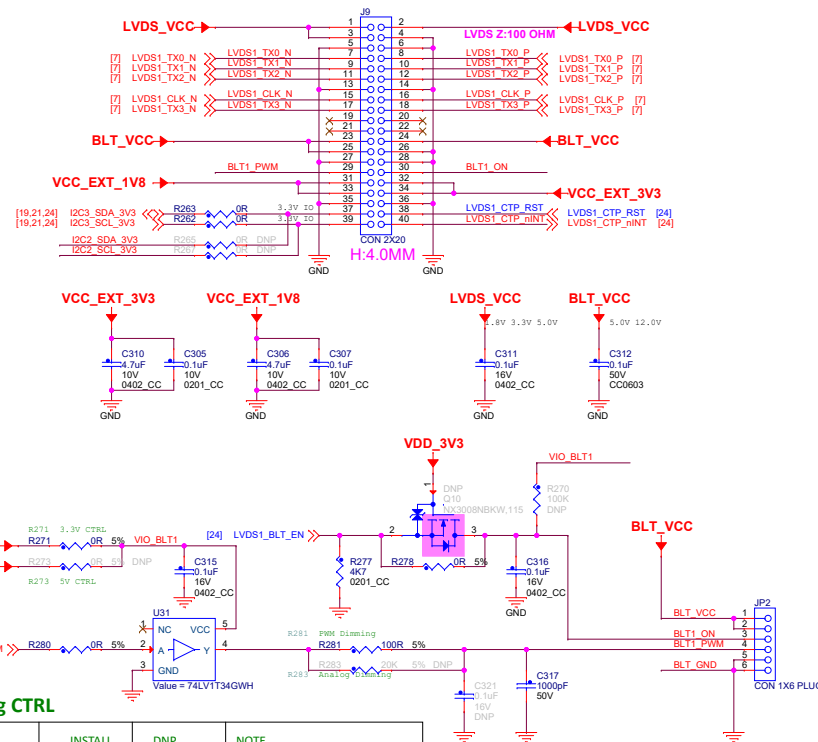
LVDS0 Display



Dimming CTRL

ITEM	INSTALL	DNP	NOTE
3.3V PWM Dimming	R272, R282	R274, R284, C320	PWM frequency according SPEC
5.0V PWM Dimming	R274, R282	R272, R284, C320	PWM frequency according SPEC
3.3V Analog Dimming	R274, R282	R272, R282	0<Vadj<3.3V
5.0V Analog Dimming	R274, R284, C320	R272, R282	0<Vadj<5.0V

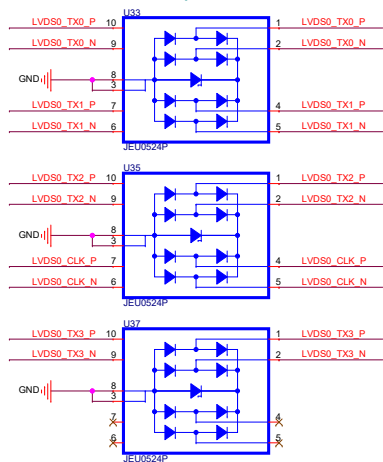
LVDS1 Display



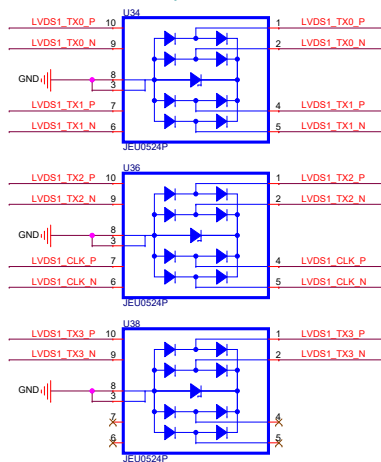
Dimming CTRL

ITEM	INSTALL	DNP	NOTE
3.3V PWM Dimming	R271, R281	R273, R283, C321	PWM frequency according SPEC
5.0V PWM Dimming	R273, R281	R271, R283, C321	PWM frequency according SPEC
3.3V Analog Dimming	R273, R281, C321	R271, R281	0<Vadj<3.3V
5.0V Analog Dimming	R273, R283, C321	R271, R281	0<Vadj<5.0V

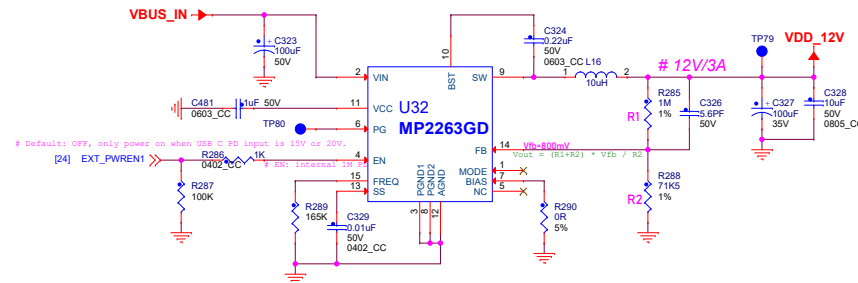
ESD protection



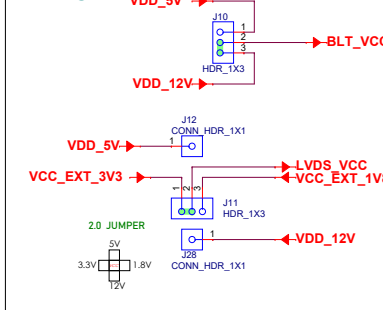
ESD protection




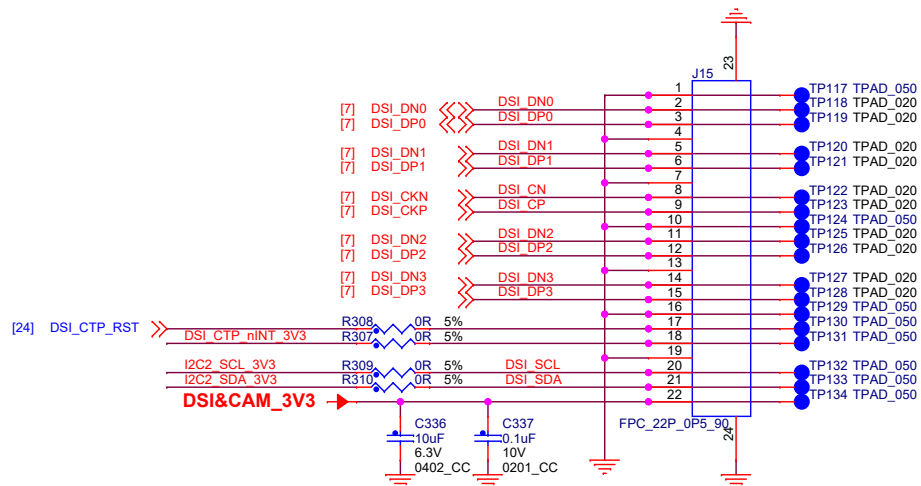
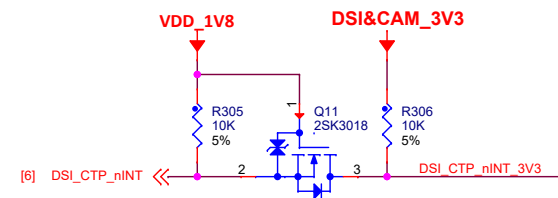
12V PWR




PWR SEL

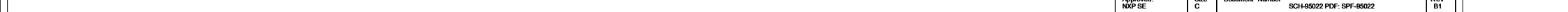
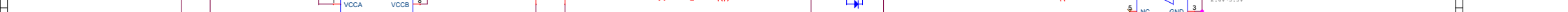
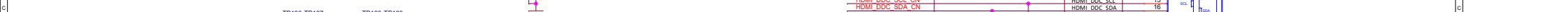


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Designer: Polyhex	Drawing Title: FRDM-IMX8MPLUS		
Drawn by: Polyhex	Page Title: LVDS0/1		
Approved: NXP SE	Size C	Document Number SCH-95022 PDF: SPF-95022	Rev B1
Date: Monday, April 21, 2025	Sheet 18	of 27	

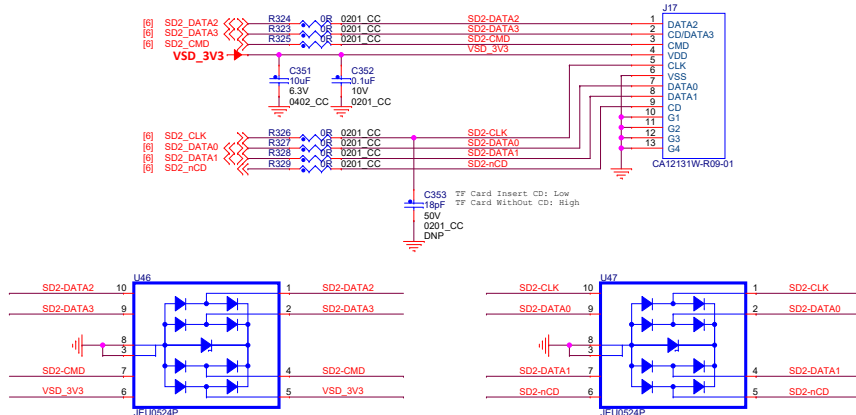


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Designer: Polyhex	Drawing Title: FRDM-IMX8MPLUS		
Drawn by: Polyhex	Page Title: MPi CSI1/CSI2/DSI		
Approved: NXP SE	Size B	Document Number SCH-95022 PDF: SPF-95022	Rev B1
Date: Monday, April 21, 2025		Sheet 19 of 27	

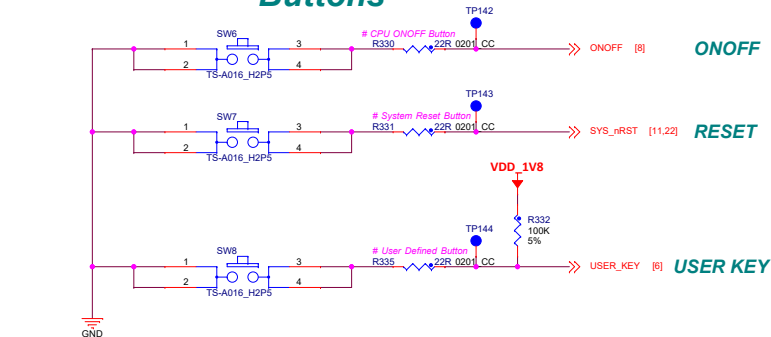
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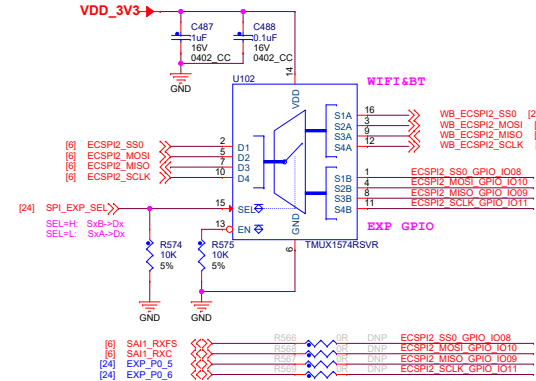
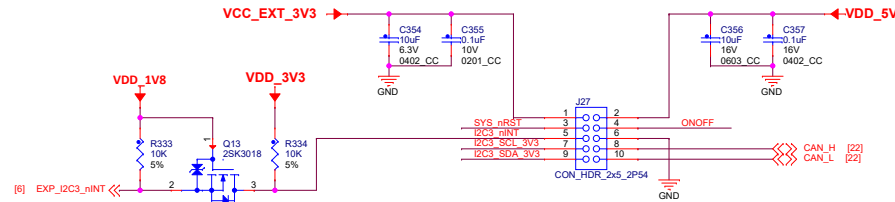
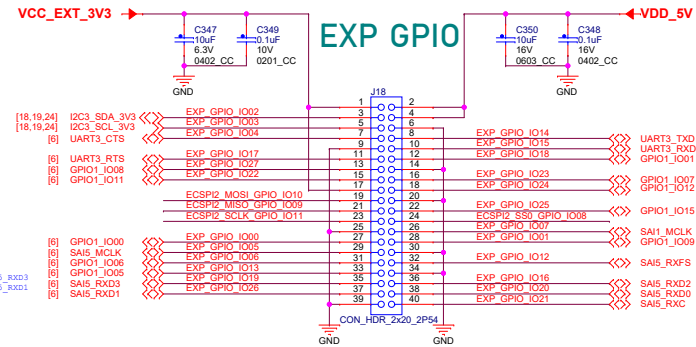
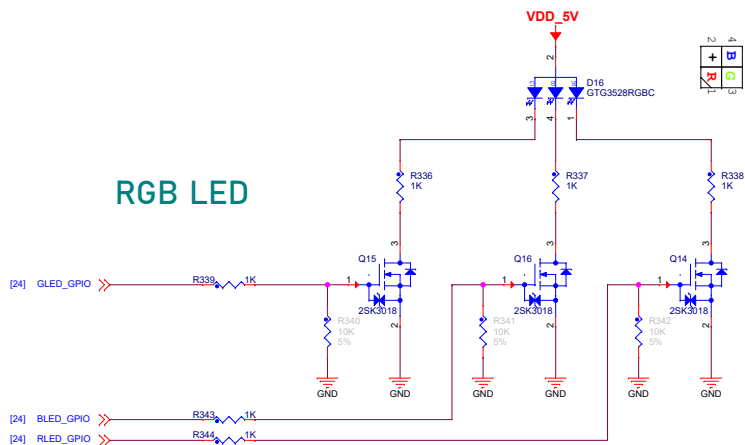
TF Card Slot



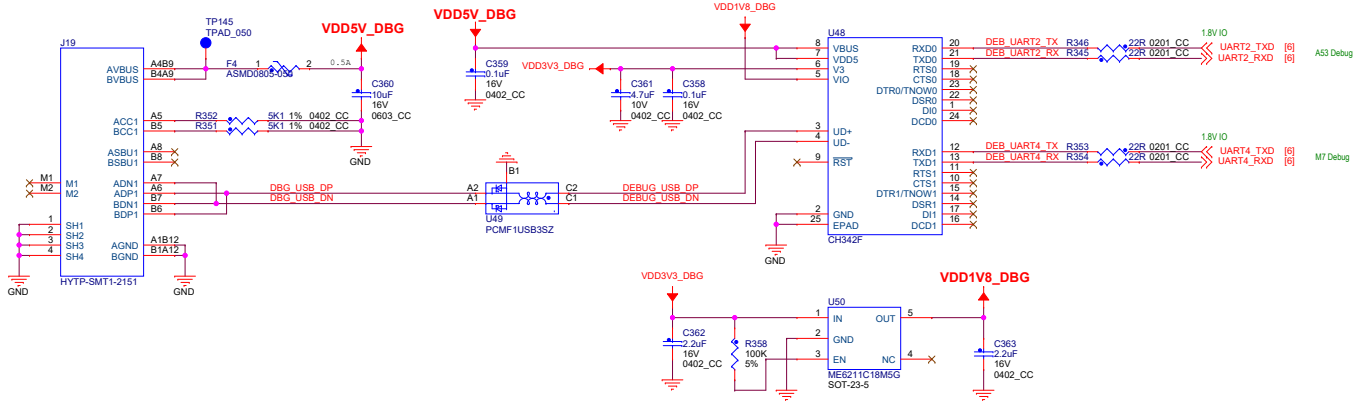
Buttons



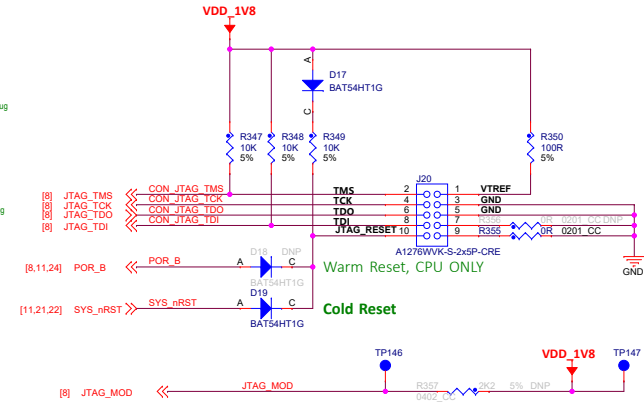
RGB LED



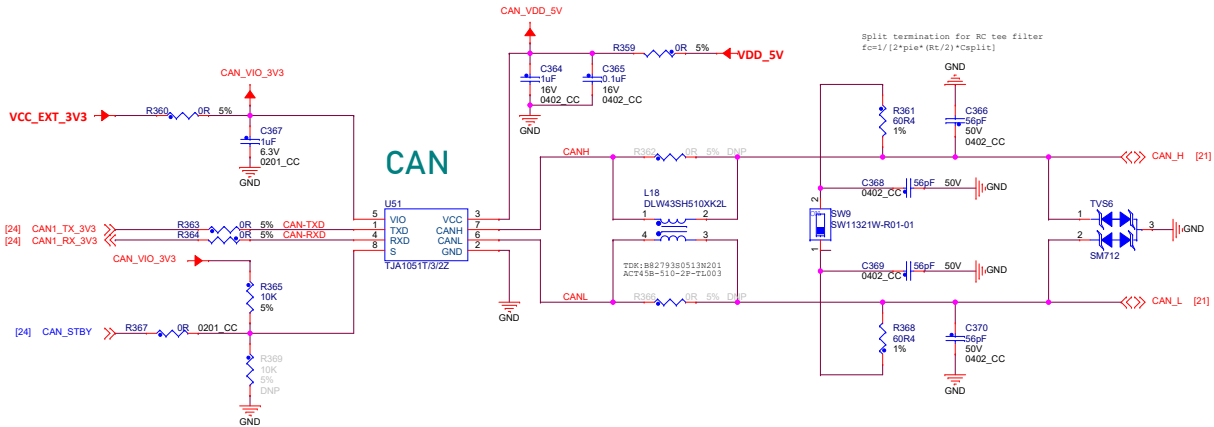
Debug



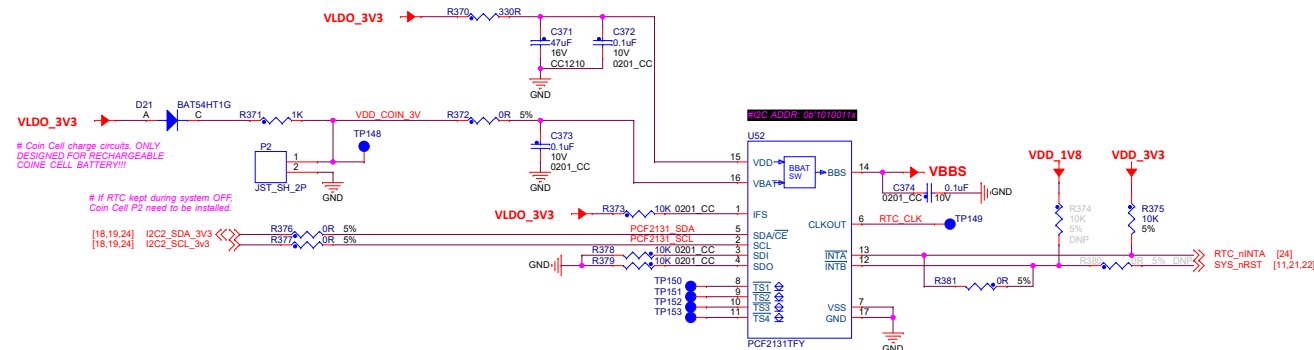
JTAG Interface




CAN



RSUP and CSUP: An appropriate RC filter needs to be added to guarantee the chip will only see <0.35 Vrms ramp down rate on supply, even if Vdd in ramp rate is very high.



Coin Cell charge circuits, ONLY DESIGNED FOR RECHARGEABLE COIN CELL BATTERY!!

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Designer: Polyhex	Drawing Title: FRDM-IMX8MPLUS		
Drawn by: Polyhex	Page Title: DEBUG/JTAG/CAN/RTC		
Approved: NXP SE	Size C	Document Number SCH-95022 PDF: SPF-95022	Rev B1
Date:	Monday, April 21, 2025		Sheet 22 of 27

CODEC

DCVDD	1.62V - 2.0V
DBVDD	1.62V - 3.6V
MICVDD	1.70V - 3.6V
AVDD	1.70V - 2.0V
PLLVDD	1.70V - 2.0V
CPVDD	1.70V - 2.0V
SPKVDD	1.70V - 5.5V

U53 WM8962BECSN/R

Zobel Networks: close to WM8962B

HP JACK

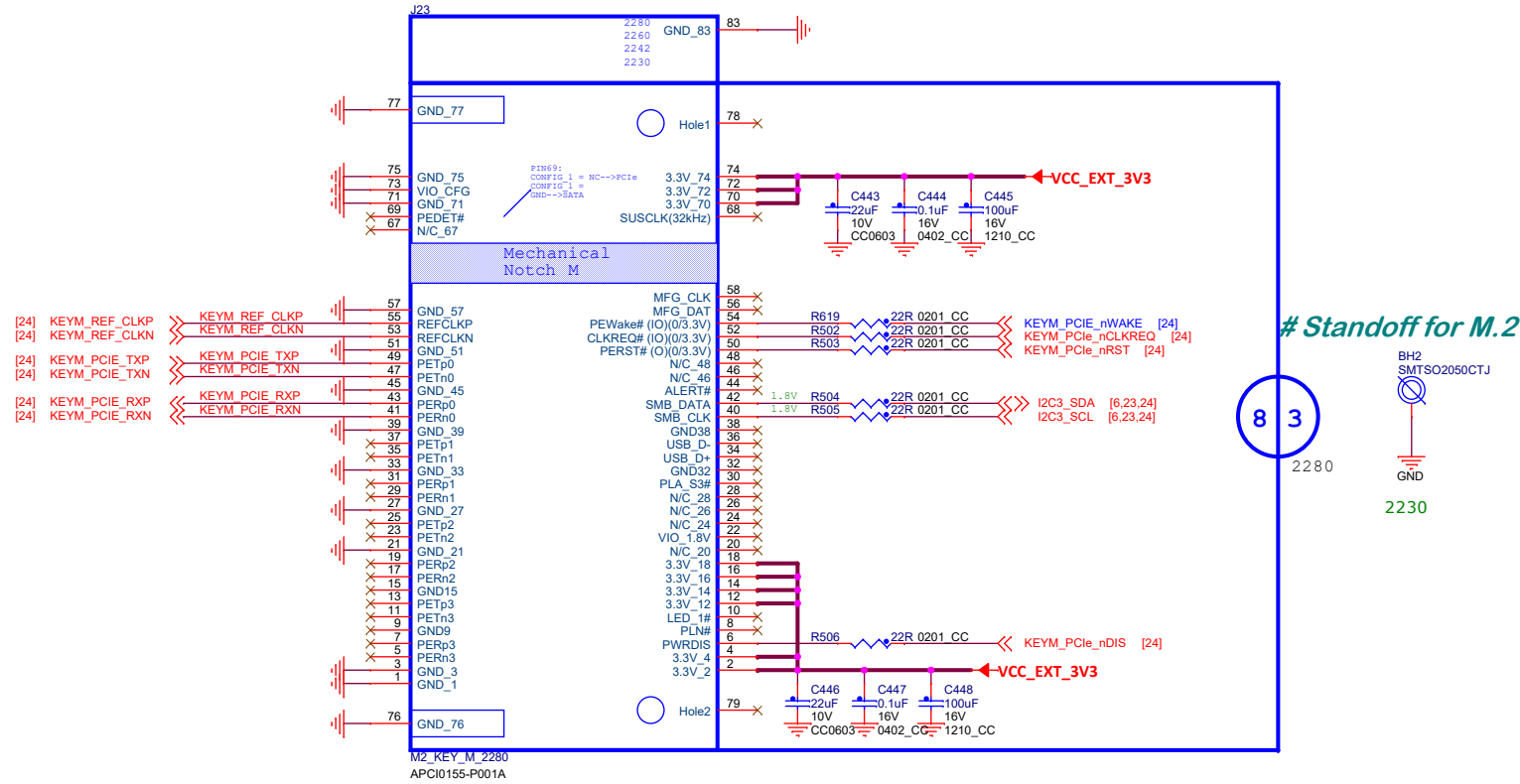
5V SPK PWR Source Load Switch


SPK CN

HP MIC

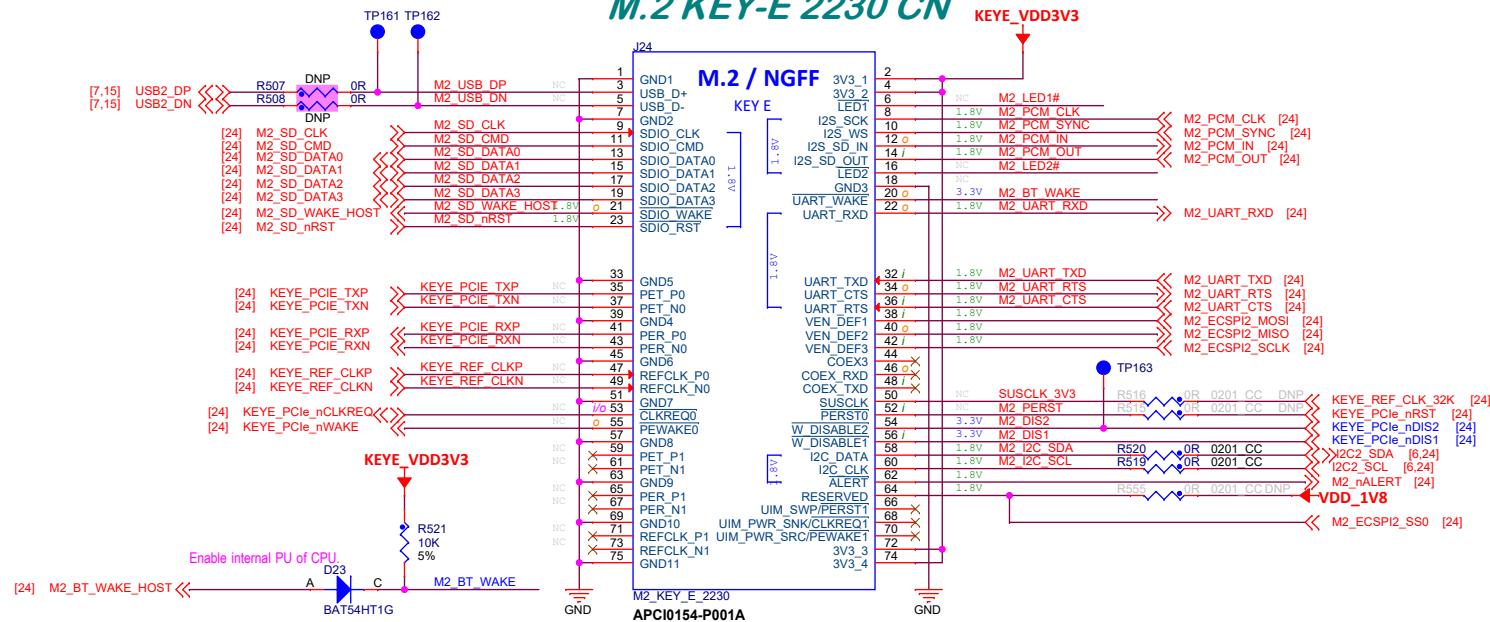
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Designer: Polyhex	Drawing Title: FRDM-IMX8MPLUS		
Drawn by: Polyhex	Page Title: Audio CODEC		
Approved: NXP SE	Size C	Document Number SCH-95022 PDF: SPF-95022	Rev B1
Date: Monday, April 21, 2025	Sheet 23	of 27	

M.2 KEY-M 2280 CN

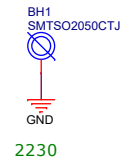


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Designer: Polyhex	Drawing Title: FRDM-IMX8MPLUS		
Drawn by: Polyhex	Page Title: M.2 KEY-M PCIe3.0		
Approved: NXP SE	Size A3	Document Number SCH-95022 PDF: SPF-95022	Rev B1
Date: Monday, April 21, 2025		Sheet 25 of 27	

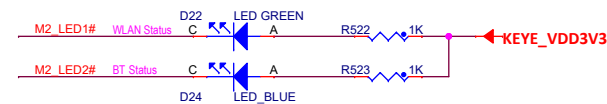
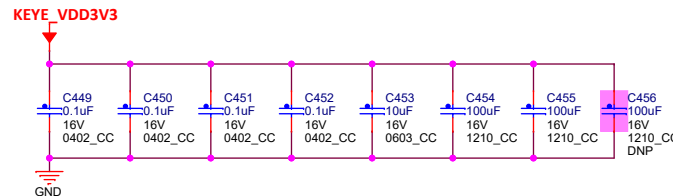
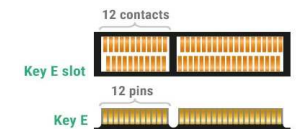
M.2 KEY-E 2230 CN



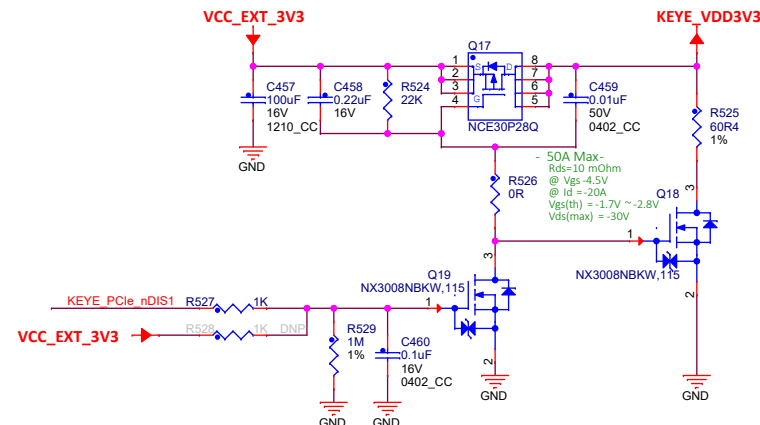
Standoff for M.2




KEYE_PCl_e_nDIS2,BT_INDEPENDENT_RESET
KEYE_PCl_e_nDIS1,WIFI&BT_Module_Power-down



M.2 KEY-E PWR



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Drawn by: Polyhex	Page Title: M.2 KEY-E WIFI/BT		
Approved: NXP SE	Size A3	Document Number SCH-95022 PDF: SPF-95022	Rev B1
Date:	Monday, April 21, 2025	Sheet 26 of 27	

