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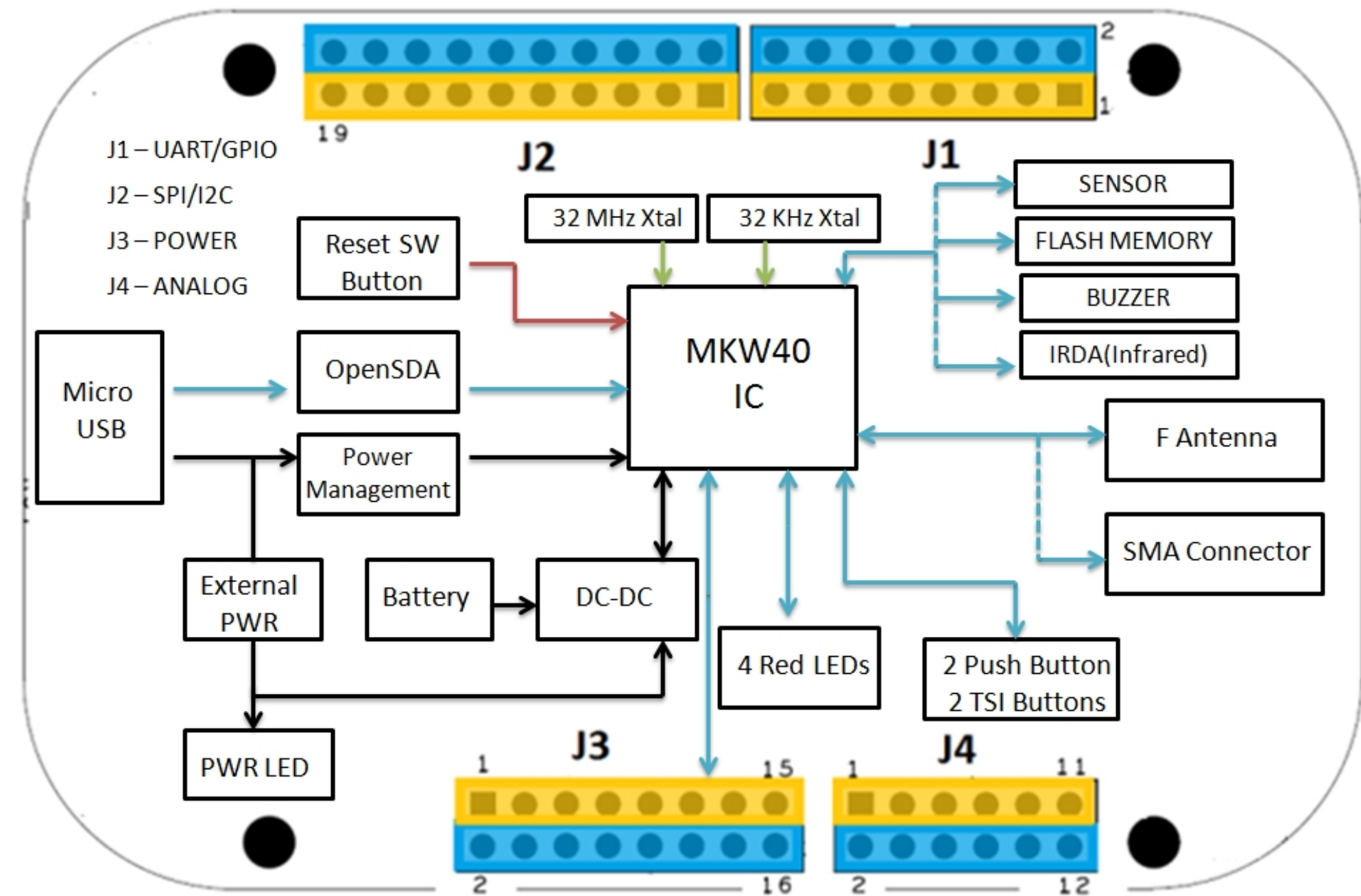
Revisions & Change Log

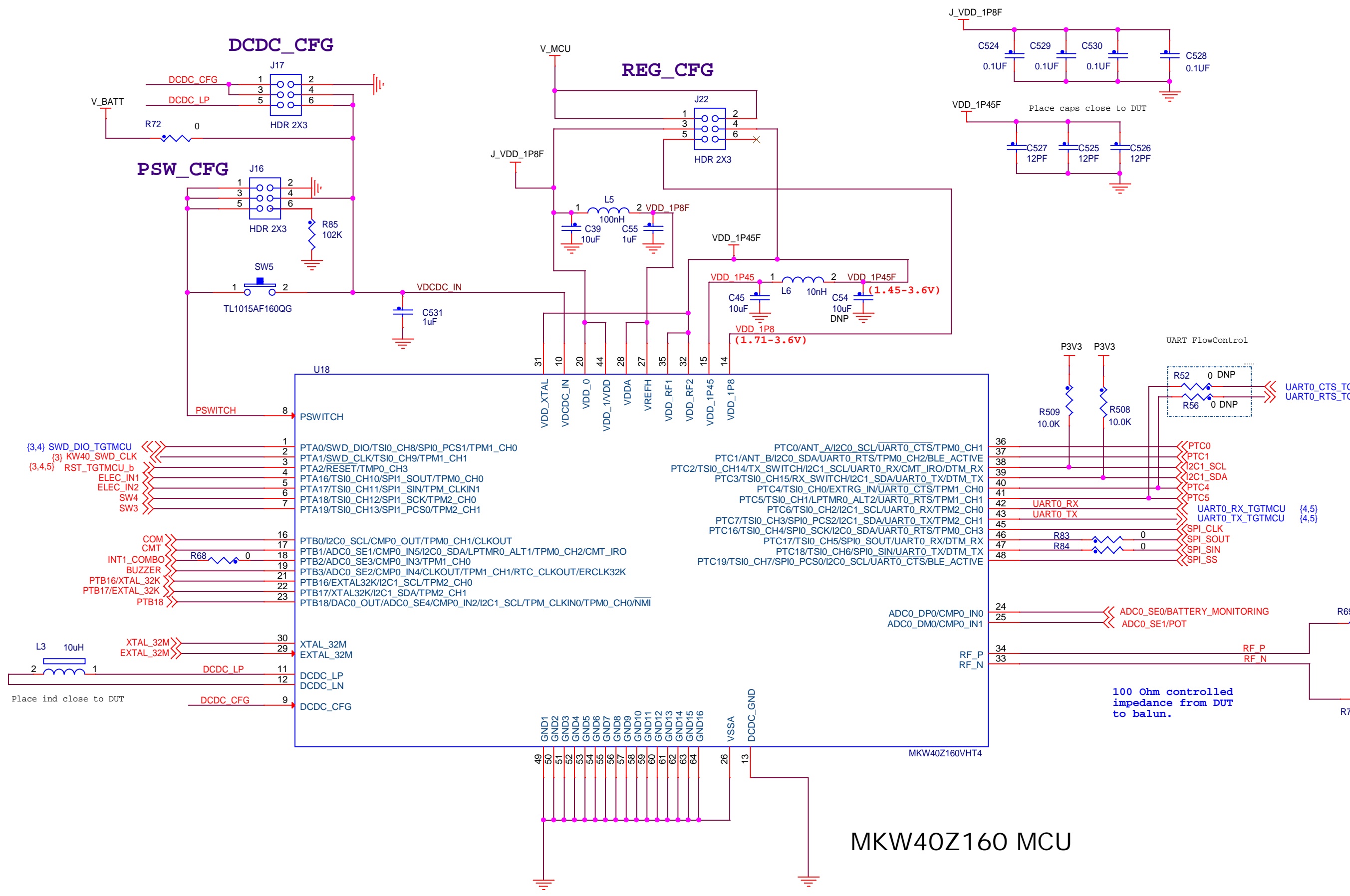
Rev	Description	Date	Approved
X1	Initial Draft	05/9/14	A. QUIROZ
X2	DCDC Jumper Sets FXOS8700CQ Accel RF Balun matching	05/19/14	A. QUIROZ
	BOM Optimization, Adding TP for Testing	05/23/14	A. QUIROZ
A	Prototype Release	07/08/14	A. QUIROZ
B	Update BOM, SPI Flash Memory	11/18/14	A. QUIROZ
B3	Update RF BOM, Adding DCDC capacitor	04/06/15	A. QUIROZ
C	Update headers and PokaYokes	7/30/15	

FREEDOM KW40Z BLE/Zigbee

		Wireless Connectivity Operation	
		6501 William Cannon Drive West Austin, TX 78735-8588	
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Designer: A. QUIROZ		ICAP Classification: FCP: FIUO: PUBI: X	
Drawing Title: A. QUIROZ		X-FRDM-KW40Z	
Drawn by: A. QUIROZ		Page Title: TITLE PAGE	
Approved: L. KELVIN		Size C	Document Number SCH-28379 PDF: SPF-28379
Date: Thursday, July 30, 2015		Sheet 1	of 5

- Unless Otherwise Specified:
 All resistors are in ohms, 5%, 1/8 Watt
 All capacitors are in uF, 20%, 50V
 All voltages are DC
 All polarized capacitors are aluminum electrolytic
- Interrupted lines coded with the same letter or letter combinations are electrically connected.
- Device type number is for reference only. The number varies with the manufacturer.
- Special signal usage:
 _B Denotes - Active-Low Signal
 <> or [] Denotes - Vectored Signals
- Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

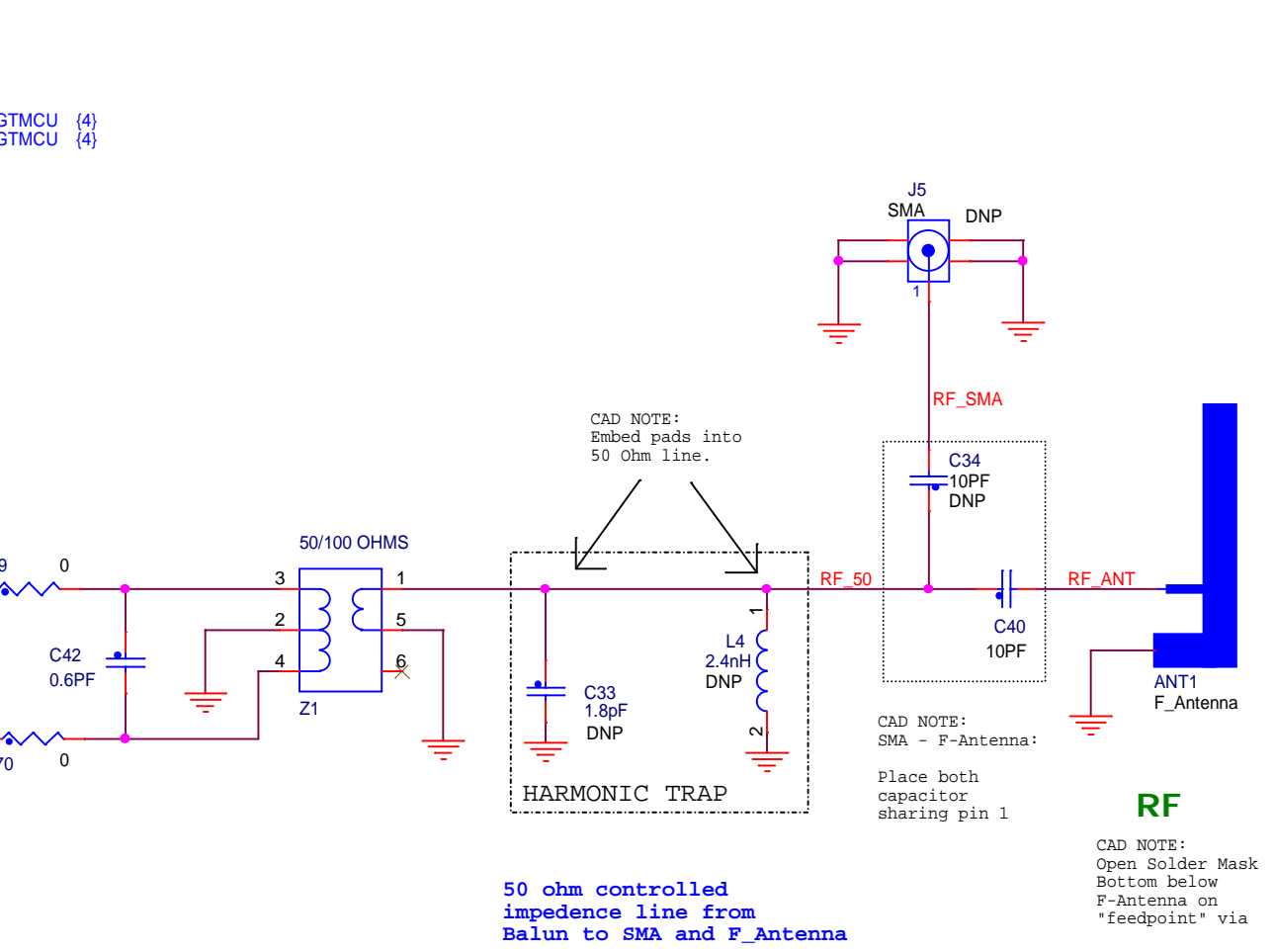




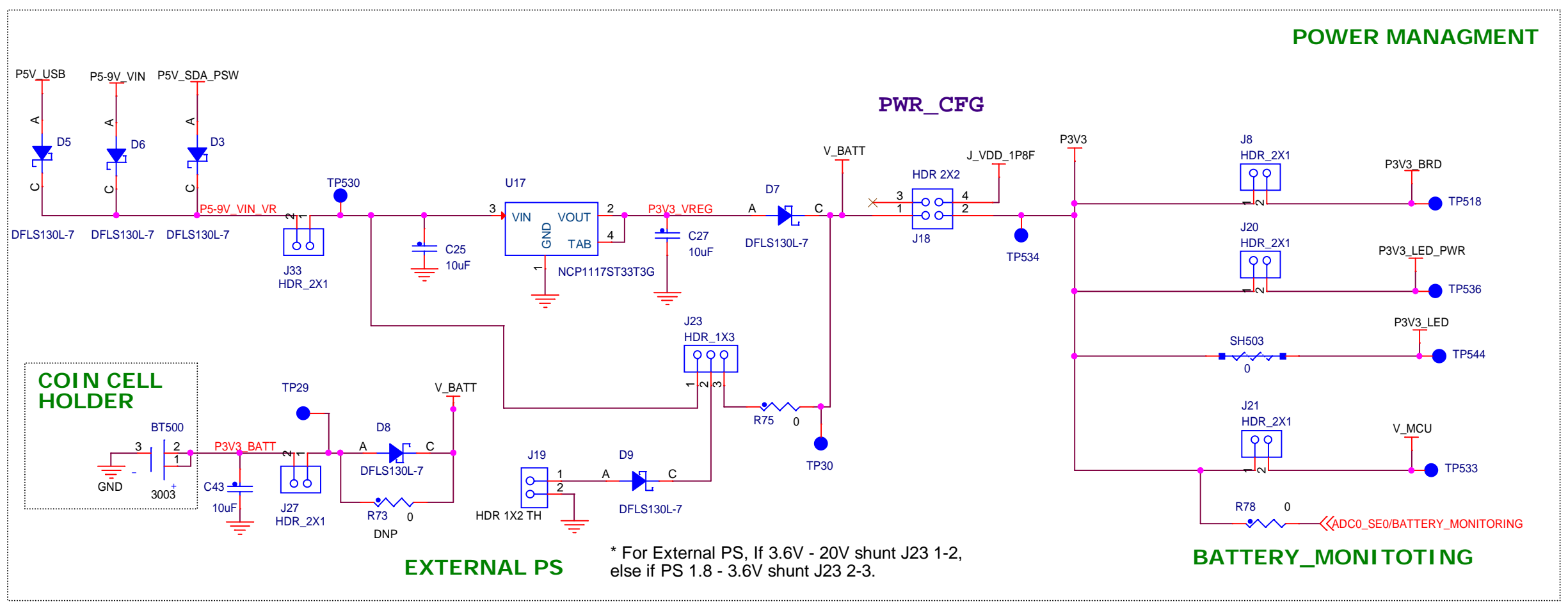
MKW40Z160 MCU

Power Configuration

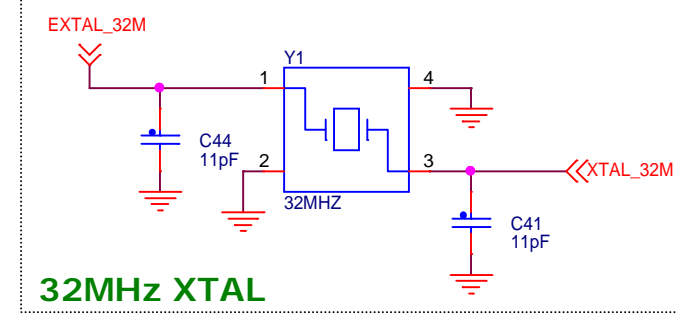
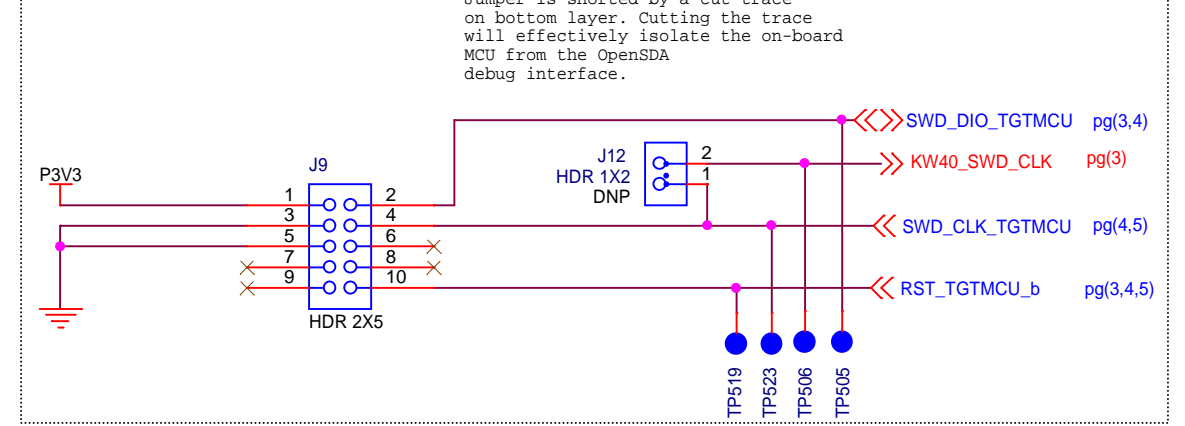
	PWR_CFG J18	PSW_CFG J16	DCDC_CFG J17	REG_CFG J22
Bypass (1.8V - 3.6V)	1-2	1-2	3-4	1-3 2-4
Buck (1.8V - 4.2V) - Coin Cell	2-4	5-6	3-4	3-5
Boost Auto Mode (1.8V - 4.2V)	2-4	3-4	3-4	3-5
Boost (0.9V - 1.8V) - Single battery	2-4	3-4	1-2 5-6	3-5



POWER MANAGEMENT



SWD CONNECTOR



freescale

ICAP Classification: FCP: _____ FIUO: _____ PUBI: X

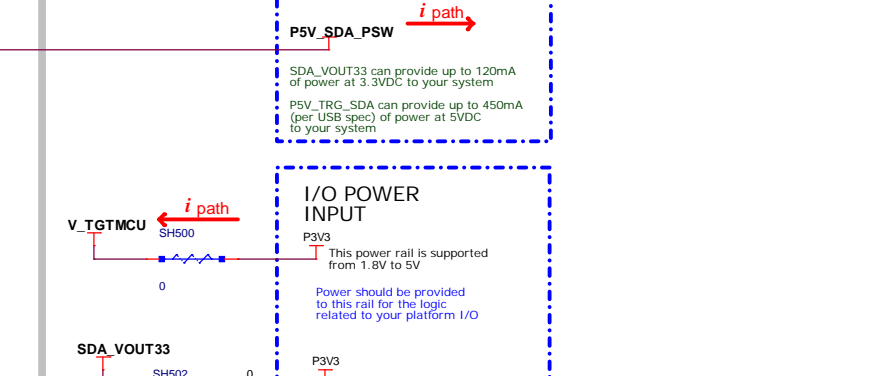
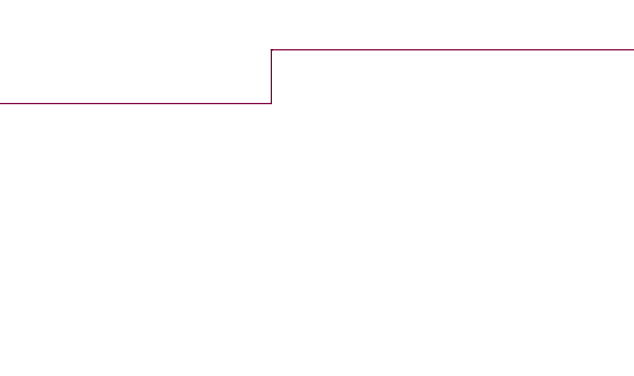
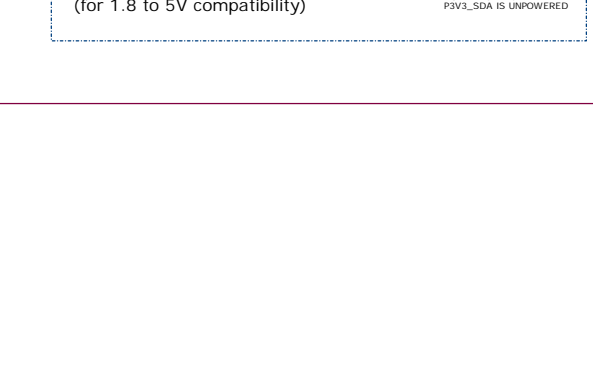
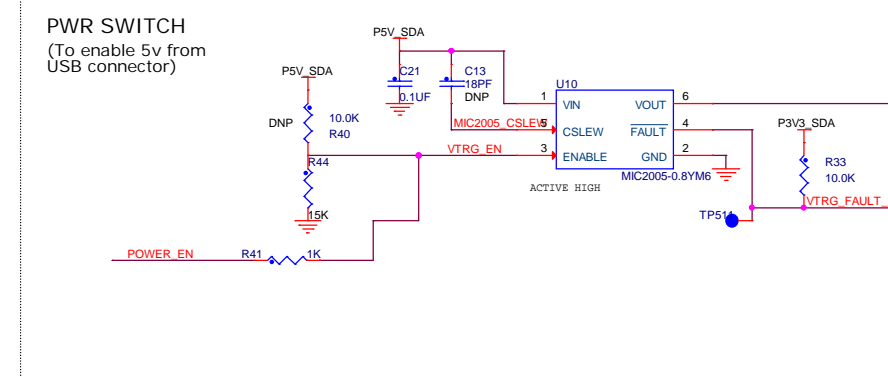
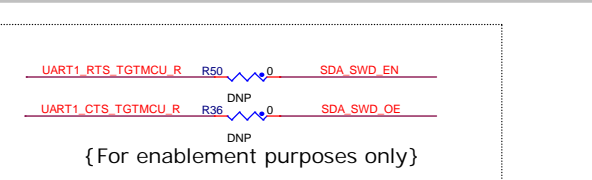
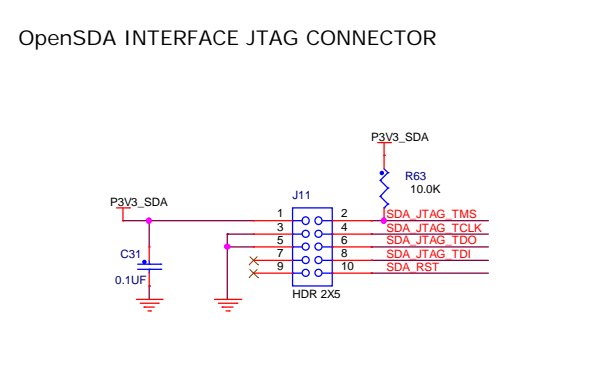
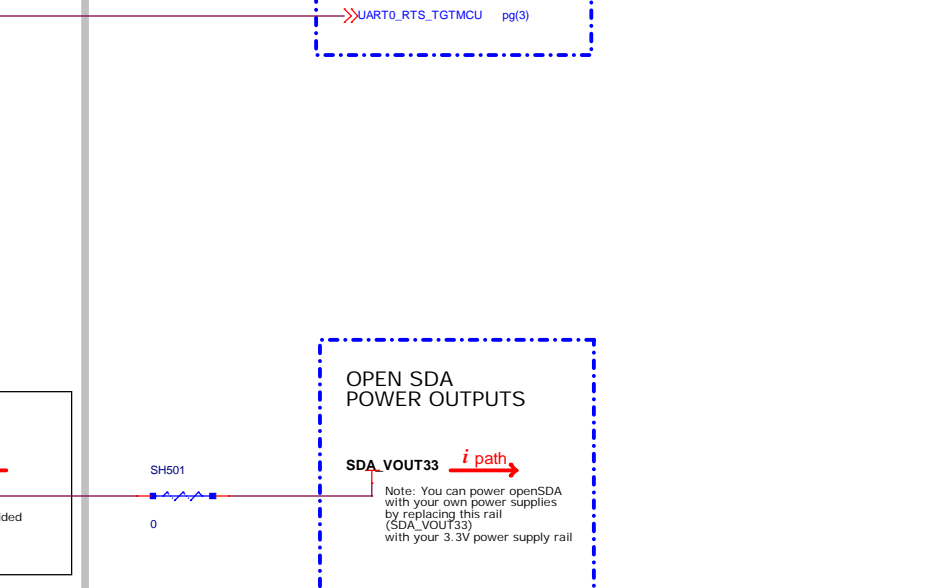
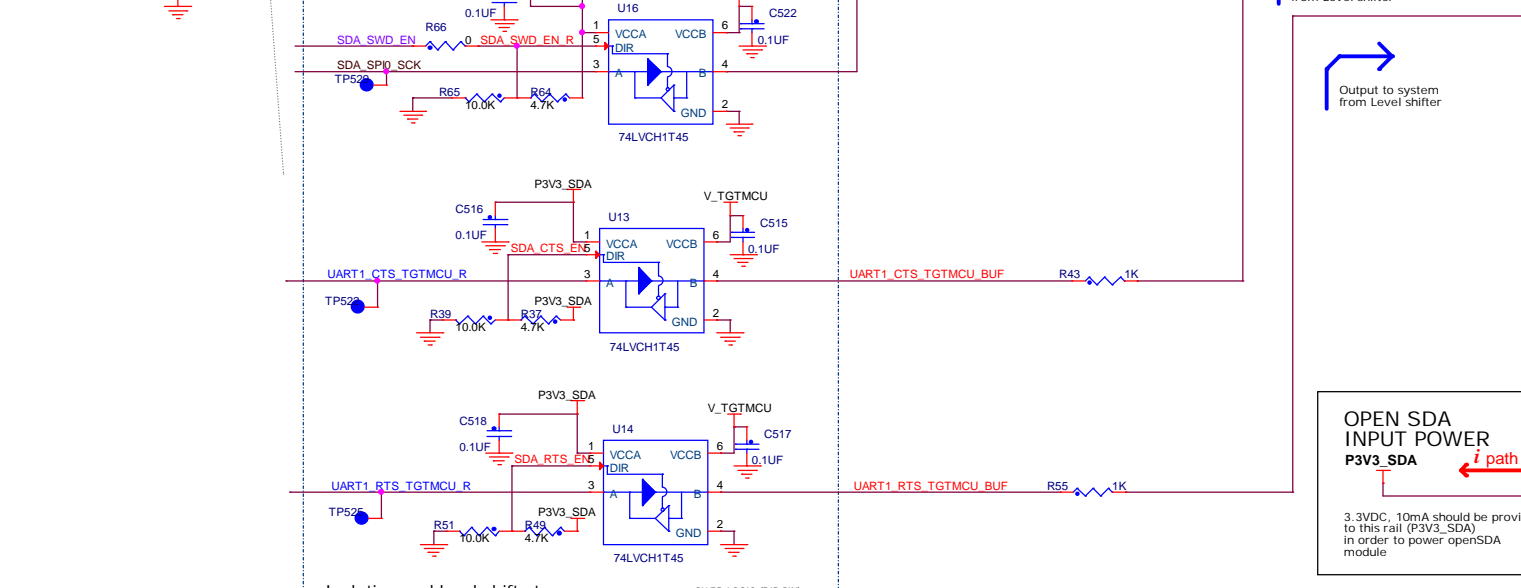
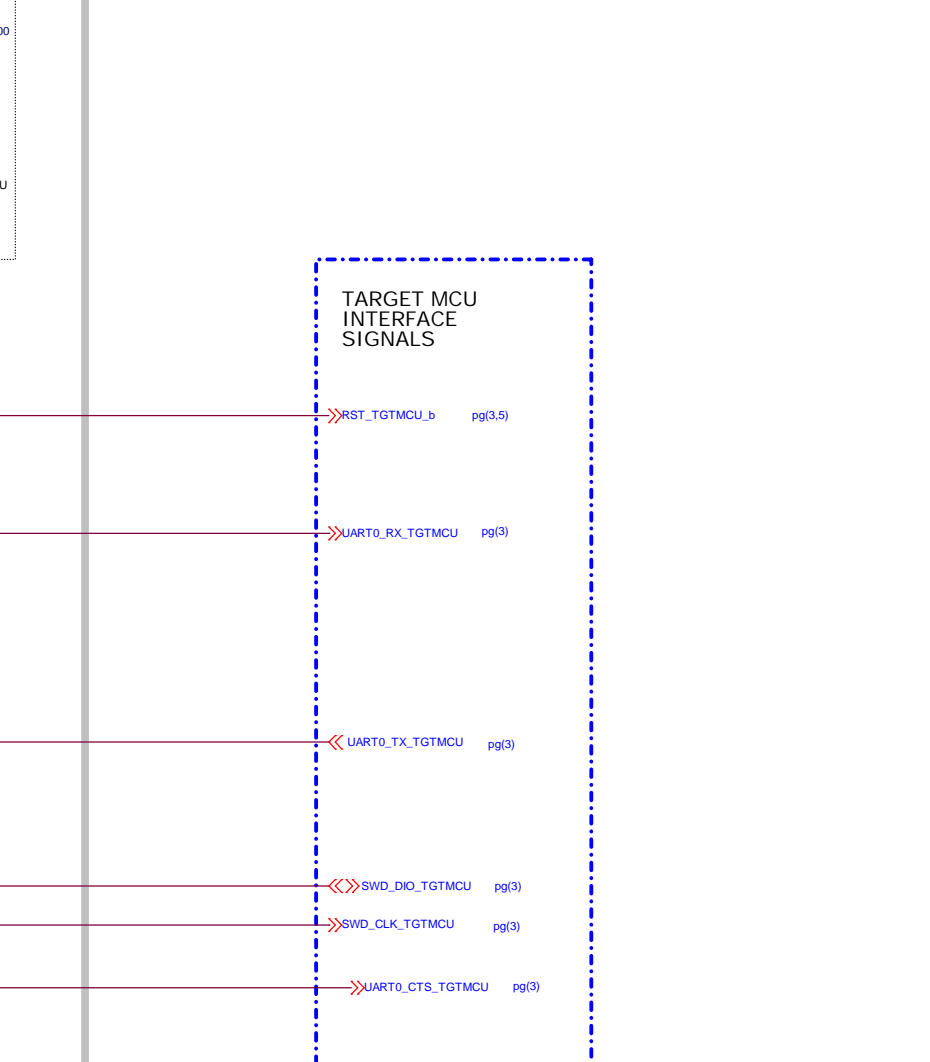
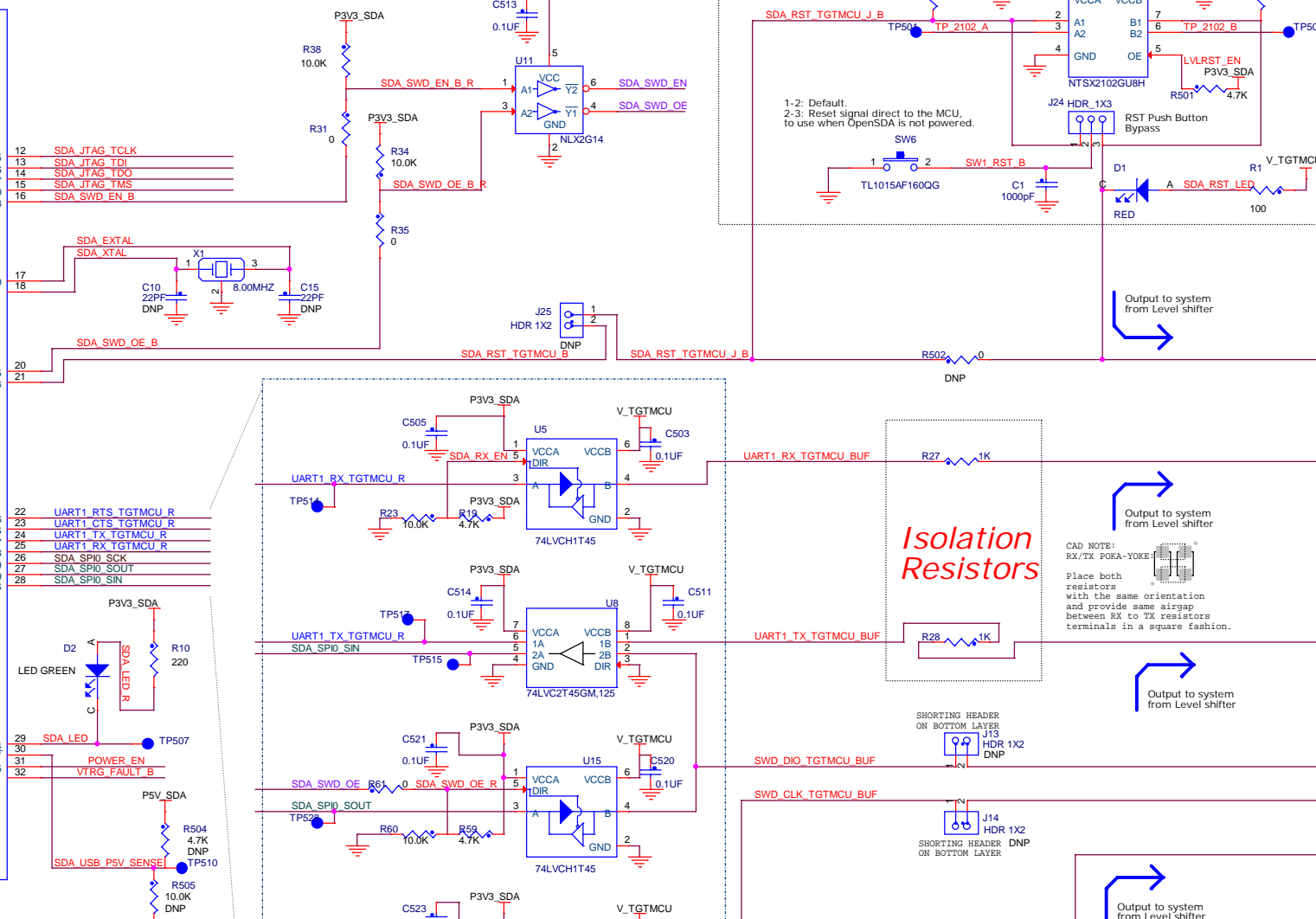
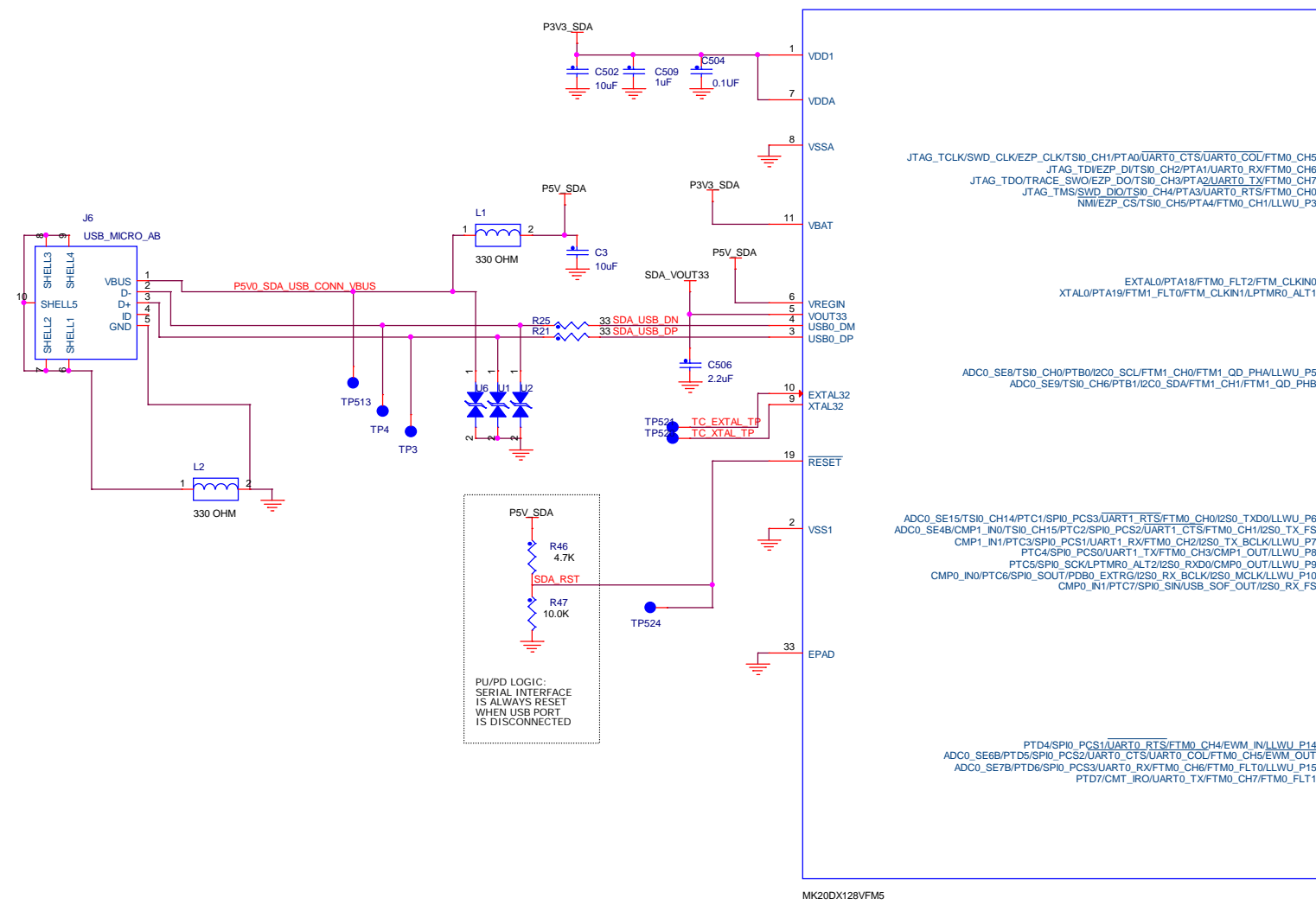
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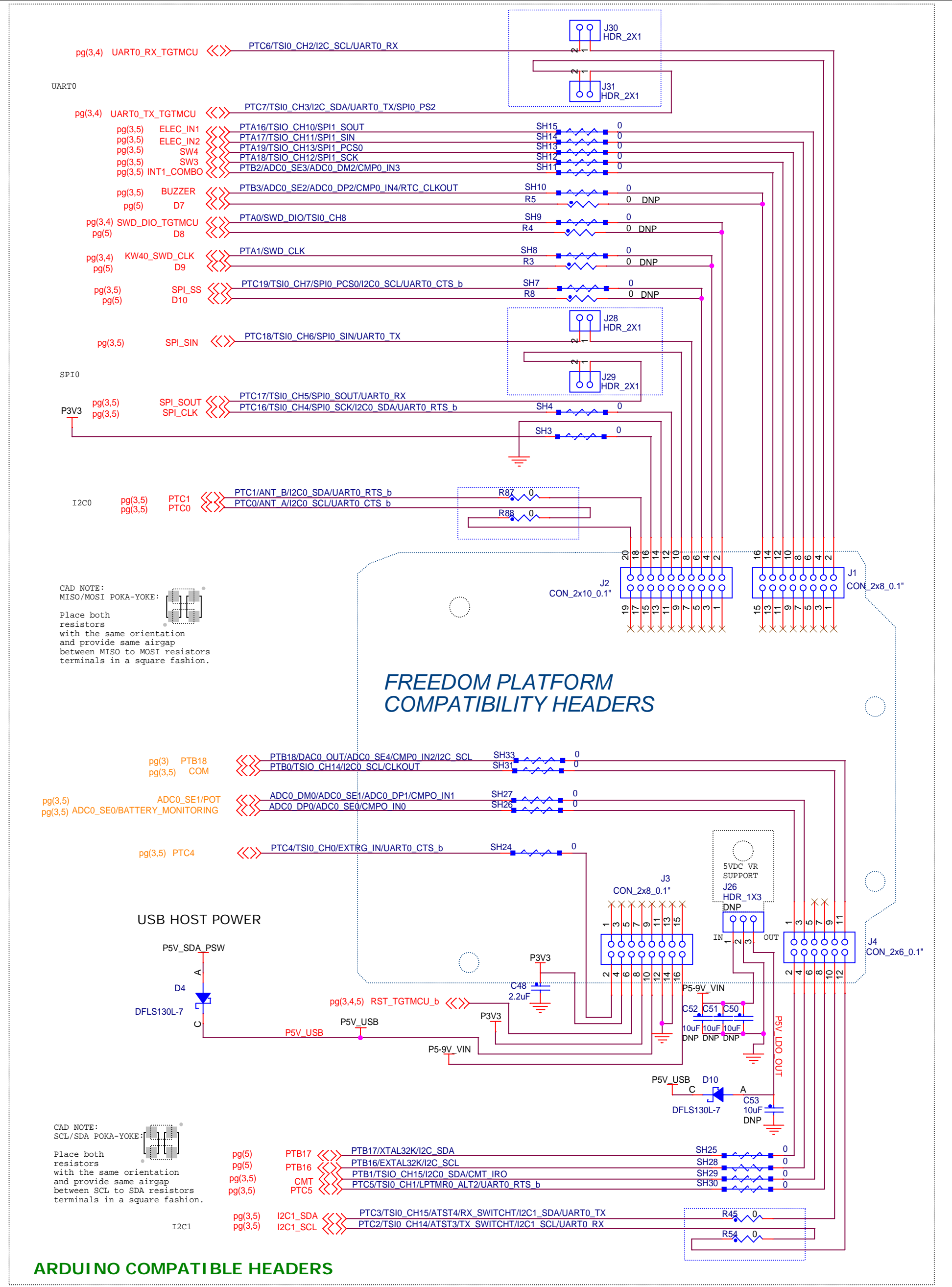
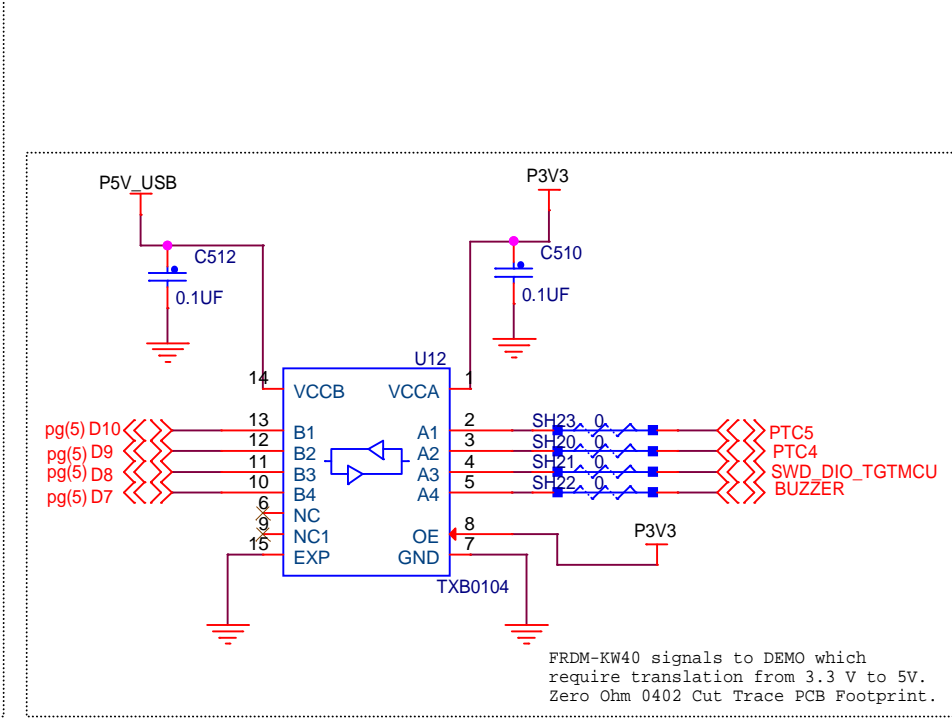
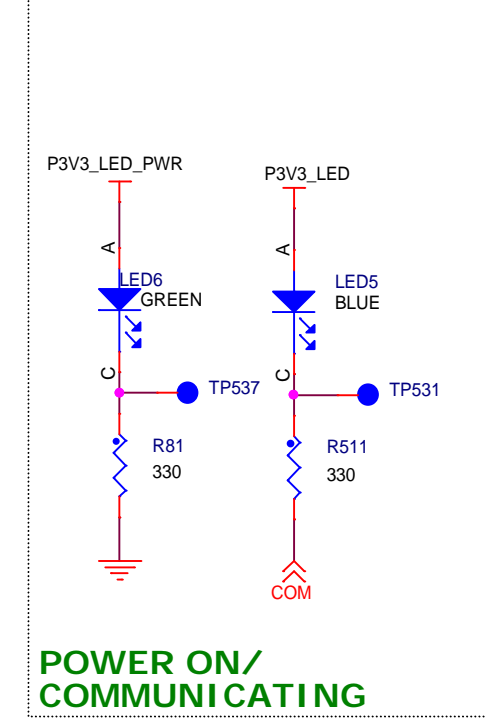
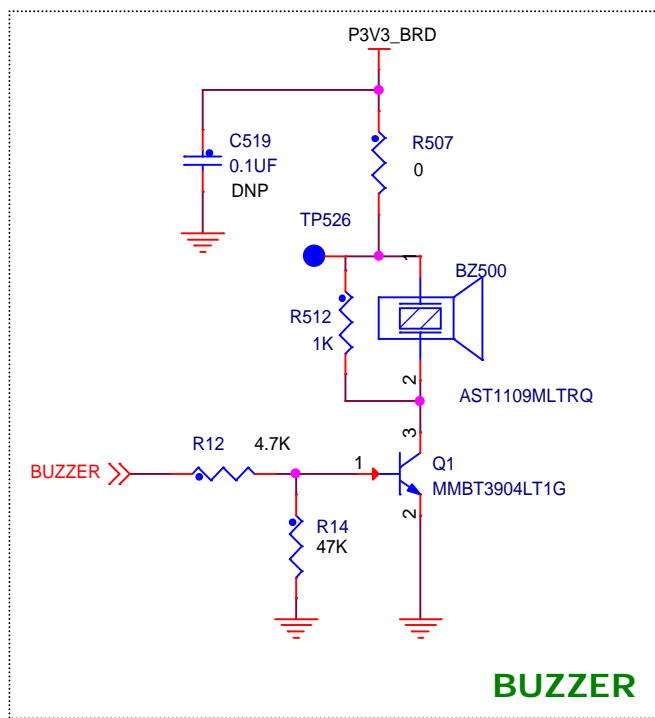
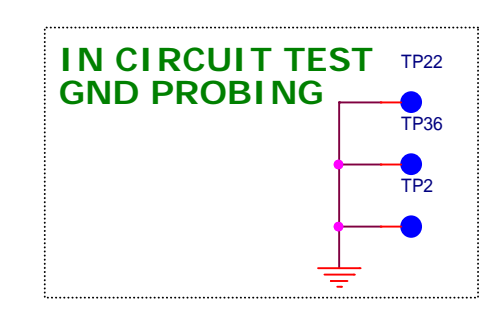
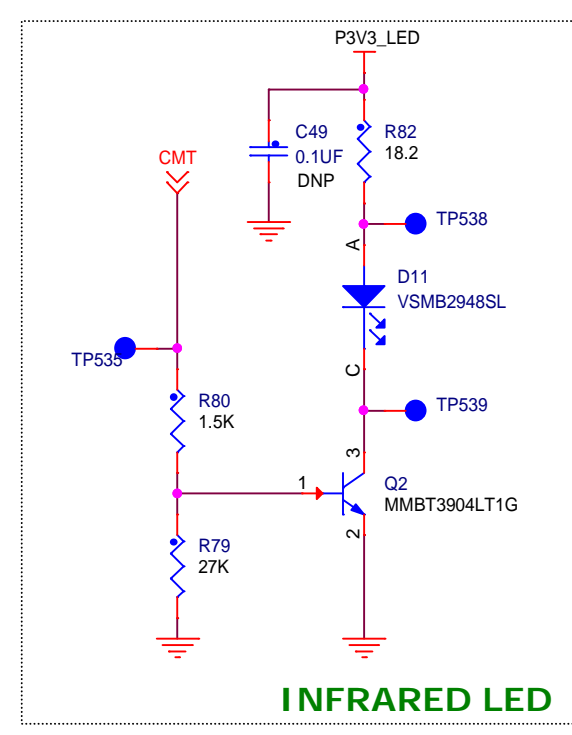
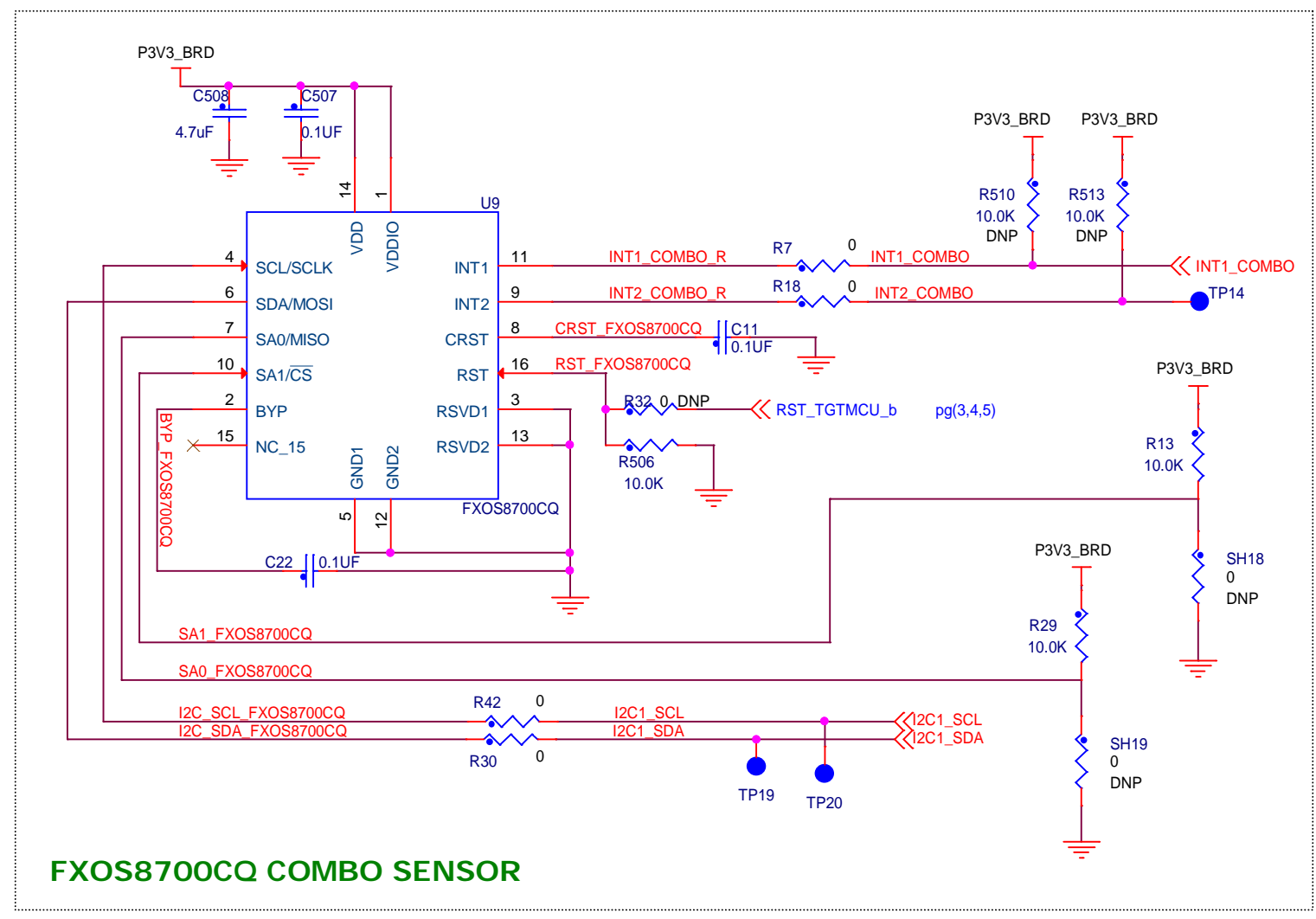
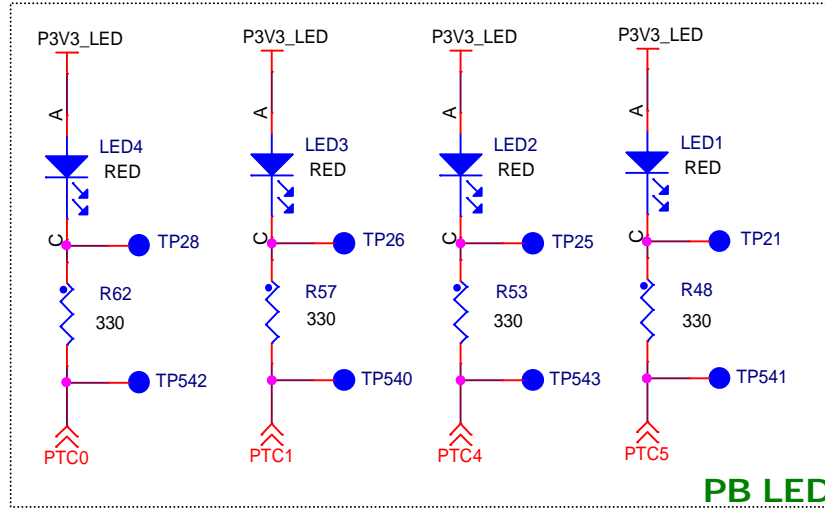
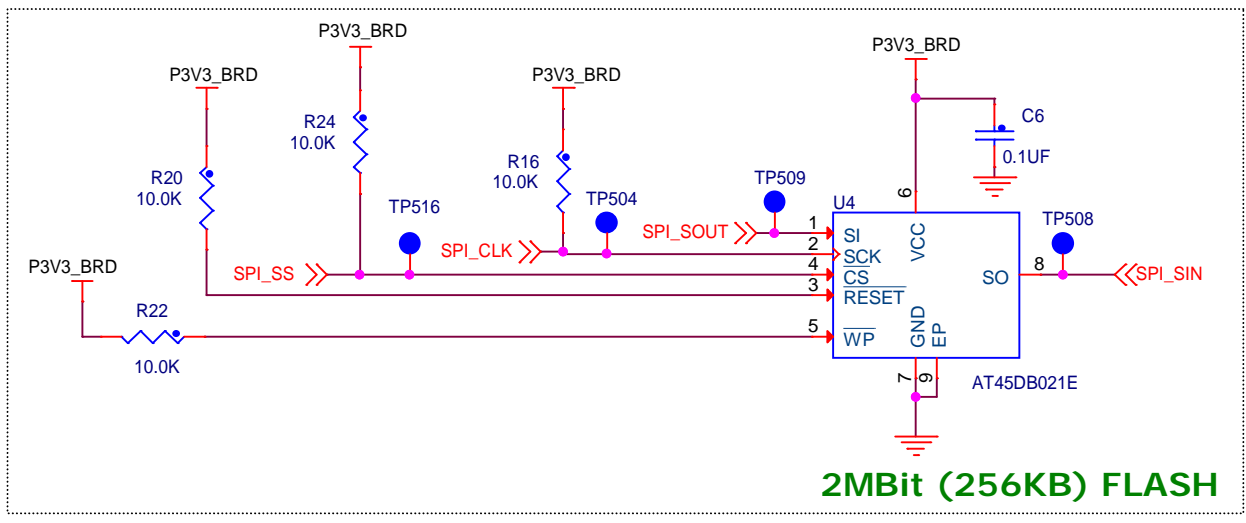
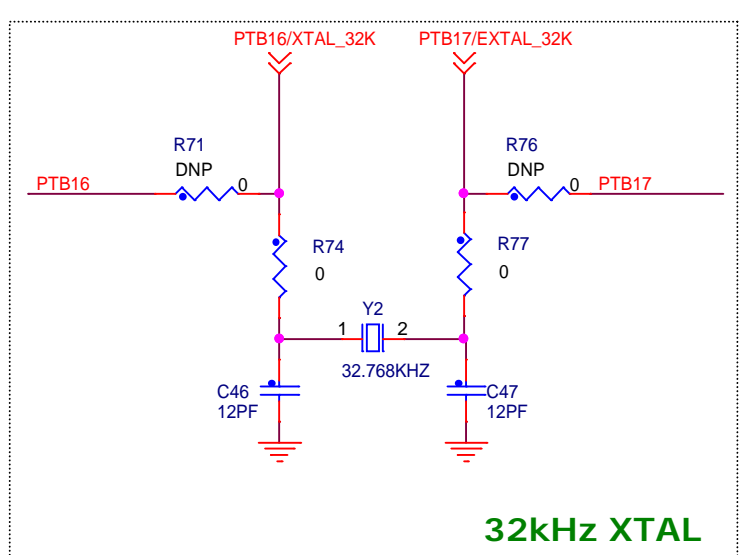
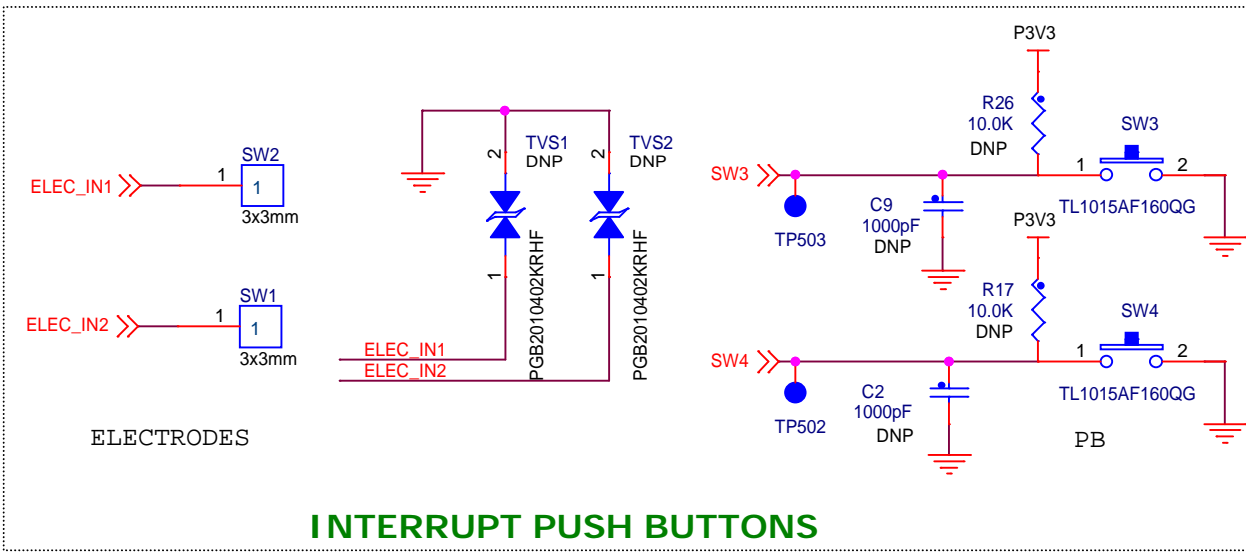
Page Title: **KW40x MCU**

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OpenSDA Interface





CAD NOTE:
MISO/MOSI POKA-YOKE:
Place both resistors with the same orientation and provide same airgap between MISO to MOSI resistors terminals in a square fashion.

CAD NOTE:
SCL/SDA POKA-YOKE:
Place both resistors with the same orientation and provide same airgap between SCL to SDA resistors terminals in a square fashion.

FRDM-KW40 signals to DEMO which require translation from 3.3 V to 5V. Zero Ohm 0402 Cut Trace PCB Footprint.