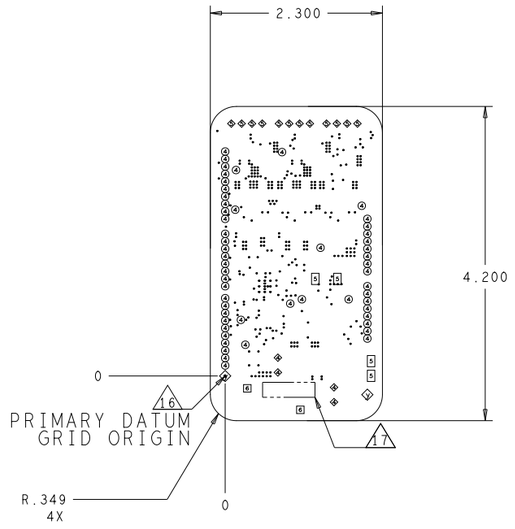
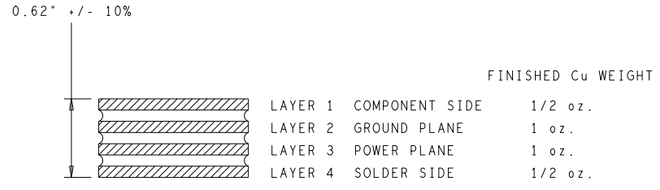
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	ORIGINAL RELEASE	11-10-16	A.M.
	B	Re-SPIN ECO66432	11-10-16	A.M.
	C	Re-SPIN ECO72075	04-03-17	A.M.
	D	Re-SPIN ECO76457	10-10-17	A.M.
	D1	SILK FIX START2->START3	11-01-17	A.M.

NOTES (UNLESS OTHERWISE SPECIFIED):

1. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-6012 CLASS 2 (LATEST REVISION).
2. THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.
3. BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101B-26, 83 or 98
   Tg - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
   Td - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.
4. COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A'
5. CHARACTERISTIC IMPEDANCE - NONE
6. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .010"/.008"
7. PLATING FINISH - BOTH SIDES ENIG (ELECTROLESS NICKEL IMMERSION GOLD):
   .07620-.232 MICRON (3-8 MICROINCH) OF GOLD OVER
   2.540-5.080 MICRON (100-200 MICROINCH) OF NICKEL.
8. ALL THROUGH HOLE VIAS MAY BE PLATED SHUT.
9. SOLDERMASK - GREEN COLOR (TAIYO OR EQUIVALENT), BOTH SIDES.
   MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM NXP.
10. SILKSCREEN - WHITE EPOXY INK, BOTH SIDES. NO SILK ON PADS.
11. ELECTRICAL TEST - 100% IPCD356.
12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.
13. DRC'S MUST BE RUN ON THE GERBER BEFORE BUILDING BOARDS, UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY NXP.
14. TEARDROPS MAYBE ADDED AT THE FAB HOUSE TO ALL SIGNAL LAYERS.
15. TWO SOLDER SAMPLES TO BE PROVIDED.
16. BASIC GRID INCREMENT AT 1:1 IS .0001.
17. SUPPLIER MARKINGS - ON SOLDER SIDE ONLY, WHERE SHOWN.
    - MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0
18. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP Pb
19. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP 260 C
20. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP. ALL HOLE LOCATION TOLERANCES ARE TO BE +/-.002 IN REFERENCE TO THE PRIMARY DATUM.
21. FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURERS REQUIREMENTS. THE ADDITION OF RAILS AND .125" NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF CONTRACT MANUFACTURER.PANELIZATION MUST BE APPROVED BY CONTRACT MANUFACTURER.
22. THIS BOARD USES VIA-IN-PAD:
    A. VIA-IN-PAD TO BE FILLED WITH NON-CONDUCTIVE VIA FILL.
       LACKWERKE-PETERS PP2795 OR EQUIVALENT AND MADE PLANAR TO THE PADS.
    B. OVERPLATE THE FILLED VIA AND APPLY FINISH METAL TREATMENT.
23. INTENTIONAL 8 SHORTS AT:

Location	RefDes	Net 1		Net 2
(4774.42 1020.51)	SH2	VSENSEN4	&	GND
(4774.42 1100.51)	SH1	VSENSEP4	&	N20122153
(4830.00 2395.00)	SH14	VSENSEN2	&	GND
(4830.00 2455.00)	SH13	VSENSEP2	&	N20116408
(6110.00 1980.00)	SH12	VSENSEN3	&	GND
(6140.00 2485.00)	SH3	VSENSEP1	&	N20093426
(6140.00 2425.00)	SH6	VSENSEN1	&	GND
(6170.00 1980.00)	SH11	VSENSEP3	&	N20145649





DETAIL A
LAYER STACKUP
SCALE: NONE

DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
·	10.0	+0.0/-10.0	PLATED	348
·	10.1	+0.0/-10.0	PLATED	12
⊕	40.0	+3.0/-3.0	PLATED	54
◈	45.0	+3.0/-3.0	PLATED	4
⊡	51.0	+3.0/-3.0	PLATED	4
◈	55.0	+3.0/-3.0	PLATED	12
⊠	64.0	+3.0/-3.0	PLATED	2
◈	125.0	+2.0/-2.0	NON-PLATED	2

22 8 8

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X IUO (NXP INTERNAL USE ONLY)
___ CP (NXP CONFIDENTIAL PROPRIETARY)

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UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS ANGLES
.XX .01 .0-30'
.XXX .005
✓ RMS ALL MACHINED SURFACES
BREAK ALL SHARP EDGES AND CORNERS. REMOVE BURRS.
UNDERLINED DIM. NOT TO SCALE.
THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.

PART NO. 170-29357

APPROVALS	DATE
DRAWN C. CRACIUN nPRO	11-01-17
CHECKED ANDREW MacDONALD	11-01-17
DESIGN ENGINEER PIERRE CALMES	11-01-17

NXP SEMICONDUCTORS
6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA

TITLE: PRINTED WIRING BOARD
FRDMPT2001EVM

SIZE	CAD FILE NAME	DWG. NO.	REV
D	LAY-29357	FAB-29357	D1

SCALE 1/1 DO NOT SCALE DRAWING SHEET 1 OF 1