

**MPC7441**  
**MPC7445**  
**MPC7447**  
**MPC7447A**

**intelligence**  **everywhere™**

**digital dna™** 

Schematic Notes

1.

Unless otherwise specified:  
All resistors are SMD0603, in ohms, 0.08W, +/-5%  
All capacitors are SMD0603, in microfarads (uF), +/-20%.  
All inductances are in microhenries (uH).  
All ferrites are Z=50 ohms at 100 MHz.  
All fuses are self-resetting polyswitch (PTC) devices.  
Board impedance is 55 +/- 5 ohms.

2.

Integrated circuits have default connections to power and ground unless explicitly shown otherwise. Global power connections are:  
GND            VCACHE            VCACHE\_IO  
VCC\_3.3       VCC\_2.5       OVDD  
VCC\_5        VCCORE       VCC\_12

3.

Part numbers used are for reference only; compatible parts may be used; refer to the bill of materials.


4.

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5.

The sheet-to-sheet cross reference format is:  
Sheet "\*" VertZoneLetter HorizZoneNumber

6.

Components with the visible property "NO STUFF" are not to be installed by default; they are for test or manufacturing purposes only.  


7.

All buses follow big-endian bit numbering order (bit 0 is the most-significant bit), except where industry standards apply (i.e. PCI). Little-endian numbering is noted at the source component.

Gyrus\*

Team Gyrus

Cindy Callis      Layout  
Ivan Erickson    Program Mgr.  
Gary Milliorn    Designer  
Tony Saucedo    Components  
Margarito TrevinoTechnician  
Gary Wojcik      Ref. Plat. Mgr

Date Changed: 7/7/2003

Time: 4:23:59 pm

Engineer: Gary Milliorn

Drawing Number: M03GYRUS

REV: X3

Project: Gyrus

TITLE: Information, please

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Analyzer Headers

REV

DATE

CHANGES

X1

01MAY25

Initial version

X2

01NOV01

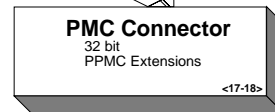
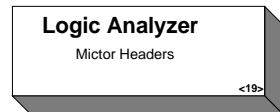
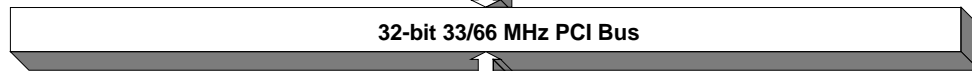
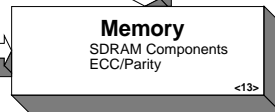
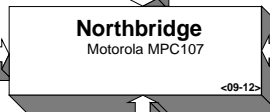
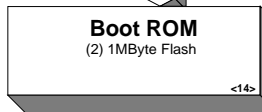
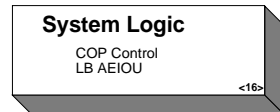
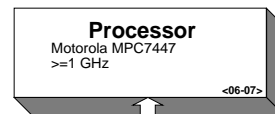
Fix for DQM scramble.

X3

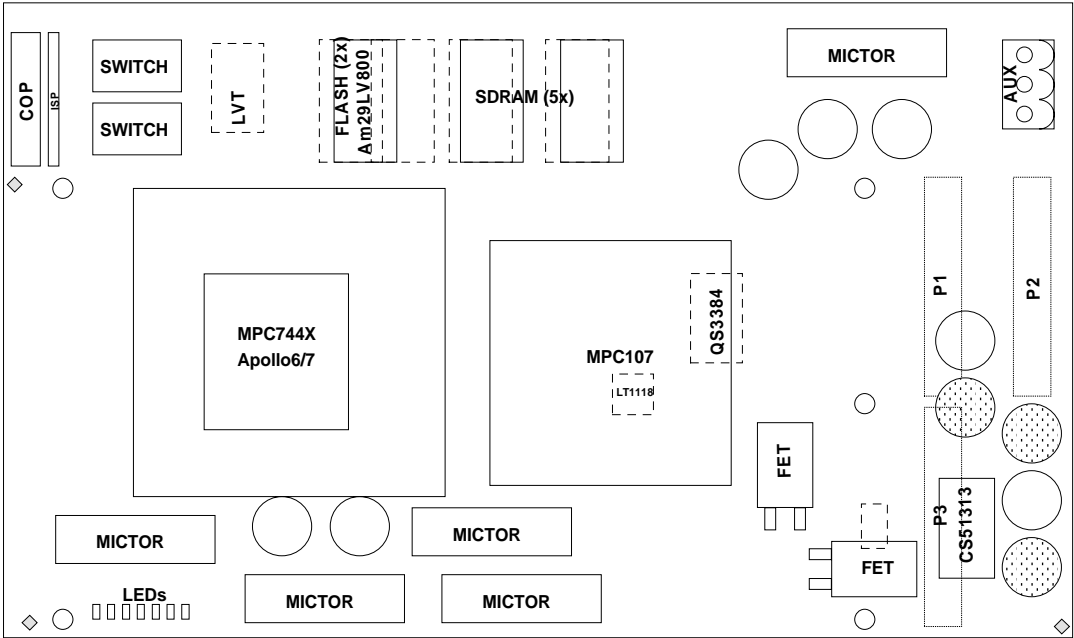
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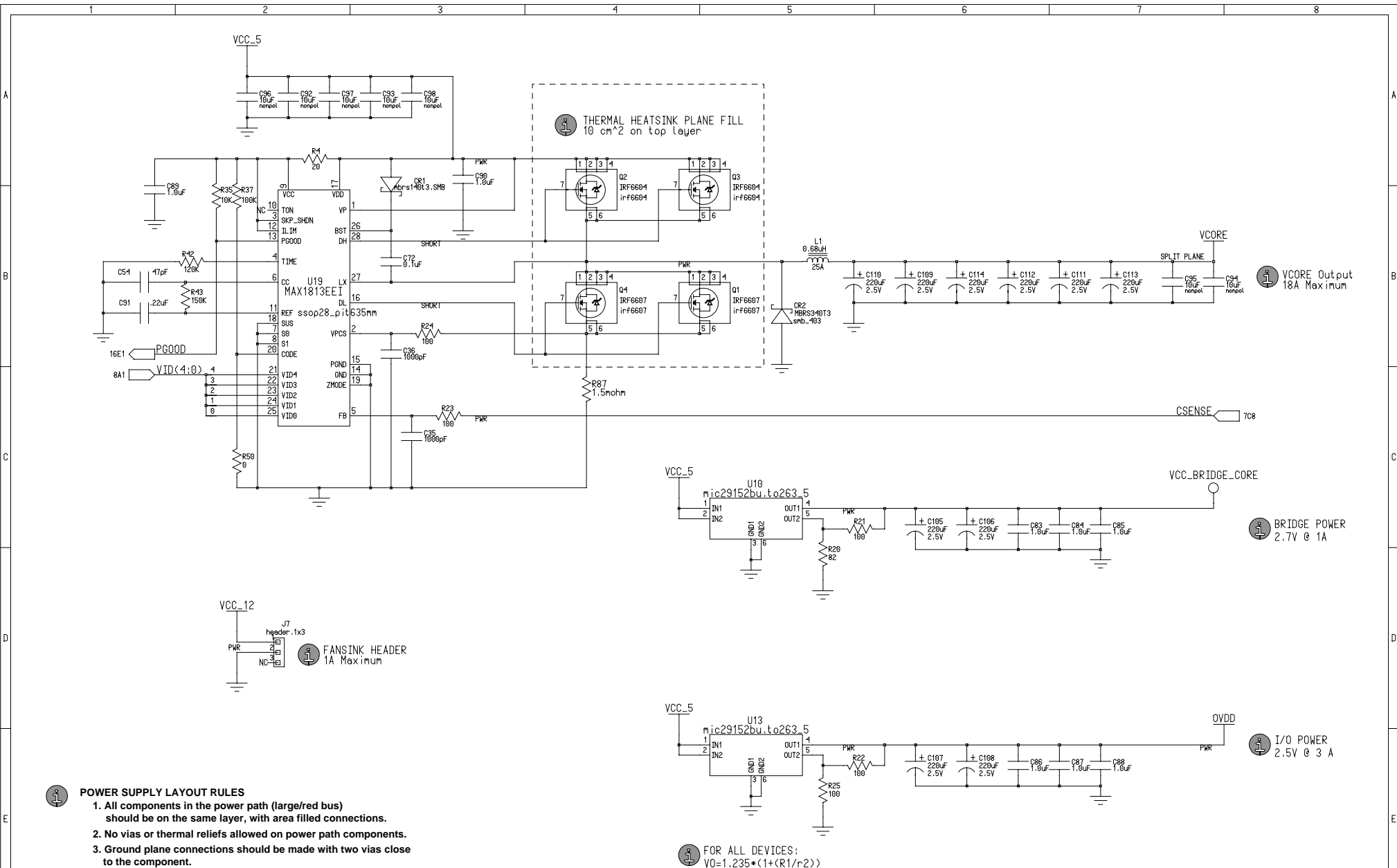
VCORE Upgrade; A7PM

Motorola 6501 William Cannon Blvd, Austin, TX 78735



	1	2	3	4	5	6	7	8
	Layout/ Routing Instructions							
05	Place components approximately as shown on this page. Keep relative distances short and use heavy traces for everything. All power connections are to be made to a plane.							
06	Avoid routing traces, especially noisy ones, across CPUPLL bus.							
07	Keep AVDD filter near CPU. Route all groups to equal lengths. L3RU L3RL L3X							
08	Avoid routing traces, especially noisy ones, across CPUPLL bus. Do not swap order of PLL switch connections. Surround MPC7450 with bypass caps to provide additional ground-return paths. Use two ground-attach vias. Place bulk capacitance near BGA IVDD and +3.3V ground planes. Place COP connector in I/O area. Proximity to CPU is not a high priority. Insure that COP pin numbering matches view as shown on schematic (i.e. pin 1 and pin 16 are on opposite corners).							
09	Place cache SRAMs within 3.5cm of MPC750 (center-to-center). Route all control, address and data traces to equal lengths. Surround each component with bypass capacitors. Use thick trace (>=12mil) for VREF, 24mil for VCACHE.							
10								
11	Avoid routing traces, especially noisy ones, across MPC107 PLL bus. Do not swap order of MPC107 PLL switch connections. PCI clock input must be 2.5" (per specification).							
12								
13	Keep AVDD/LAVDD filters near MPC107. Use heavy, short traces from filter to pins. Surround MPC107 with bypass caps to provide additional ground-return paths. Use two ground-attach vias. Connect VCC_PCI_C (PCI Clamp) using heavy trace.							
14	Place series termination resistors very near source (MPC107). < 2cm. Route SDRAM clocks to equal lengths, including SDRAM_SYNCOUT to SDRAM_SYNCIN path.							
15								
16	Keep data bus length for ROM short.							
17								
18	Maximum trace length for PCI signals to MPC107 is 1.5" per the PCI specification.							
19								
20								



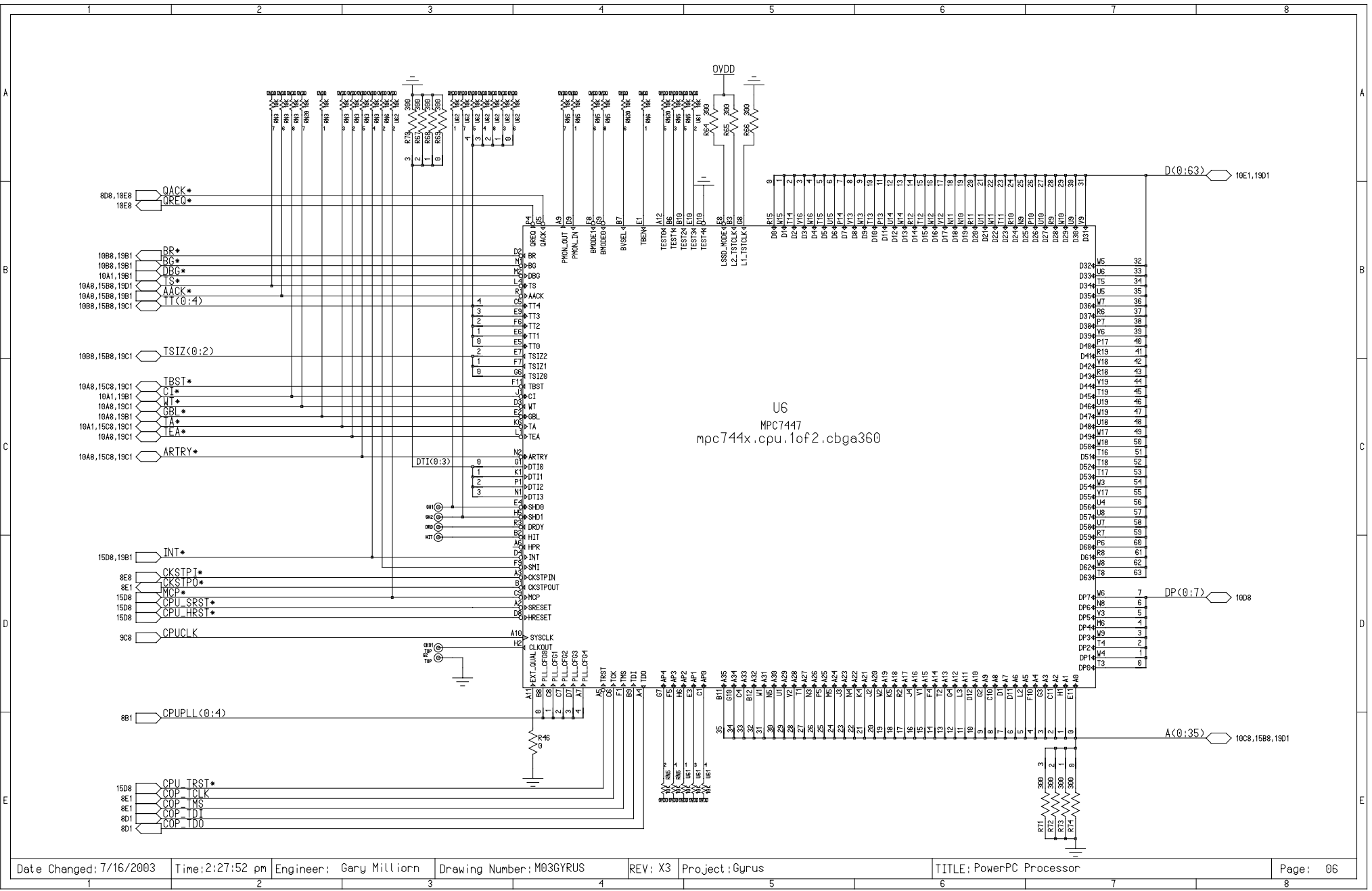


**POWER SUPPLY LAYOUT RULES**

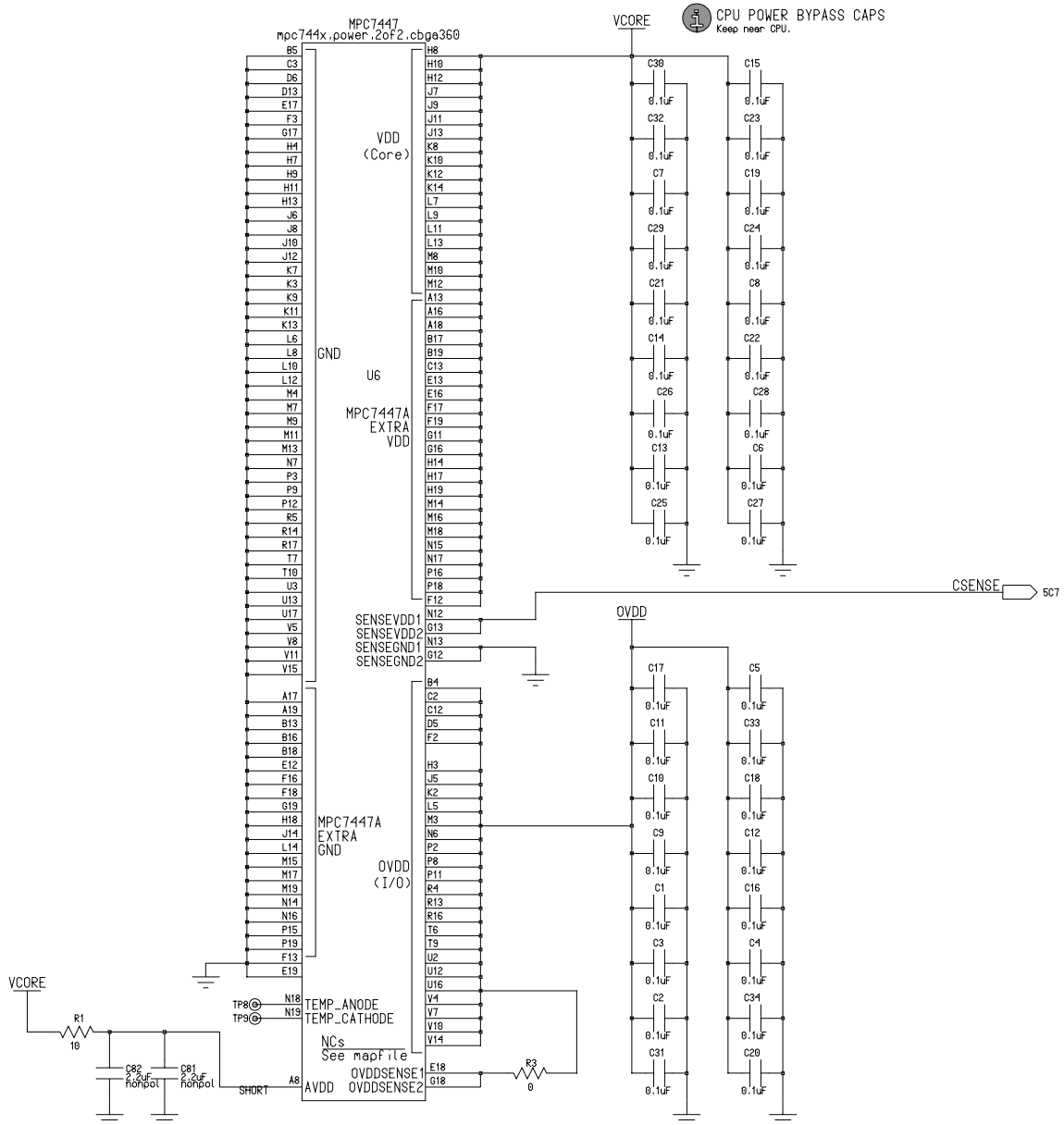
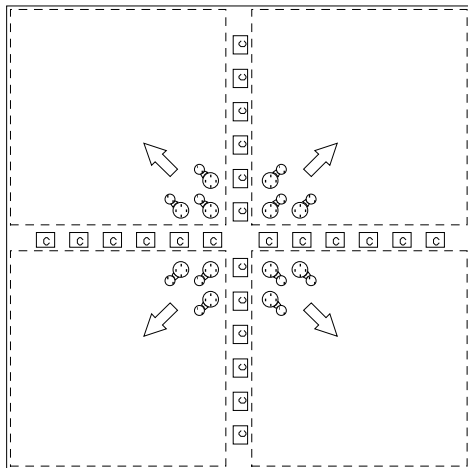
1. All components in the power path (large/red bus) should be on the same layer, with area filled connections.
2. No vias or thermal reliefs allowed on power path components.
3. Ground plane connections should be made with two vias close to the component.

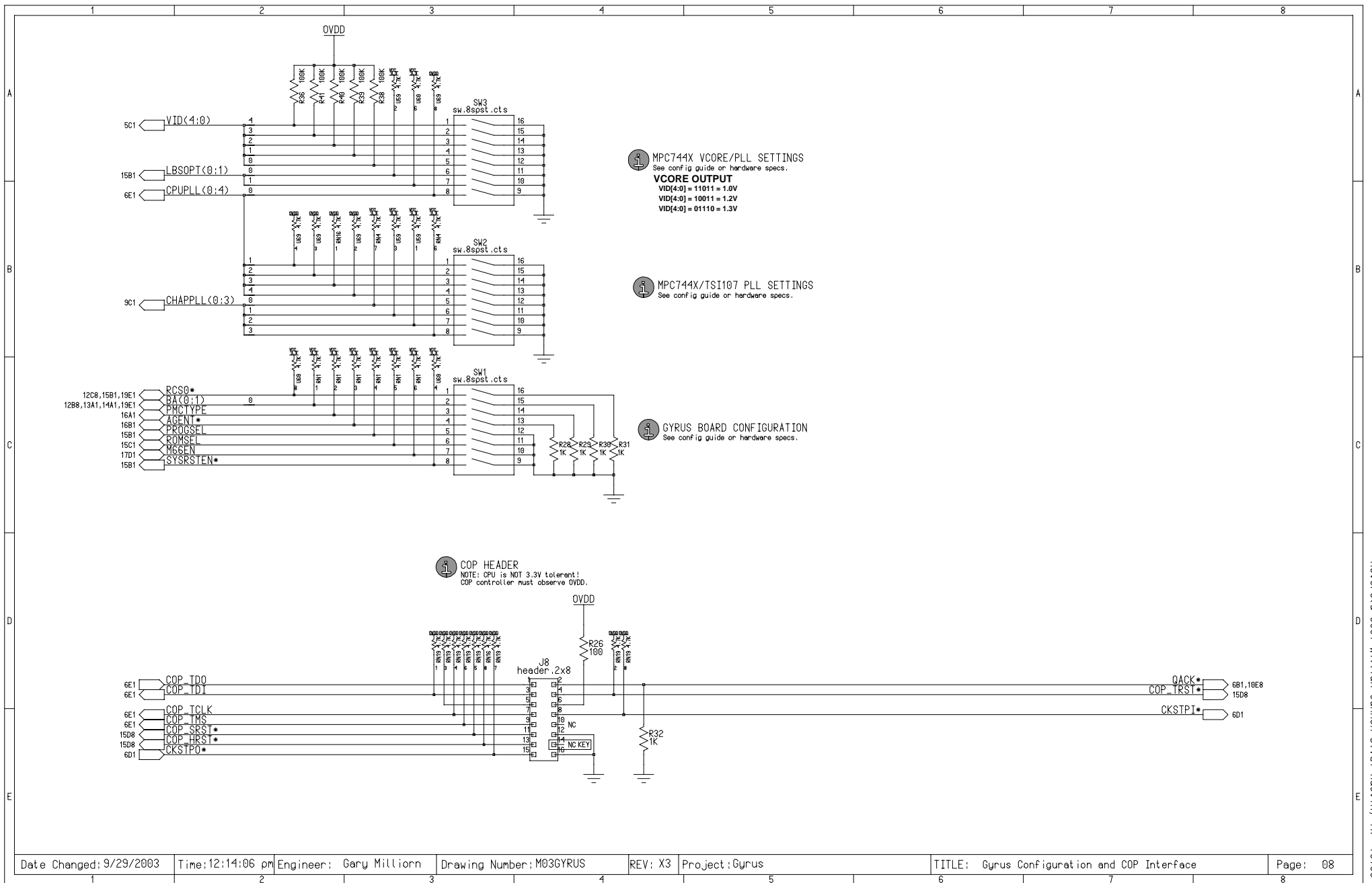


FOR ALL DEVICES:  
V0=1.235\*(1+(R1/r2))

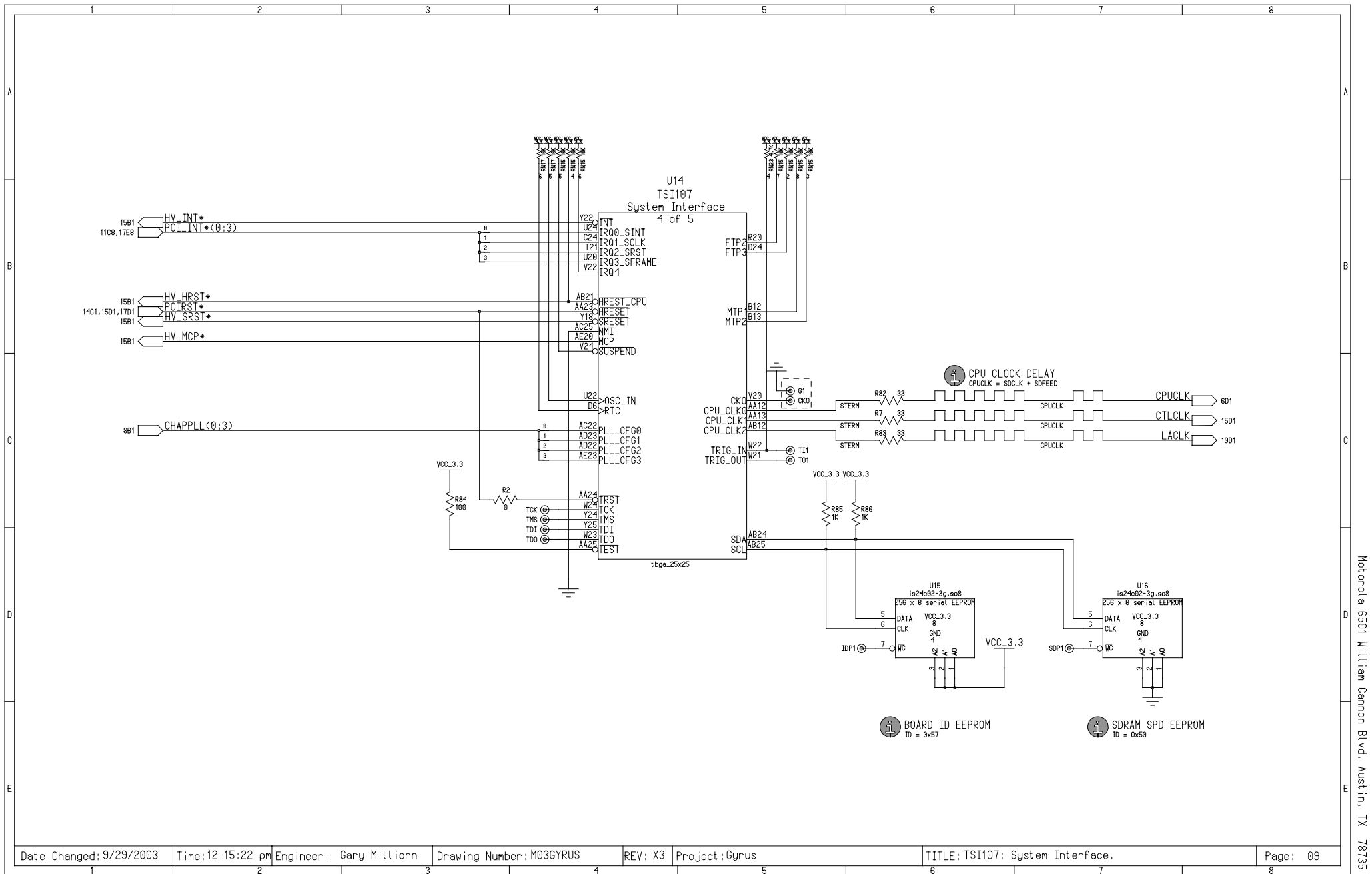


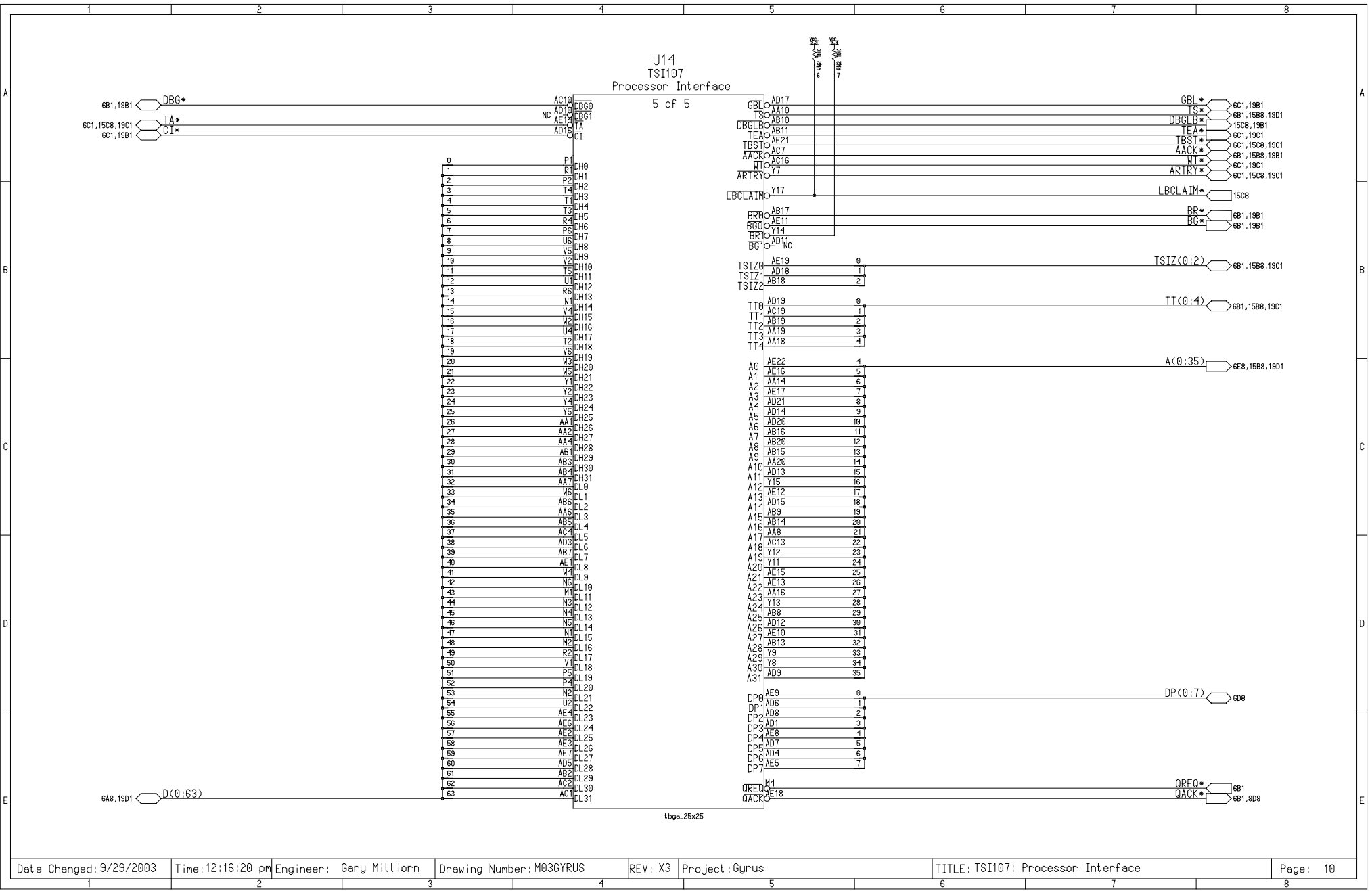
CBGA360 ESCAPE PATTERN  
and CAPACITOR PLACEMENT

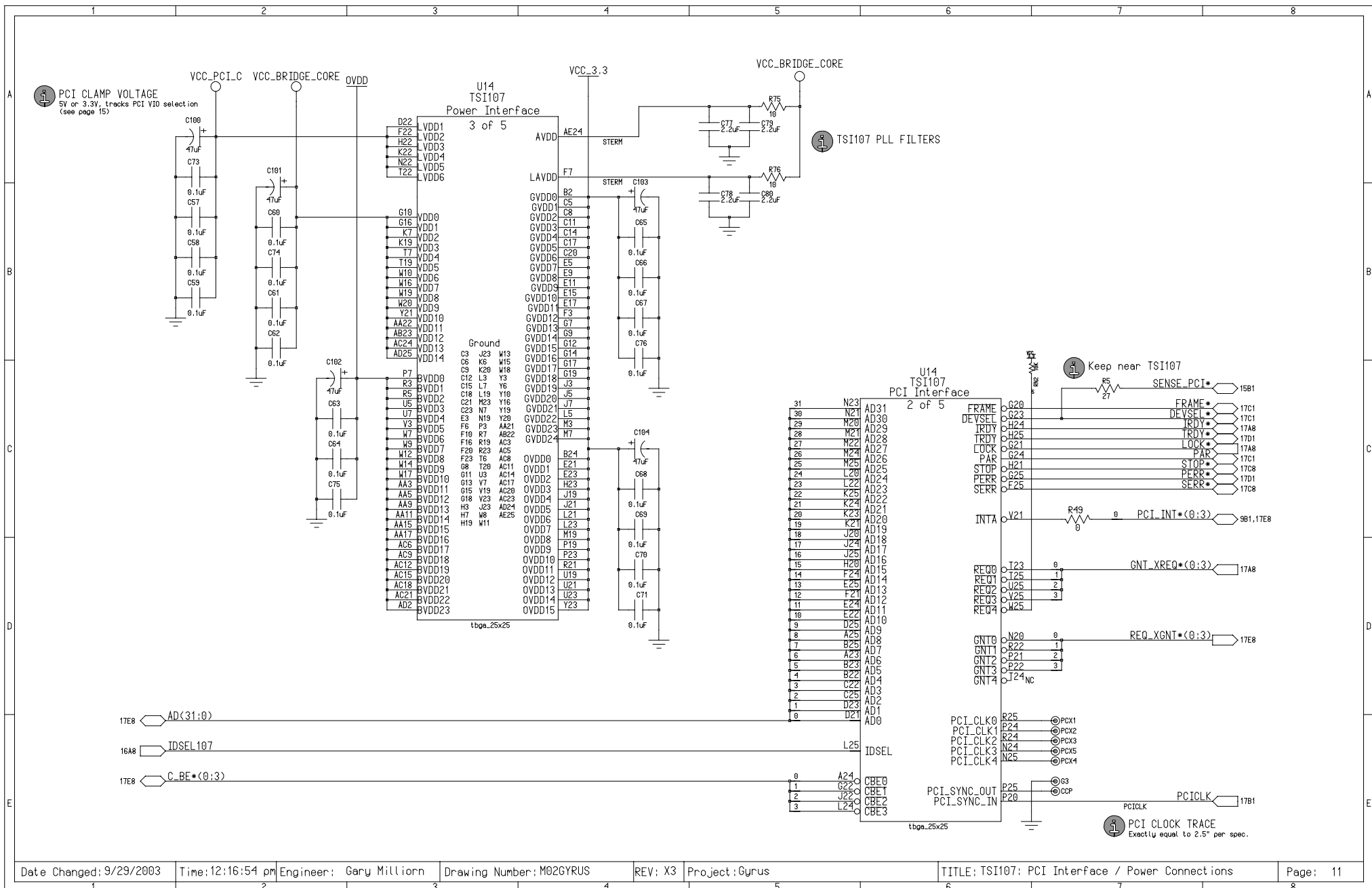


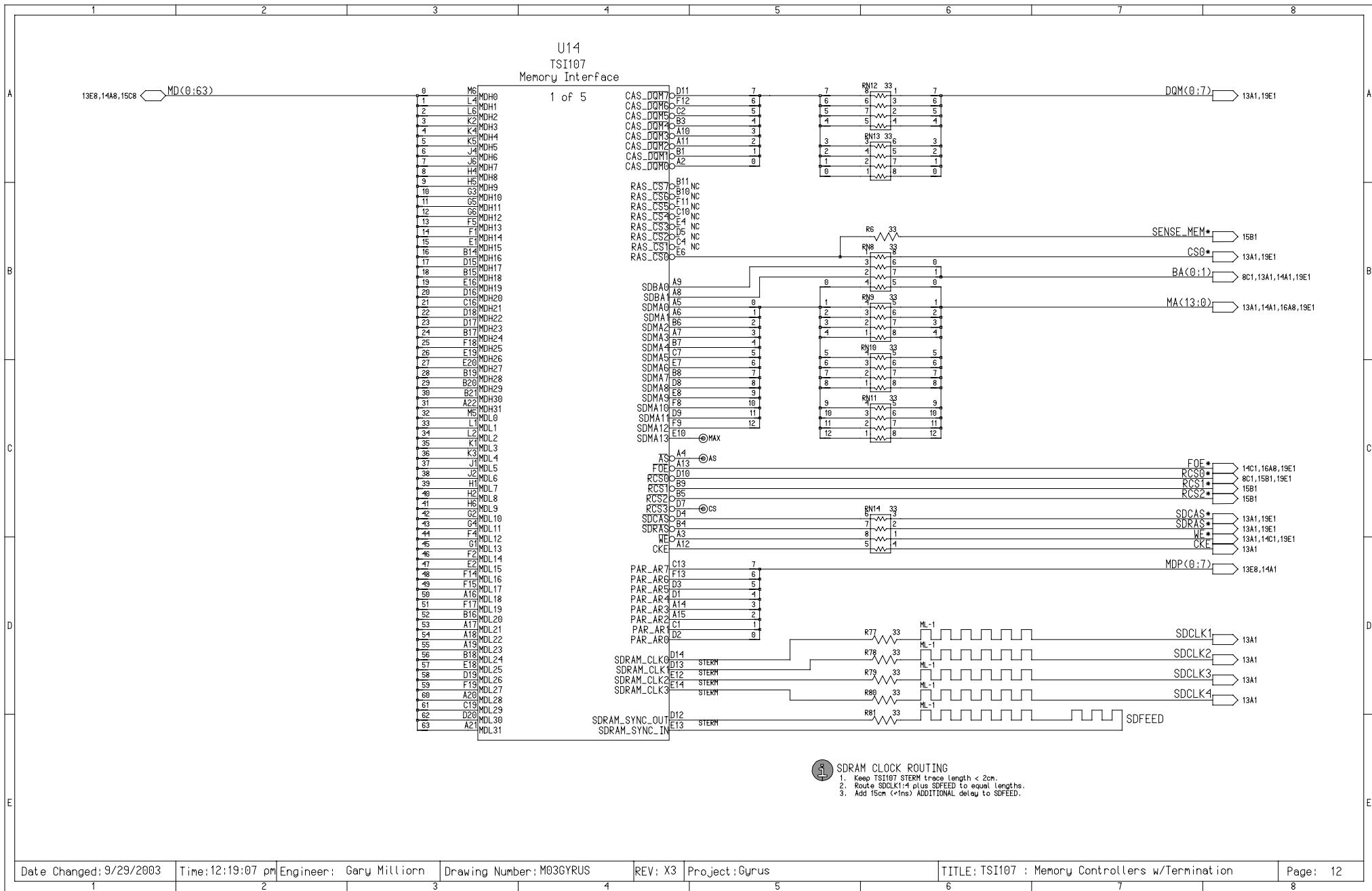


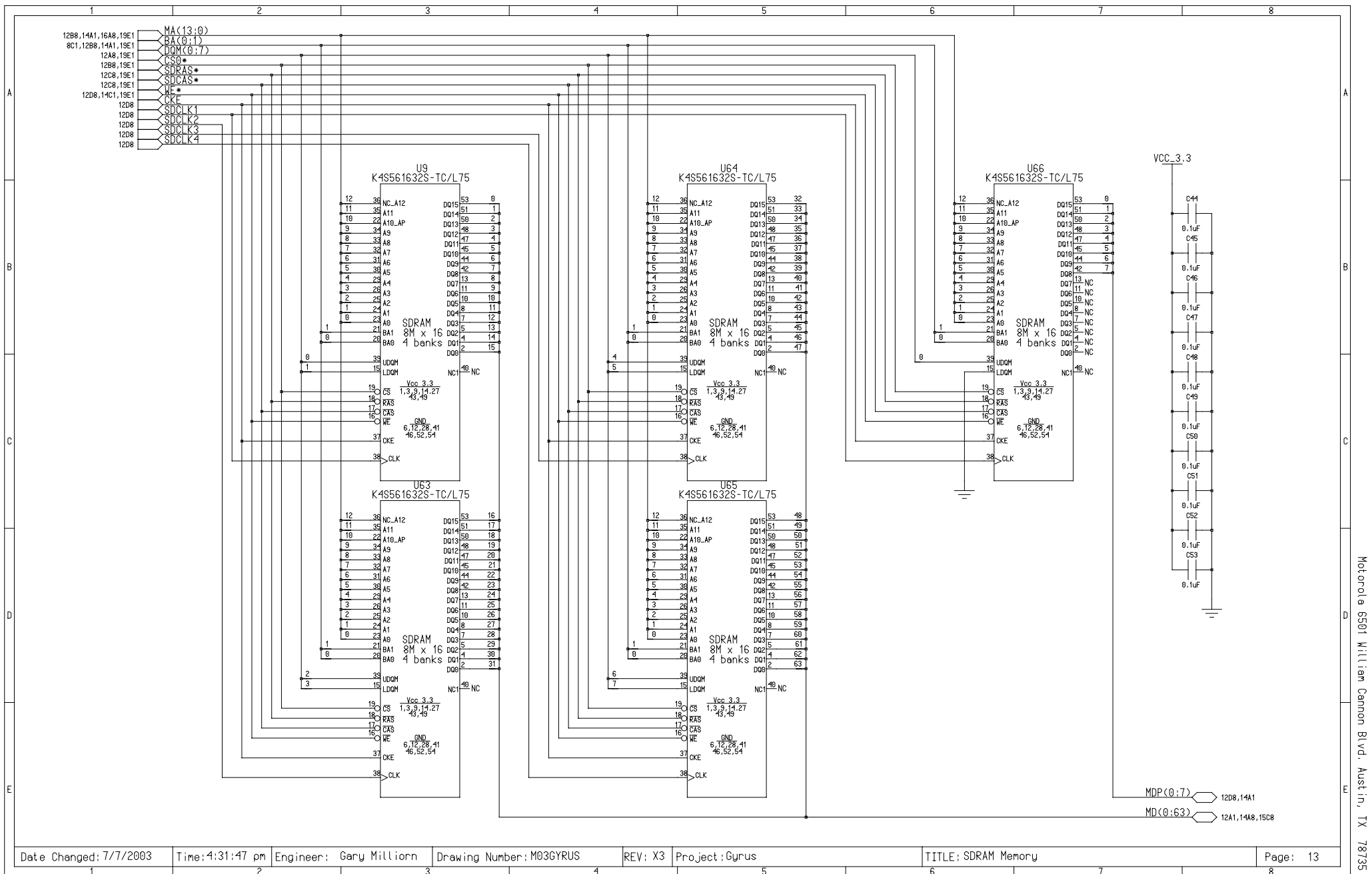


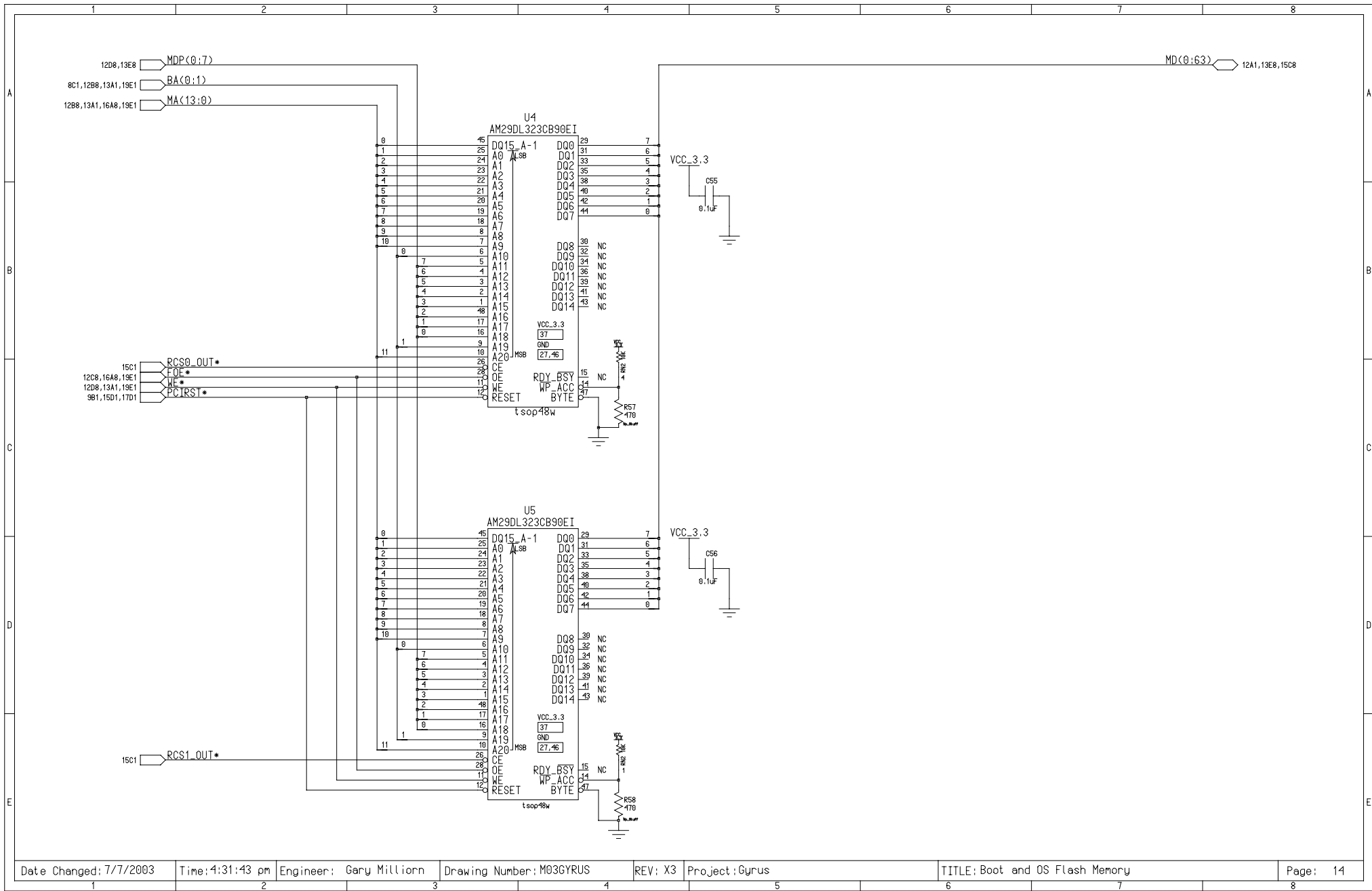




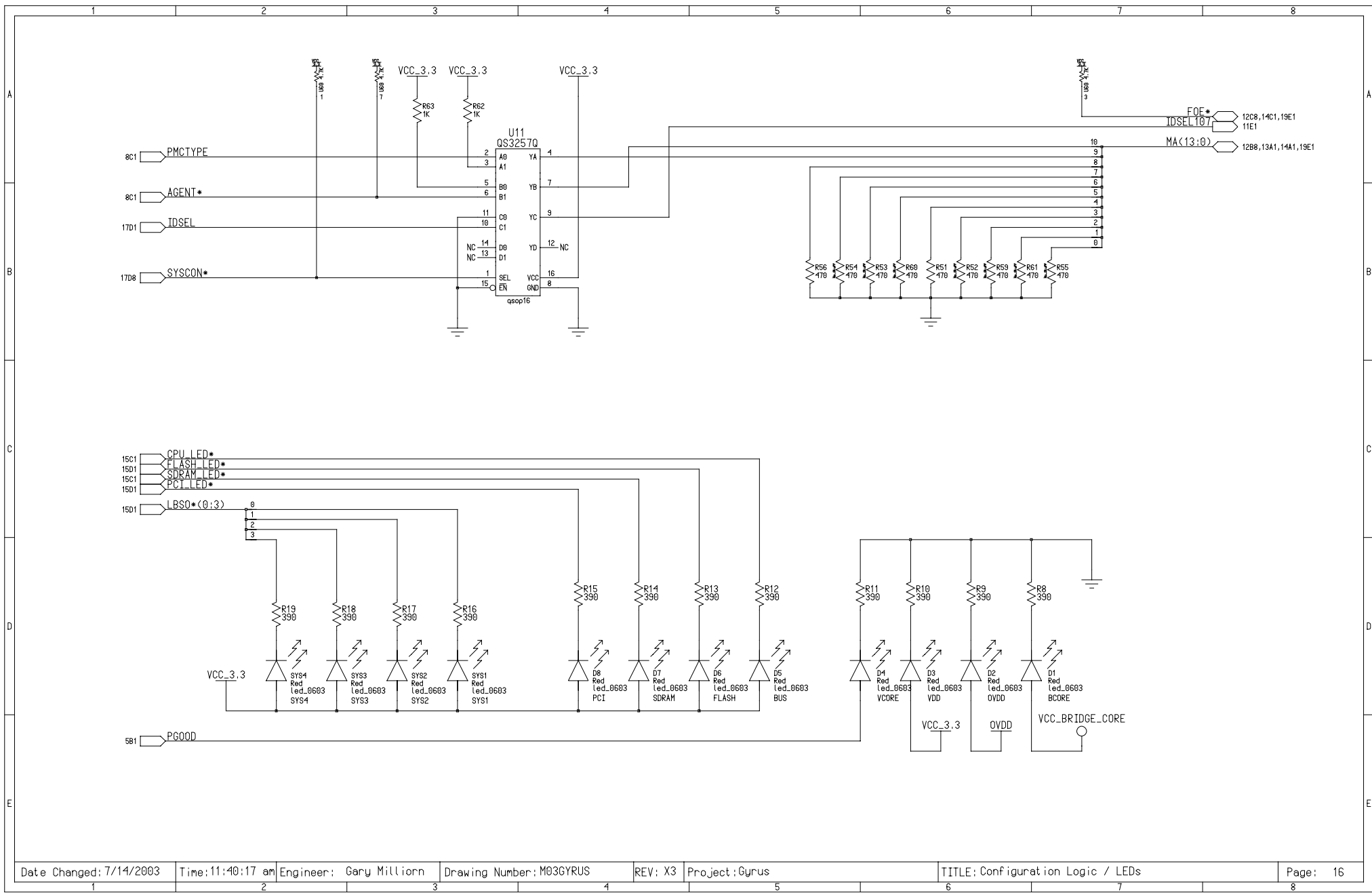






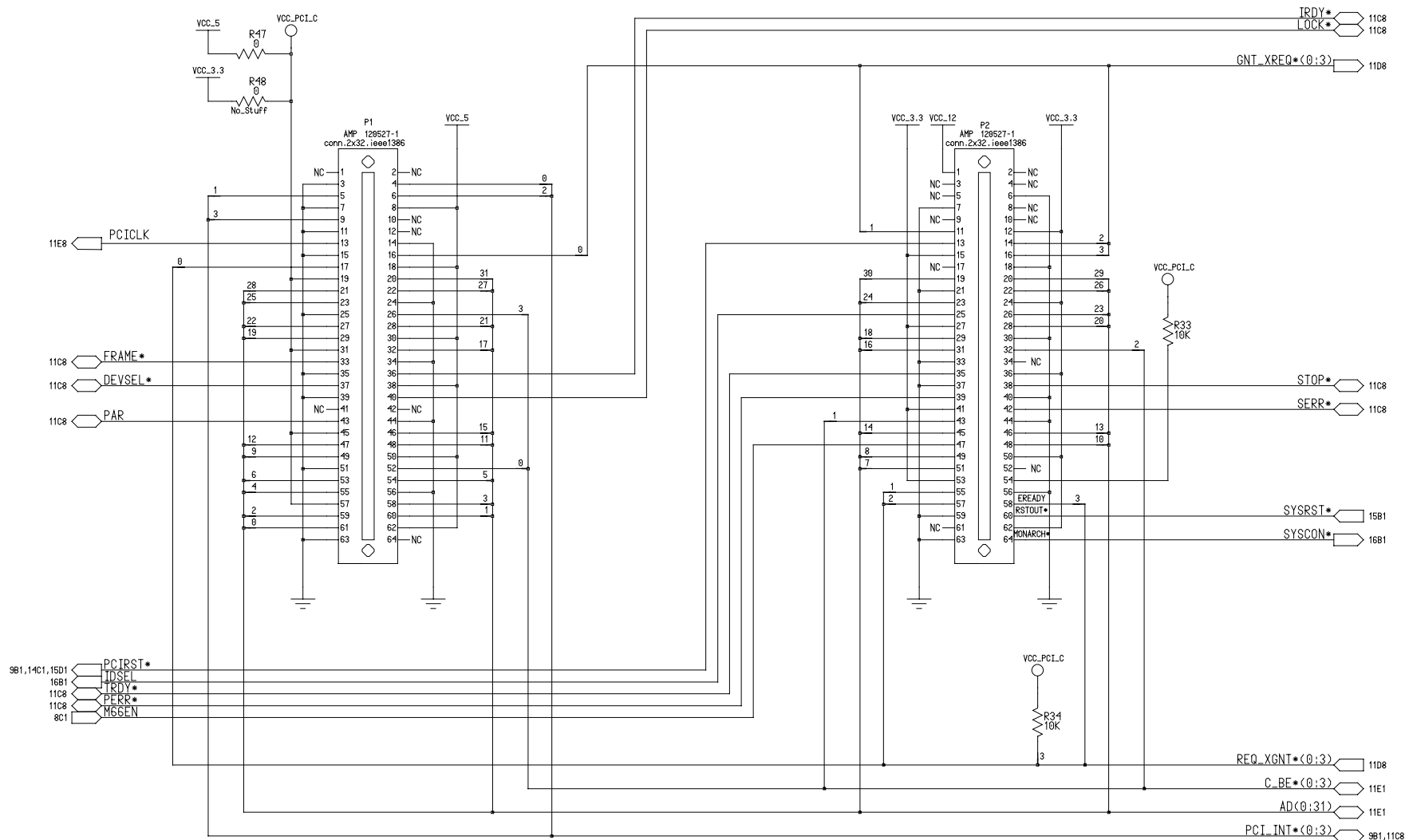


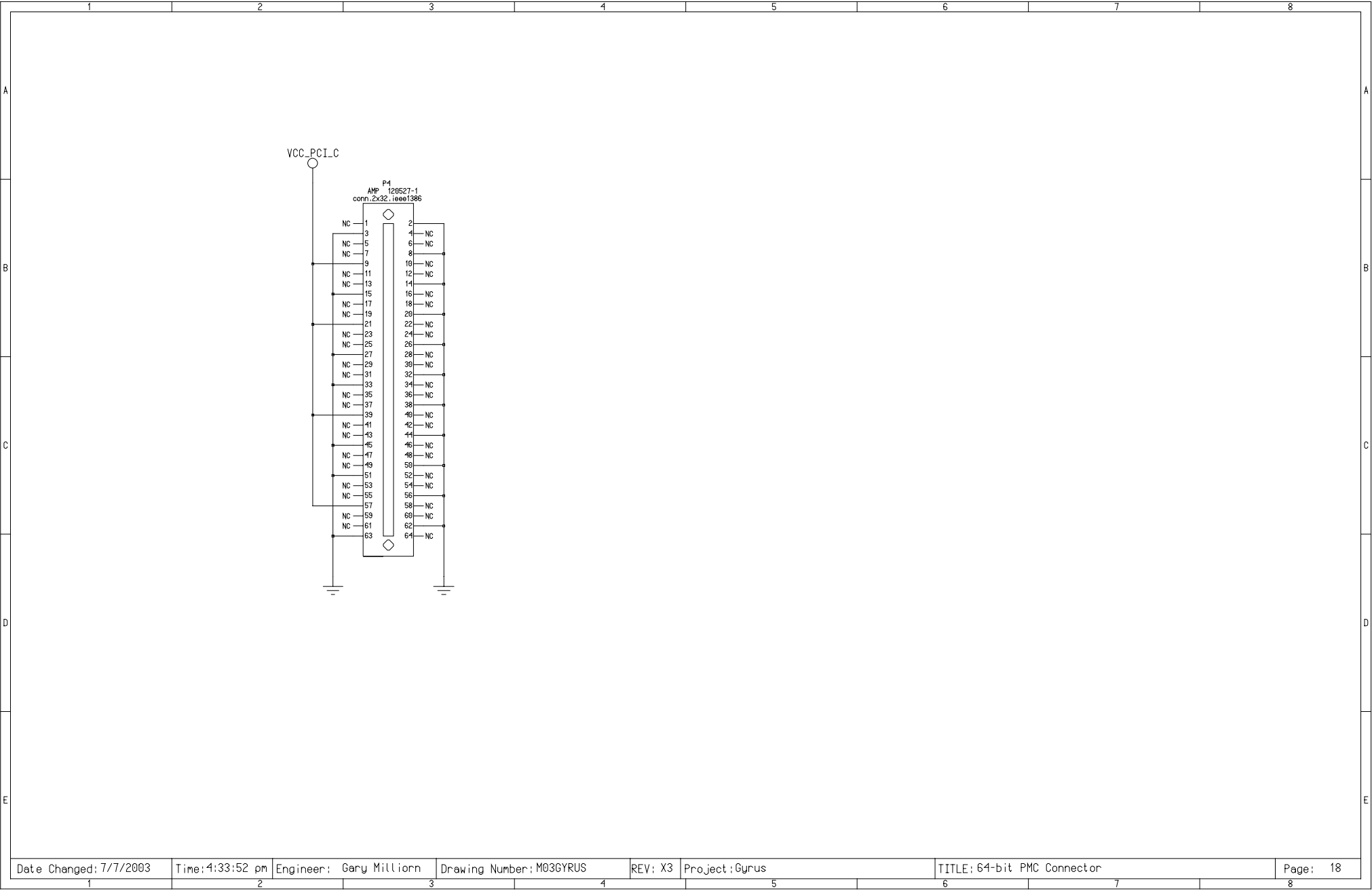


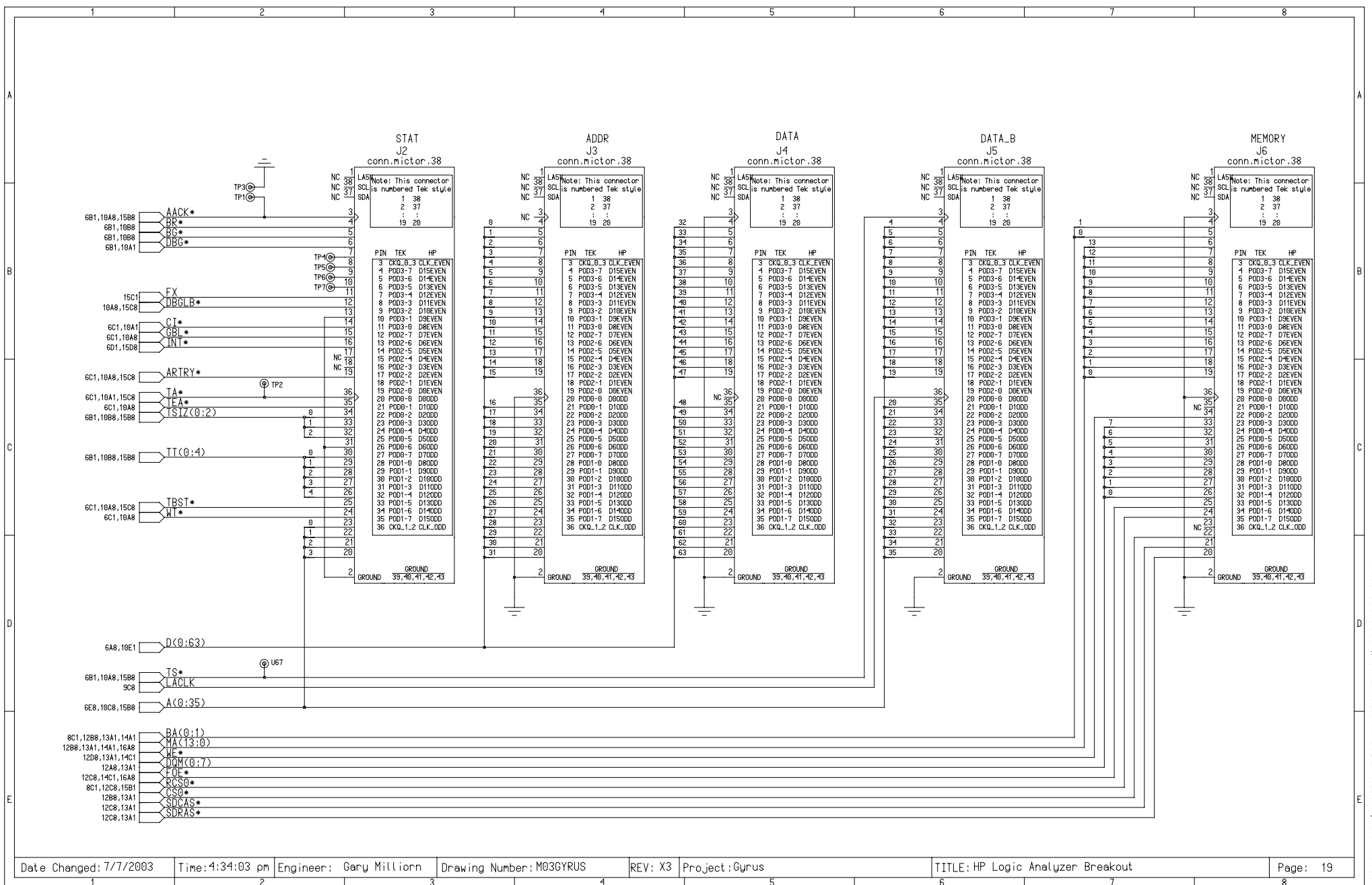




1 PCI VIO SELECTION  
 V<sub>I</sub> on 3.3V; MUST match MPMC carrier  
 (Sandpoint, Arcadia, etc.)











1		2		3		4		5		6		7		8																																	
<table><tr><td colspan="4">REFDES</td><td colspan="4">GND</td><td colspan="4">OVDD</td><td colspan="4">VCC_3.3</td></tr><tr><td colspan="4">J2 J3 J4 J5 J6 RN1 RN2 RN4 RN15 RN17 RN21 RN22 RN23 RN3 RN5 RN6 RN16 RN19 RN20 RN24 RN25 RN26 U4 U5 U9 U63 U64 U65 U66 U12 U14  U15 U16</td><td colspan="4">39 40 41 42 43  27 46 54 52 46 41 28 12 6 11 26 38 43 59 74 86 95 C3 D6 C9 C12 C15 C18 C21 C23 E3 F6 F10 F16 F20 F23 G8 G11 G13 G15 G18 H3 H7 H19 J23 K5 K20 L3 L7 L19 M23 N7 N19 P3 R7 R19 R23 T6 T20 U3 V7 V19 V23 W8 W11 W13 W15 W18 Y3 Y6 Y10 Y16 Y19 Y20 AA21 AB22 AC3 AC5 AC8 AC11 AC14 AC17 AC20 AC23 AD24 AE25 4</td><td colspan="4">9 10   39 91</td><td colspan="4">9 10 37 49 43 27 14 9 3 1   8</td></tr></table>																REFDES				GND				OVDD				VCC_3.3				J2 J3 J4 J5 J6 RN1 RN2 RN4 RN15 RN17 RN21 RN22 RN23 RN3 RN5 RN6 RN16 RN19 RN20 RN24 RN25 RN26 U4 U5 U9 U63 U64 U65 U66 U12 U14  U15 U16				39 40 41 42 43  27 46 54 52 46 41 28 12 6 11 26 38 43 59 74 86 95 C3 D6 C9 C12 C15 C18 C21 C23 E3 F6 F10 F16 F20 F23 G8 G11 G13 G15 G18 H3 H7 H19 J23 K5 K20 L3 L7 L19 M23 N7 N19 P3 R7 R19 R23 T6 T20 U3 V7 V19 V23 W8 W11 W13 W15 W18 Y3 Y6 Y10 Y16 Y19 Y20 AA21 AB22 AC3 AC5 AC8 AC11 AC14 AC17 AC20 AC23 AD24 AE25 4				9 10   39 91				9 10 37 49 43 27 14 9 3 1   8			
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